Advanced Packaging Trends in the Semiconductor Industry

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Abstract. Advanced packaging is an important technology that is now taking over from advanced processes to help the semiconductor industry continue to grow. The researcher found that the personnel in contact with the semiconductor industry chain have already had a preliminary understanding of advanced packaging, however, the future development trend of the advanced packaging industry still lacks a comprehensive knowledge. Therefore, the research topic of this paper is the development trend of advanced packaging industry. The research methodology of this paper is as follows: firstly, to understand the concept and development trend of advanced packaging, secondly, to list the factors driving the development of advanced packaging, and finally, to understand the development direction of international enterprises in advanced packaging. This paper finds that after the chip process technology has entered the "post-Moore era", advanced packaging has been widely used in the fields of high-end logic chips, memories, RF chips, image processing chips, touch chips and so on. Advanced packaging technology tends to be diversified in function, stacking and connection. According to Yole, a market research organization, the global share of advanced packaging in the IC packaging and testing market will continue to increase. At the same time, Yole predicts that the global compound annual growth rate of traditional packaging will be only 1.9% from 2019 to 2025, which is much lower than the growth rate of advanced packaging. Advanced packaging is the key path to improve system performance in the post-Moore era.

Keywords: Advanced Packaging, Development Trends, Post-Moore Era.

1. Introduction

Advanced packaging is now entering a stage of rapid development due to its advantages of high economic efficiency, high packaging density and high integration. In the post-Moore era, chip manufacturing is facing the dual challenges of physical limits and marginal improvement of economic benefits, advanced process technology is gradually approaching the physical limits, further reducing the feature size has become particularly difficult, and many vendors have begun to change the direction of research and development from "how to make the chip smaller" to "how to seal the chip smaller". Chip sealed smaller". Advanced packaging plays a more important role in the process of improving chip integration, electrical connection and performance optimization, and all links in the industry chain benefit from this round of technological innovation. Currently, advanced packaging leads the growth of the global packaging market. Global packaging market by technology type, advanced packaging growth rate is much higher than the traditional packaging, is expected to 2026, the overall market share of advanced packaging will be more than 50%, become the core of the packaging industry growth [1].

At the beginning of advanced packaging, there were only a few choices of WLP, 2.5D package and 3D package. In the case of the process remains unchanged, through the high-speed interconnection, 3D structure, etc. to achieve system performance breakthroughs, to achieve the Moore's law beyond, that is, "More than Moore", and one of them, the advanced packaging this road has now begun to show results. In recent years, the development of advanced packaging has exploded in all directions, and each company that develops related technologies has independently named and trademarked its own technology, such as TSMC's InFO, CoWoS, Sun Micron's FoCoS, Amkor's SLIM, SWIFT, and so on.

One of the most effective ways for IC manufacturers to stay ahead of the curve in terms of smaller size, lower cost, and higher performance is to integrate more advanced chip packaging technologies,

such as 3D integrated circuits, into the overall manufacturing process. These advanced packaging technologies ensure higher quality chip connections and lower power consumption than traditional packaging technologies. Although most of these technologies are not yet fully developed, they still have great advantages in the future of IC manufacturing [2]. This paper analyzes the development trend of advanced packaging in semiconductor industry based on past data and information, and hopes to explore the future development direction of advanced packaging by combing the current development pattern of advanced packaging.

2. Advanced Packaging Concepts and Development Trends

2.1. Advanced Packaging Concepts

Semiconductor packaging is a semiconductor manufacturing process of the latter process, refers to the wafer processing through the test to get an independent chip process, that is, the production of semiconductor devices, placed in a plastic, ceramic or metal shell with the support of mechanical protection, so that it is free from the loss of physical, chemical and other environmental factors, and finally through the cutting, welding, plastic sealing of circuits and external devices to achieve the connection of the process. Advanced packaging refers to packaging forms and technologies at the cutting edge. Advanced packaging is characterized by the use of stacking, heterogeneous integration (meaning the integration of different types and functions of chips into the same package) and other technologies, mainly including wafer-level packaging (WLP), silicon through-hole (TSV), 2.5D packaging, 3D packaging, system-in-package (SiP) and other packaging technologies [3, 4].

2.2. Advanced Packaging Development Trends

Table 1. Advanced Packaging Development History

Point	Timing	Package form	Specific typical package form
Phase I	Prior to the 1970s	Through-Hole Cartridge Package	Transistor Package (TO), Ceramic Dual In-line Package (CDIP), Plastic Dual In-line Package (PDIP)
Phase II	1980s onwards	Surface Mount Package	Plastic Leaded Chip Carrier Packages (PLCC), Plastic Quad Leaded Flat Packages (PQFP), Small Outline Surface Packages (SOP), Leadless Quad Flat Packages (PQFN), Small Outline Transistor Packages (SOT), Dual Side Flat Pinless Split Packages (DFN)
Phase III	1990s	Ball Grid Array Package (BGA)	Plastic Ball Array Package (PGBA), Ceramic Ball Array Package (CBGA), Heat Sink Ball Array Package (EBGA), Flip Chip Ball Array Package (FCBGA)
		Wafer Level Packaging (WLP)	
		Chip-Scale Packaging (CSP)	Leadframe CSP packages, flexible insertion board CSP packages, rigid insertion plate CSP packages, wafer-level CSP packages
Phase III	Since the end of the 20th century	Multi Chipset Package (MCM)	Multilayer ceramic substrates (MCM-C), multilayer thin film substrates (MCM-D), multilayer printing plates (MCM-L)
		System in Package (SiP)	
		Three-dimensional stereoscopic packaging (3D)	
Phase IV	Beginning of the first decade of the twenty-first century	Bumping on chips	
		Micro Electro Mechanical Systems Packaging (MEMS)	
		Wafer Level System Packaging - Silicon Through Hole (TSV)	
		Flip-Chip Package (FC)	
		Surface activated room temperature connection (SAB)	
		Fan-Out Integrated Circuit Packages (Fan-Out)	
		Fan-in IC Packages (Fan-in)	

In the post-Moore era, the development trend of advanced packaging has been determined, such as Table1.The economic efficiency brought by the continuous advancement of Moore's Law has

reached a bottleneck. Moore's Law refers to the fact that as technology evolves, the number of transistors housed on a chip will grow exponentially, doubling every 1.5-2 years, with the effect of doubling chip performance or halving cost. In semiconductor manufacturing, the continuous miniaturization of process steps leads to transistor density approaching its limits, along with serious problems of leakage, heat generation and power consumption due to the short channel channel effect. At higher process nodes, each process node increase brings a non-linear increase in cost, and the change in technology node is gradually slowing down against the background of a significant increase in capital expenditure.

From the perspective of technological development, advanced packaging tends to be functionally diversified: the packaging object from the initial single die to multi-die development, a package may have a variety of different functions under the die; connection diversification: the internal interconnection technology under the package continues to diversify from bumping (Bumping) to embedded interconnections, the density of the connection continues to improve; stacking diversification: the arrangement of devices has been gradually from the plane to the three-dimensional In addition, the stacking technology is diversified: the device arrangement has gradually moved from planar to three-dimensional, and rich stacking topologies are constructed by combining different interconnection methods. The development of advanced packaging technology extends and expands the concept of packaging, from the wafer to the system can be used to "package" to describe the integrated processing.

Conventional packaging methods typically involve a process of dicing wafers into individual chips and packaging them. The main types of packages include single in-line packages (SIP), dual in-line packages (DIP), small outer shell packages (SOP), small transistor outer shell packages (SOT), and transistor outer shell packages (TO), etc. However, as semiconductor technology continues to evolve and enter the "post-Moore era," semiconductor manufacturers have shifted their focus away from wafer process technology. However, as semiconductor technology continues to evolve and enter the "post-Moore era," semiconductor manufacturers have shifted their focus from wafer process technology enhancements to system-level design and innovative packaging technologies. As a result, cutting-edge packaging technologies have made great strides. This innovative packaging refers to novel packaging forms and technologies. Currently, flip chip (FC) structure packaging, wafer-level packaging (WLP), system-in-package (SiP), 2.5D packaging, and 3D packaging are all considered to belong to the field of innovative packaging technologies. [5]

3. Drivers of Advanced Packaging Development

3.1. Big Computing Applications Drive Advanced Packaging Development

High-end packaging processes are becoming increasingly important in the post-Moore's Law era as high-computing applications such as high-performance servers (HPC) and autonomous driving (ADAS) replace cell phones and personal computers as the new drivers of the semiconductor industry. Looking at TSMC's downstream applications, the revenue growth rate of high-performance computing has outpaced that of cell phones since the third quarter of 2020 and will become TSMC's largest application area in the first quarter of 2022, while in comparison, electronic devices with high arithmetic power accounted for only 16% of the total output value of the packaging and testing vendor. This paper argues that as the demand for high computing power rises, advanced packaging technology instead of advanced processes has become the preferred solution to reduce the cost per unit of computing power, and this will also increase the share of computing electronics in the value volume contribution of the packaging and testing vendors.

3.2. Market Generates New Demand for Advanced Packaging

Advanced integrated packaging in the post-Moore era is reshaping the product supply chain and value chain, and is also affecting the industry form and competitive landscape. According to Yole data, the share of advanced packaging in the global packaging market has increased from 39% in

2015 to 44% in 2021. It is expected that by 2027, the share of the advanced packaging market will increase to 53%, with a size of about $65.1 billion, and the 2021-2027 CAGR is about 9.6%. Taking Intel Lakefield microprocessor as an example, the TSV process, Chip-on-Wafer, etc. of IC chips are completed by Intel, and these links become the most critical part of the technology chain, accounting for a relatively large proportion of the product cost and high value-added [6].

4. Global Companies Competing for Packaging Industry

4.1. TSMC

TSMC, as an industry leader, established a specialized wire and packaging technology integration department to develop packaging technology as early as the end of 2008. After more than a decade of technology research and development, TSMC has accumulated a variety of advanced packaging technologies and announced the launch of the 3D FabricTM brand in 2020 to further integrate the company's process technology and packaging technology. 3D FabricTM consists of the front-end System-on-Chip technology (In 2021, TSMC has launched its new advanced packaging technology for the data center market, COUPE (Compact Universal Photonic Engine). Engine heterogeneous integration technology for the data center market [7]. COUPE offers superior electrical interface performance with 85% lower parasitic capacitance than uBump and 51% lower PDN impedance. In terms of power consumption and speed, COUPE consumes 30% less power than ubump at the same rate; at the same power, COUPE's speed is 170% of ubump. If this technology is successfully launched, it will greatly reduce the power consumption of data center chips and increase the transmission speed to cope with the explosive growth of network traffic [8].

4.2. Three Stars

Due to TSMC's leading edge in CoWoS technology, Samsung has missed out on chip foundry orders from giants such as NVIDIA and Apple on the mainland in recent years, and the gap between its market share and TSMC's has been widening. In order to reverse the backward situation of the company's packaging technology, Samsung continued to make efforts to launch three major advanced packaging technologies, I-Cube, H-Cube and X-Cube. 2018 Samsung launched the first I-Cube2 program, enabling it to stand firm in the field of advanced packaging. This was followed in 2020 by the introduction of a 3D stacked design with the X-Cube solution. In November 2021, Samsung announced that it had co-developed the Hybrid Substrate Cube (H-Cube) technology with Amkor Technology, which is its latest 2.5D packaging solution. [9] Samsung is also the world's first to introduce the 3nm GAA process to mass production lines in 2022. The company has formed an Advanced Packaging (AVP) business team within its semiconductor business unit to accelerate research and development (R&D) for next-generation semiconductor post-processing. By 2027, Samsung plans to mass-produce the 1.4nm process on schedule. In the first quarter of 2023, global foundry market share expanded slightly from the previous quarter, with Samsung Electronics at 12.4%.

4.3. Intel

Similar to TSMC, Intel has also been laying out in the field of advanced packaging for many years, and has successively launched advanced packaging technologies such as EMIB, Foveros, and Co-EMIB, etc. Its EMIB and Foveros technologies are benchmarked against TSMC's CoWoS and InFO technologies respectively, but the mass production times of the relevant products are lagging behind those of TSMC. At the recent CES2019, Intel focused on displaying a new generation of CPU products packaged with "Foveros" technology." Foveros, Intel's latest 3D packaging technology, enables 3D stacking on logic chips, integrating chips with different processes, structures, and uses, providing designers with greater flexibility [10]. Designers can also use Foveros to create a new generation of CPUs, which can be packaged on a logic chip. [10] Designers can "mix and match" different IC modules, I/O configurations, and enable products to be broken down into smaller "chip

combinations" in new product forms. Intel announced the industry's first glass substrate solution for next-generation advanced packaging in 2023. Intel notes that glass substrates can withstand higher temperatures, have 50% less pattern distortion, and have the dimensional stability needed for extremely tight interlayer interconnect coverage [11].

5. Conclusion

By studying the development trend of advanced packaging technology and leading enterprises in the industry, this paper finds that it is more difficult to break through the process technology in the "Post-Moore Era", and the process technology is subject to the significant increase in cost and technical barriers and other factors such as the slowdown in the rate of improvement. As the integrated circuit process technology is difficult to break through in the short term, through advanced packaging technology to enhance the overall performance of the chip has become the integrated circuit industry technology trends. Semiconductor products from two-dimensional to three-dimensional development, from the direction of technological development of semiconductor products appeared in the system level packaging (SiP) and other new packaging methods, the purpose of which is to minimize the packaging area. Therefore, with Moore's Law out of speed, the cost of advanced processes is rapidly increasing, advanced packaging will become the main growth point of the future packaging and testing market. The development focus of some foundries is shifting from the pursuit of more advanced nano-processes in the past to innovation in packaging technology.

The main contribution of this paper is to explore the new trends in the development of advanced packaging industry, which is helpful to help enterprises and scholars understand the technological development and trends of advanced packaging industry. The current study still has insufficient survey samples, and future studies should expand the scope of the survey.

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