Analysis Of 4-Bit Absolute Value Detector for ECG Signal Comparation

Hao Li [*]

Department of HDU-ITMO Joint Institute, Hangzhou Dianzi University, Hangzhou, 310018, China

* Corresponding Author Email: 631401120123@mails.cqjtu.edu.cn

Abstract. In the present era, where numerous heart conditions are prevalent, the significance of monitoring cardiac electrical signals has surged within the medical realm. Within this study, we leverage Complementary Metal Oxide Semiconductor (CMOS) and Pass-transistor Logic (PTL) methodologies for crafting and refining a 4-bit absolute value detection mechanism. This mechanism serves to identify and juxtapose electrocardiogram (ECG) signals. The 4-bit absolute value detection system is bifurcated into two core segments: one for absolute value identification and the other for comparative analysis. This setup facilitates a binary input's comparison with a predetermined threshold, thereby yielding a corresponding comparative outcome. Subsequently, a meticulous assessment is conducted on the lengthiest pathway, which is then subject to refinement through gate sizing and voltage supply (Vdd) adjustments. The findings unveil a delay of $34.13t_{p0}$ and an energy dissipation of 184.832 C. The resultant 4-bit absolute value detection mechanism, borne from this research institution's efforts, emerges as an invaluable asset in the medical domain, attributed to its exceptional optimization with respect to minimal delay and energy outlay.

Keywords: ECG; CMOS and PTL; 4-bit absolute value detector.

1. Introduction

An electrocardiogram is a process that people use to record electrical signals associated with heart activity during a specific period of time. It has been widely accepted over the past 70 years and has become an important part of medical evaluation. [1]. Electrocardiograms are used to diagnose and treat different types of heart disease, like myocardial infarction and arrhythmia [2]. In order to better understand the patient's situation, people often analyze its time domain characteristics and electrical characteristics, and carry out A series of processing on the ECG signal, such as filtering and noise reduction, amplification, A/D conversion and so on [3, 4]. When processing signals, it is often necessary to compare the encoded binary ECG signals with specific ECG signals [5]. In this case, an absolute value comparator is very important.

This study employs CMOS and PTL techniques for the purpose of crafting and refining a 4-bit absolute value detection mechanism aimed at facilitating the comparison of ECG signals. The 4-bit absolute value detector is bifurcated into distinct segments: the half-adder and the comparator. In cases where the input signal adopts a 4-bit binary format, the absolute value detection module discerns its polarity, while the comparator module undertakes a comparison between the resultant output and a predefined threshold. Ultimately, the outcome is determined and generated. Following the initial functional implementation, the research proceeds to identify the lengthiest pathway, subsequently leveraging gate sizing and Vdd scaling to optimize the delay and energy consumption within the constructed circuitry. This endeavor culminates in a successful reduction of both delay and energy usage within the circuit, consequently leading to error mitigation during the process of ECG signal detection and comparison. This outcome contributes to achieving heightened precision in the results yielded by the detection and comparison of ECG signals.

2. The basis of ECG signal processing

2.1. Generation mechanism of ECG signal

ECG is a comprehensive reflection of the electrical activity of numerous cardiomyocytes, and the generation of ECG is closely related to the depolarization and repolarization of cardiomyocytes [6]. In the resting stage, Cardiomyocytes carry a positive charge outside the cell membrane. At the same time, there is an equal amount of negative charge inside the cell membrane. This state of charge distribution is called the polarization state. In this case, the potential difference of cardiomyocytes remains constant, which is called the resting potential. When one side of the myocardial cell membrane is stimulated above the threshold value, the permeability of potassium, ionizing and chlorine plasma changes, which causes the movement of ions inside and outside the cell membrane. The resting potential of the outside negative and the inside positive reverses the membrane potential of the excited part. This change process is called depolarization, but due to the instantaneous change of the resting potential, the membrane potential will soon return to the standard resting potential, which is called repolarization. The ECG signal is to complete the process of depolarization and repolarization, which can be analyzed by collecting the potential difference of the human body surface through the electrode sheet.

2.2. Characteristics of ECG signal

The characteristics of ECG signals generally include time domain characteristics and electrical characteristics. In this part, this paper will analyze the time domain characteristics and electrical characteristics of the ECG signal [7]. The ECG signals depicted in Figure 1 exhibit distinctive temporal features, comprising sequences of waveform clusters. Each cluster captures variations in the ECG signal at distinct stages, with individual wave points offering detailed descriptions as follows: 1. P wave: Serving as the initial deflection, this is referred to as the P wave. It encapsulates alterations in atrial depolarization potentials, signifying the depolarization of both atria. 2. QRS wave group: This set of waves, marked by a prominent peak, mirrors the potential shifts during ventricular activation. It elucidates the potential fluctuations within the ventricular muscle depolarization process. 3. PR interval: Spanning from the commencement of the P wave to the initiation of the QRS complex, this interval signifies the temporal lapse between atrial muscle depolarization inception and ventricular muscle depolarization onset. 4. T segment: Positioned post the QRS wave group and preceding the T wave, this phase presents as a horizontal line. It signifies the timeframe amid full depolarization of the left and right ventricles, transitioning into the initiation of repolarization. 5. T wave: This waveform represents the potential modifications attributed to the ventricular muscle repolarization process. The temporal attributes of the ECG signal's waveform are visually depicted in Figure 1.

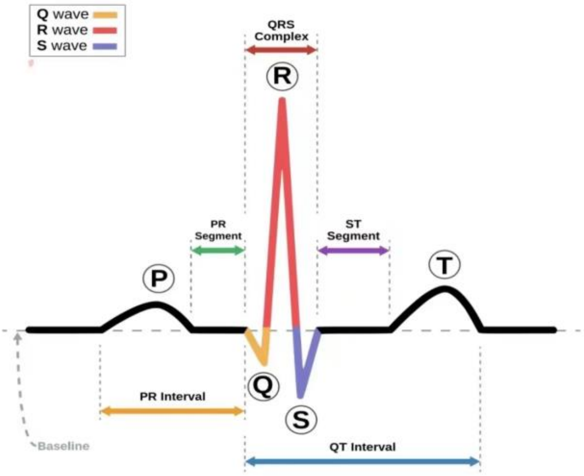


Fig. 1 Time domain characteristics of the ECG [6]

The electrical attributes inherent in ECG signals can be succinctly categorized into four aspects: fragility, volatility, low-frequency nature, and stochasticity. Owing to the ECG signal's low-frequency nature and substantial direct current (DC) component, a considerable portion of its spectrum exhibits pronounced concentration, primarily within the range of approximately 0.25-35Hz. The ECG signals are subject to multifarious influences stemming from diverse factors, encompassing human physiological condition, measurement procedures, and interindividual disparities.

2.3. ECG signal processing flow

After obtaining the original ECG signal, the ECG signal must be preprocessed first. The pre-processing of ECG signal is mainly denoising and filtering to improve the signal-to-noise ratio and reduce interference [8]. Denoising can be considered from the amplitude and frequency of the signal. Filtering can be divided into two types, low pass filtering and band-pass filtering. low-pass filtering can eliminate high-frequency noise, and band-pass filtering can filter specific frequency signals. After that, this paper needs to amplify the pre-processed ECG signals [9]. The purpose and significance of ECG signal amplification is to effectively filter out high-frequency signals that have nothing to do with ECG signals. Since this paper need to display the ECG signal on the computer monitor, it is impossible to do so with analog signals, so A/D conversion is required to convert analog signals to digital signals [10]. In the A/D conversion process, there are four steps. First, a sampling circuit needs to be designed for sampling, and then the sampling circuit needs to go into hold mode before the real conversion begins. Then the collected signal needs to be quantized, and the role of ADC is to divide this analog quantity into many small quantities to form the digital quantity. Finally, this paper encodes it to get the binary number this paper need. The ECG signal processing flow is shown by figure 2. below.

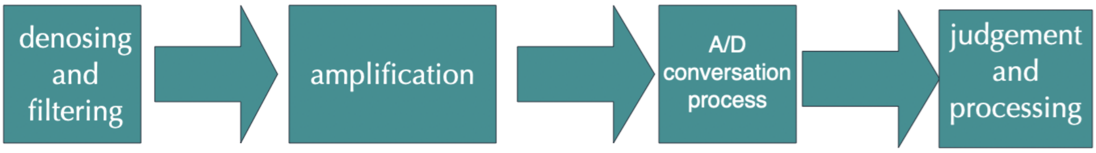


Fig. 2 ECG signal processing flow (Photo/Picture credit: Original)

3. Design of 4-bit absolute value detector

In the process of ECG processing, people often need to compare the size of the obtained binary signal with the existing data to determine whether the detected person's heart rate is normal. So how do people compare the absolute values of two signals? Obviously, researchers often need to design a comparator at this time, and this comparator is generally multi-digit. In this study, due to the limited time, this paper designs and optimizes a 4-bit absolute value detector. At the same time, this paper fixed the comparison threshold, whose binary is 011. The truth table of the whole circuit is shown in table 1 below.

Table 1. The truth table.

A3	A2	A1	A0	B2	B1	B0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1
1	1	0	0	1	0	0	1
1	1	0	1	0	1	1	0
1	1	1	0	0	1	0	0
1	1	1	1	0	0	1	0

This section covers how to build a 4-bit absolute value detector. The whole circuit consists of two modules, the absolute value acquisition module, and the comparison module. This paper uses half-adder to obtain the absolute value, while the comparator is used to compare the obtained number with the given number. In each section, this paper breaks down the entire circuit into different modules, explain how to implement this function through algorithms and carry out basic design optimization. The whole circuit idea is shown by figure 3 below.

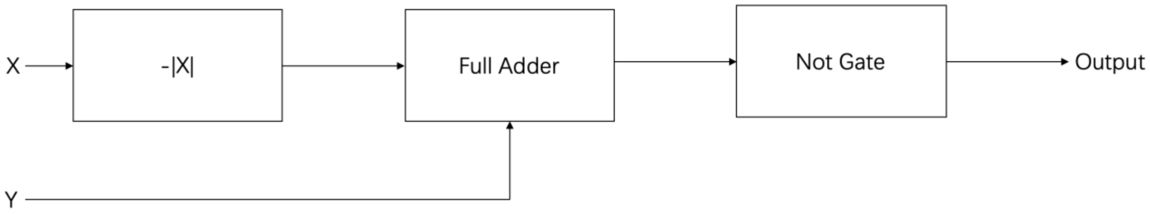


Fig. 3 The whole circuit idea (Photo/Picture credit: Original)

3.1. Half-adder

In this study, this paper assume that the input is a 4-bit binary number, A3, A2, A1, and A0. In the first module, unlike the traditional way of thinking, this paper wants to get the opposite of the absolute value, since it is convenient for later comparison. Through the truth table, it can be found that there are two cases at this time, when A3 (MSB) is 1, indicating that it is a negative number, then the remaining three digits do not need to change; If A3 (MSB) is 0, it is a positive number, then this paper need to invert the remaining three digits and add 1. The half-adder is shown in figure 4.

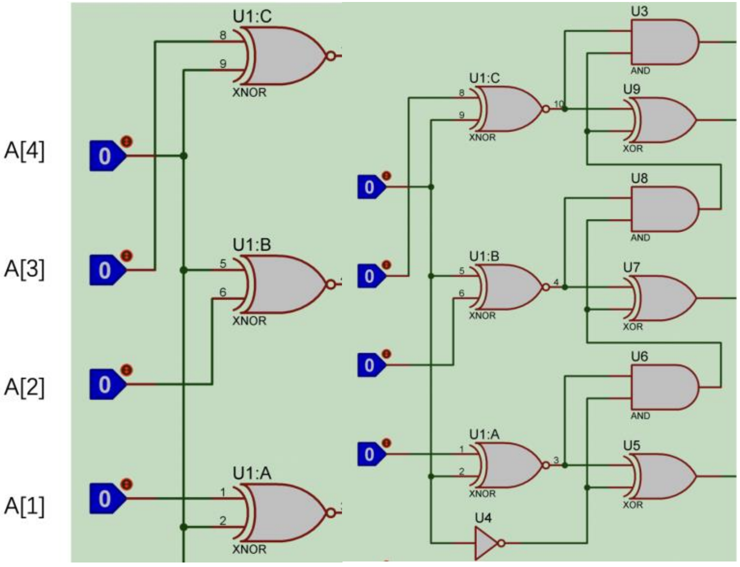


Fig. 4 Structure of the half-adder (Photo/Picture credit: Original)

3.2. Comparator

In the comparator module, this paper design a comparator based on subtractor. Compare by subtracting the input value X from the given comparison value Y. In the case of 3-digit subtraction, the highest digit of the result is actually 4 digits. When the highest digit of the result is 1, X is greater than or equal to Y; When the highest digit of the result is 0, X is less than Y. To make the result clearer, this paper uses an inverter to invert this, allowing Y to be subtracted from X, and comparing the sizes according to the highest bit of the result. The comparator is shown by figure 5.

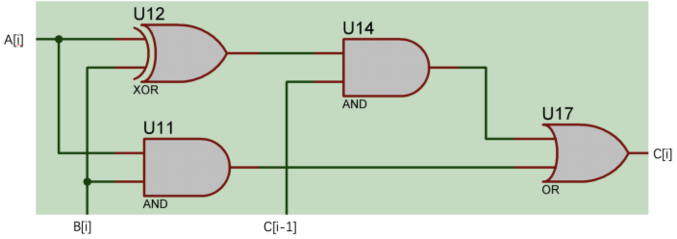


Fig. 5 Structure of the comparator (Photo/Picture credit: Original)

3.3. 4-bit absolute value detector

After analyzing each module individually and what it does, this paper put it all together. The final circuit structure is shown in the figure 6.

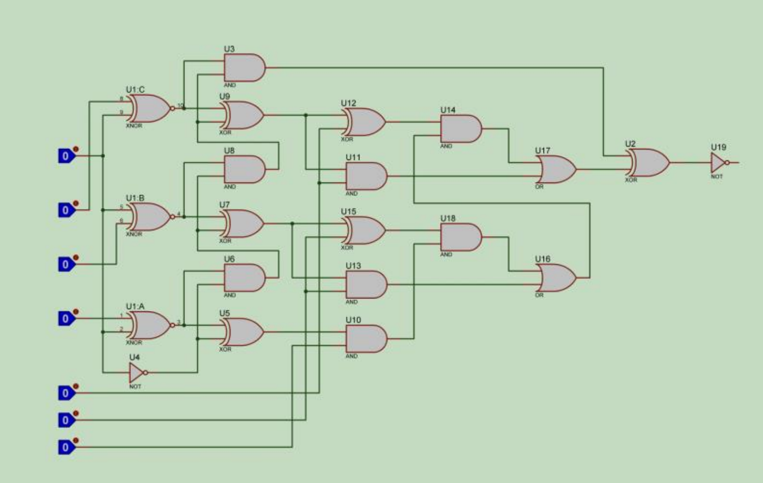


Fig. 6 Structure of the whole circuit (Photo/Picture credit: Original)

4. Critical path analysis

When detecting the ECG signal, there is often some delay and energy loss due to components, power supply voltage, and other reasons. Therefore, this paper carried out some optimization of the designed 4-digit absolute values, including gate sizing, and Vdd scaling, and calculated the final delay and energy.

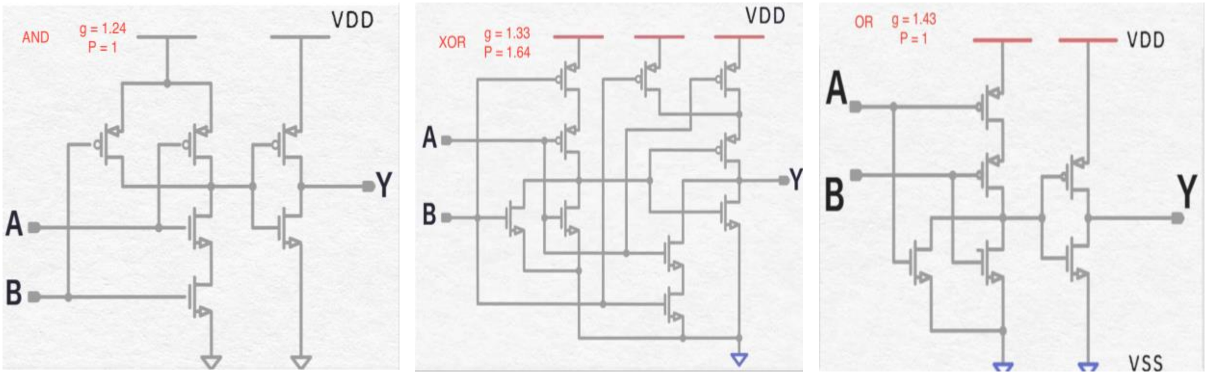
In this section, this paper chooses the longest path to analyze it. In the entire circuit, the longest path has the highest delay and the greatest energy loss, so choosing the longest path for analysis can represent the highest delay and the greatest energy loss of the entire circuit. As shown in the Figure. 6, this path first goes through the carry operation in the adder, then compares with the given number in the comparator, and finally outputs the result. The critical path is shown by figure 7 below.

Fig. 7 The critical path (Photo/Picture credit: Original)

4.1. Gate sizing

As mentioned earlier, this paper has constructed the structure of the entire 4-bit absolute value comparator in this study using logic gates. However, in the process of calculating the delay, this paper needs to calculate the parameters related to each logical gate, such as logical effort (*g*) and parasitical effort (*p*).

First, this paper uses NMOS and PMOS to build the logic gates used in the previous circuit, including inverters, AND gates, OR gates, and XOR gates. It is worth noting that in order to reduce the use of components, this paper have replaced the XNOR gate with an XOR gate and an inverter. For the MOS tube used here, the Unit-sized inverter is $Lp = Ln = 100\text{nm}$, $Wp = 650\text{nm}$, $Wn = 430\text{nm}$. The schematic diagrams of each logic gate are shown in figure 8 below in which figure 8(a) is the AND gate, figure 8(b) is the XOR gate, and figure 8(c) is the OR gate.



(a) (b) (c)

Fig. 8 The schematic diagrams of each logic gate (Photo/Picture credit: Original)

Then, by finding the reference model corresponding to each logic gate, this paper calculated *g* and *p* respectively through the formula.

$$g = \frac{R_{gate}\times C_{in,gate}}{R_{INV}\times C_{in,INV}} \tag{1}$$

$$p = \frac{C_{par,gate}}{C_{par,INV}} \tag{2}$$

Where *g* means logic effort, *p* means parasitical effort

4.2. Vdd scaling

Gate sizing is not the only factor affecting circuit delay, supply voltage (*Vdd*) is also important. According to the principle of charge and discharge of a capacitor, an expression of delay about *Vdd* can be obtained by deducing some basic formulas.

$$Delay = \frac{C \times V_{dd}}{\beta \times (V_{dd} - V_T)^2} \tag{3}$$

Where C and β are the correlation parameters; The value of V_T is 0.2v, which represents the threshold voltage. By using this formula, this paper first finds the maximum delay by treating *Vdd* as 1v. This paper then increases the maximum delay by a factor of 1.5, corresponding to which this paper finds an optimal *Vdd* of 0.76v.

4.3. Optimization of delay and energy

This paper uses the logic effort method to calculate the delay and energy. Logic effort is used to describe the properties of different kinds of logic gates and how they interact with each other in a specific logic chain, and to provide techniques for minimizing delay. There are the formulas.

$$\mathrm{G} = \prod gi \tag{4}$$

$$\mathrm{B} = \prod bi \tag{5}$$

$$\mathrm{H} = \frac{Cin}{Cout} \tag{6}$$

$$\mathrm{F} = \mathrm{G} \times \mathrm{H} \times \mathrm{B} \tag{7}$$

$$\mathrm{f} = \sqrt[N]{F} \tag{8}$$

$$Delay = \sum_{i=1}^{N} pi + Nf \tag{9}$$

Where *G* refers to the overall logical effort; *B* is the branching effort; *H* is the overall electrical fanout; f refers to the optimal stage effort.

This paper has calculated the *g* and *p* of the various logic gates in the above section. In the selected critical path, there are total 10 stages, so *N* equals to 10. At the same time, there are four branches, which can be obtained *B*=16. *H* is equal to *Cout*/*Cin,* and in this path, this paper gets 16. Finally, by bringing all of our known parameters above into the given formula, this paper find that delay is equal to 34.14.

In the energy part, this paper first calculates the delay corresponding to the maximum energy this paper can achieve, and then substitute the circuit delay 34.133 (which has been derived when calculating the delay) into the formula to get the corresponding *Vdd*, and then substitute into the energy formula to get the energy 306. On this basis, the optimized circuit is obtained by multiplying the delay after expansion by 1.5 times, and the minimum energy required is 184.832 calculated by the formula. This paper found that lower delay is always associated with higher power consumption.

5. Conclusion

In this project, this paper successfully uses CMOS and PTL technology to design and optimize a 4-bit absolute value detector. In the process of circuit design, in the first part of this paper, this paper uses a half adder to obtain the absolute value detection and uses an XOR gate and an inverter replace the XNOR gate. In the comparison part, this paper uses a comparator based on subtractor. Compared to traditional comparators, this method can reduce the number of components to achieve less latency and energy loss. In the process of circuit optimization, this paper selects the longest path for analysis. First, this paper uses a 650nm width PMOS and a 430nm width NMOS for gate sizing. Then, according to the functional relationship between delay and supply voltage, the supply voltage is selected as 0.76v, and the delay is 34.13tp0 and the energy loss is 184.832C. Although this study successfully designed and optimized a 4-bit absolute value detector, it is completely insufficient in the field of ECG detection and analysis. In the future, the first thing this paper needs to do is to scale up. Because in real life, the input ECG signal is often more than 4 digits, there may be more digits. Therefore, this paper needs to optimize the input part so that it can detect more signals. Second, only CMOS and PTL technologies are used in this study, and then other more complex and optimized technologies need to be included in this paper to achieve less delay and energy loss.

References

[1] Zhaoyang P, Xueyan H, Man C, et al. Short-term exposure to ozone and ECG abnormalities in China: A nationwide longitudinal study. Journal of Hazardous Materials, 2023, 459.

[2] Su Guanli, Liu Gang, Zheng Mingqi et al. The diagnostic and prognostic value of repolarization abnormal electrocardiogram findings in coronary heart disease. Journal of Practical Electrocardiology, 2015, 24(04): 261-266.

[3] M A,Deepa. Comparison between CMOS full adder and PTL full adder. IOP Conference Series: Materials Science and Engineering, 2021, 1065(1).

[4] Liu Chunjuan, Xu Xiaorui, Yang Chaoshan. CMOS semi-adder circuit Robustness Design. Journal of Lanzhou Jiaotong University, 2016, 35(03): 68-71.

[5] Li Wenshi, Tang Pushan, Xu Qi 'an, et al. Analysis and Simulation of Time Delay Optimization for Integrated Circuits. Microelectronics, 2004, (06): 655-657+662.

[6] Zhang J W. Study on recognition of morphological characteristics of electrocardiogram and its role in classification. East China Normal University, 2011.

[7] Yang Xudong. Research on extraction of ECG signal feature parameters based on Wavelet transform. University of electronic science and technology, 2020.

[8] QIN Fangjun, Xu Jiangning, Li An et al. Accelerometer signal noise reduction based on new adaptive Kalman filter. Data Acquisition and Processing, 2009, 24(02): 227-231.

[9] Shruti J,Sudip P. Design of filters using current amplifiers for removal of noises from ECG signal. Procedia Computer Science, 2023, 218.

[10] Canon Kabushiki Kaisha: Patent Issued for Imaging Apparatus and Imaging System for Performing Ad Conversion on Signal Output from Pixels (USPTO 10015421). Journal of Engineering, 2018.