

Designing a Low-Power Single Stage Neural Amplifier for Efficient Wireless Neural Recording Systems

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Abstract. In the realm of upcoming neural recording systems, the demand for simultaneous monitoring of a substantial range of 100 to 1000 neurons within fully implanted devices has intensified. Accommodating such requirements calls for integrated electronics that exhibit low power consumption, minimal noise, reduced data rate, and compact size to facilitate their widespread implantation. Central to these characteristics is the amplification circuit of the neural recording system, as it plays a pivotal role in determining power consumption, bandwidth, noise output, and overall system size. This article proposes a novel design of a single-stage neural amplifier, incorporating an operational transconductance amplifier as the primary functional unit, alongside a peripheral circuit comprising MOS bipolar pseudo-resistors and capacitors to ensure stable feedback. Moreover, to enhance signal quality and attenuate noise, a more intricate circuit, building upon the previous system, is introduced. The core section of this system demonstrates impressive performance metrics, achieving a power consumption of less than $9\mu\text{W}$, an amplification rate exceeding 80 dB, and a cutoff frequency of 3kHz. The architecture's performance can be further augmented by the more complex circuitry if necessitated by specific application demands.

Keywords: neural recording systems, operational transconductance amplifier, bipolar pseudo-resistor

1. Introduction

Neural activities in vivo are conducted through the means of altering potentials. The typical values of human neural potential are -70mV under stasis and 40mV under activity. The potential difference is about 110mV . Such difference is consistent for one specific subject, thus can be treated as a digital signal with little processing. The ideal approach is to directly acquire the active potential. However, due to the complicity of the CNS and the limit of current electrode process, such direct acquirement is not feasible. Based on the mechanism of the neural activity, relevant signals other than merely active potential are being observed and recorded. The Amplitude and frequency characteristics of electroencephalogram (EEG), electrocardiogram (ECG), electromyogram (EMG), local field potential (LFP) and neural spikes.

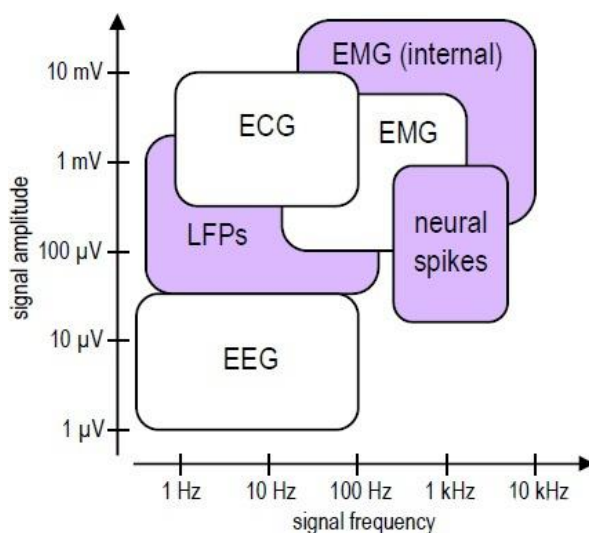


Fig. 1 Amplitude and frequency characteristics [1]

The most important in vivo neurophysiological signals are EEG, EMG collected on the surface of the scalp, LFPs collected in the brain. These signals differ in characteristics, such as amplitude and frequency band. The electrodes used to acquire them differ in properties, such as impedance, polarization voltages. Requirements of accuracy for these signals differ in noise levels and time domain features. Further requirements of power consumption shall be met under the circumstance which the electrodes are to be planted insidiously.

Through the amplitude and frequency characteristics shown in Fig.1, some of the most basic performance requirements of an acquisition system can be obtained: 1-dynamic range (maximum amplitude/minimum resolution); 2-bandwidth; 3-sampling rate requirements.

In terms of amplitude and frequency range, the EEG is the weakest of the neurophysiological signals in the body, only 10uV in this order of magnitude, giving the need for high amplification and noise rejection capability, but its frequency bandwidth is only 100Hz, so it does not require a very high pass band, and the dynamic range requirements are not very strict, the upper limit only needs to reach a few tens of uV. LFP and spikes are generally collected with electrodes implanted in the brain, and LFP fluctuations may be of the order of 2mV, while spikes may be as small as 30uV, so a large enough dynamic range is required for the amplifier. Also, a flat frequency response and high sampling speed (typically 30kHz) is required for the frequency range from <1Hz to around 5kHz. Emphasis should be laid in accordance with the specific neural signals captured while designing an amplifier. Since LFPs can convey information of the brain neuron activities more directly and accurately, neural recording systems concerning LFPs are more common in recent advances. The following parts of this article will elaborate some kinds of LFP signal recording systems, especially their amplifying system.

2. Single Stage Neural Amplifier

Fig.2 shows the schematic of this design. This circuit was first described in [2]. The mid-band gain A_M can be calculated as C_1/C_2 . Given that C_1, C_L is far greater than C_2 , the bandwidth can be approximated as $g_m/(C_L * A_M)$.

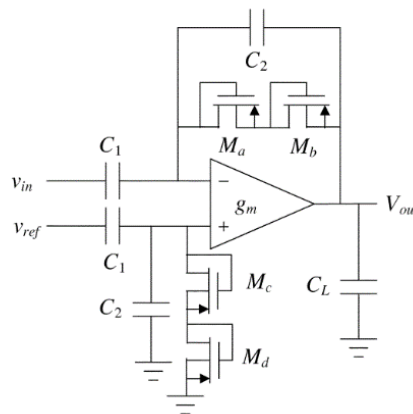


Fig. 2 System schematic with simplified Operational Transconductance Amplifier (OTA) [2]

2.1. Peripheral Part

The peripheral part of this system consists of capacitors C_1 , C_2 , C_L and MOS-Bipolar Pseudo-resistor Elements(M_{a-d}). The main purpose of the capacitors are to provide feedback to construct a closed loop.

Transistor M_{a-d} are MOSFETs acting as pseudo-resistors. With negative gate-to-source voltage, each device can be treated as a diode connected transistor working in forward biasing. For a device level of view, the parasitic p-n-p bipolar junction can work in forward active region, and it has the behavior like a diode-connected BJT [3]. The size of the transistors are set as $4\mu\text{m} \times 4\mu\text{m}$. Their I-V curve is elaborated in Fig.3. The resistance under different voltages is plotted as Fig.4. For ΔV ranged

from -0.2V to 0.2V, it is nearly impossible to obtain a precise resistance value because of the limit of the current measuring approaches.

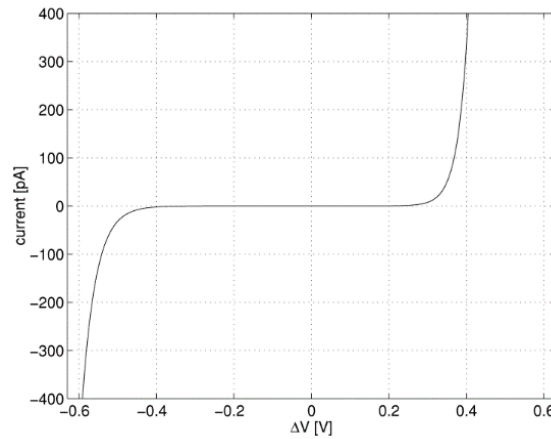


Fig. 3 Characteristic curve of the MOS-bipolar devices.[4]

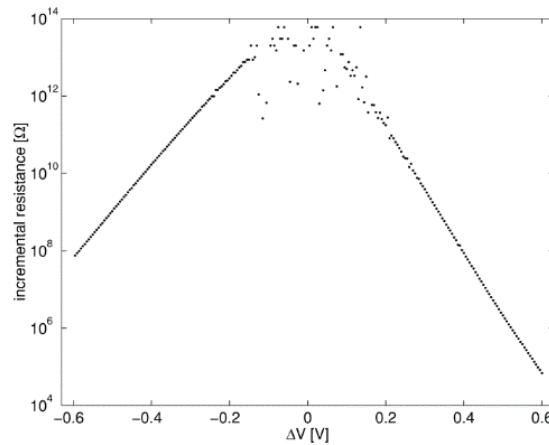


Fig. 4 Incremental resistance of the MOS-bipolar devices [4]

To reduce the distortion caused by large output signals, two pseudo-resistors are connected in series. The cutoff frequency ω_L of the amplifier is given by:

$$\omega_L = \frac{1}{2 \cdot C_2 \cdot r_{MOS}} \quad (1)$$

Utilizing an extended time constant, the system responds to substantial input shifts, generating a significant voltage across MOS-bipolar components, thereby reducing their incremental resistance and facilitating rapid settling. This approach effectively approximates large-valued resistors, necessitating supplementary biasing circuitry for implementation. Alternatively, another design adopts diode-connected NMOS transistors to serve as pseudo-resistors, enabling the attainment of an equivalent resistance exceeding $10^{10}\Omega$. However, the specific configuration of connecting the body and source for implementing a diode-connected bipolar transistor remains ambiguous [5].

2.2. Low Noise Low Power OTA Design

In the amplifier design, Fig. 5 depicts the schematic of the two-stage OTA utilized. Common circuits were responsible for providing the bias current and supply voltage [6]. For the sake of universality, the power consumption of these circuits was excluded from the power calculations.

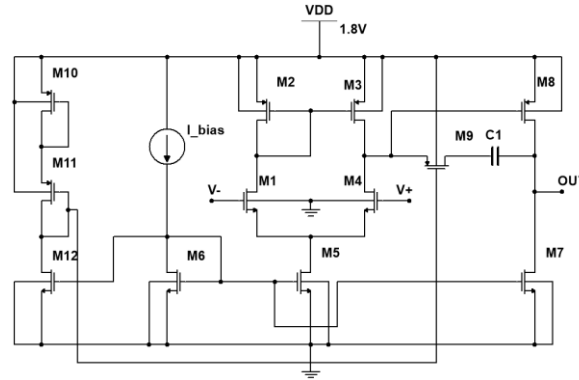


Fig. 5 Design schematic of the OTA (Photo/Picture credit: Original)

For the overall amplifier gain, the gain of the first stage can be derived as:

$$A_1 = -g_{m4} \cdot (r_{o4} // r_{o3}) \quad (2)$$

The gain of the second stage can be derived as:

$$A_2 = -g_{m8} \cdot (r_{o8} // r_{o7}) \quad (3)$$

Thus, the expression of overall gain A_v is:

$$A_v = g_{m4} \cdot g_{m8} \cdot (r_{o4} // r_{o3}) \cdot (r_{o8} // r_{o7}) \quad (4)$$

Sizing of each transistor is required to meet the designed parameters to achieve a low-noise low-power behavior. The bias current is set to $1\mu\text{A}$ and is copied by the current mirror to each stage and biasing circuit. The first stage is designed to take $2\mu\text{A}$. The second stage and the biasing circuit on the left part is designed to take $1\mu\text{A}$. The design parameters and operating points of transistors in the circuit are shown in Table 1.

Table 1. Component Parameters of M_{1-4} , M_8

	W/L($\mu\text{m}/\mu\text{m}$)	$I_D(\mu\text{A})$	$g_m(\mu\text{S})$	$V_{ov}(\text{V})$
$M_{1,4}$	1.2/5	0.97	10.67	0.156
$M_{2,3}$	20/5	0.97	16.75	0.068
M_8	10/2	1.05	18.61	0.068

The input NMOS M_1 and M_4 are designed to be identical in sizes. Their transconductance are denoted as $g_{m1,4}$ and their aspect ratio as $(W/L)_{1,4}$. Transistors $M_{2,3}$ are of the same size $(W/L)_{2,3}$ and transconductance $g_{m2,3}$. The size and transconductance of the current mirror transistors $M_{5-7,12}$ are denoted separated in Table 2.

Table 2. Component Parameters Of Current Mirror

	W/L($\mu\text{m}/\mu\text{m}$)	$I_D(\mu\text{A})$
M_6	2.2/1.8	1
M_5	6.6/1.8	1.94
M_7	2.2/1.8	1.05
M_{12}	2.2/1.8	1.05

The right half plane zero in the frequency response will cause a -90 degrees phase shift, causing a serious decrease in phase margin. Thus, the zero should be cancelled or be shifted to the left half plane. A resistor R_z in series with the compensation capacitor can be applied to relocate zero. This will cause one extra pole to appear, but for an adequate resistance, this third zero will be at an extremely high frequency so that the performance of the circuit will not be affected. This zero can be expressed as:

$$\omega_z \approx \frac{1}{C_1 \cdot (g_{m8}^{-1} - R_z)} \quad (5)$$

Thus, the shift in zero position can cancel the first nondominant pole if R_z gets the value:

$$R_z = \frac{C_L + C_1}{g_{m9} \cdot C_1} \quad (6)$$

Where C_L stands for the load capacitance.

To implement R_z , a transistor working in triode region is adopted. The aspect ratio of this transistor can be calculated as:

$$\left(\frac{W}{L}\right)_9 = \sqrt{\left(\frac{W}{L}\right)_{11} \left(\frac{W}{L}\right)_8} \cdot \sqrt{\frac{I_{D11}}{I_{D8}}} \cdot \frac{C_C}{C_C + C_L} \quad (7)$$

Where $I_{D8,11}$ stands for the drain current of the MOSFET concerned. This design has less implementation difficulty compared to the one using resistor, and further can ensure that the zero tracks the first nondominant pole as process, voltage, and temperature change.

The simulation result of the circuit is shown below in fig.6 as bode plot. The simulation process is done with Cadence Virtuoso 6.1.5. The technology used is smic18mmrf. The open-loop gain of this OTA is 80.96 dB. The Gain Bandwidth is 16.6 MHz. Phase margin is 42.3 degrees.

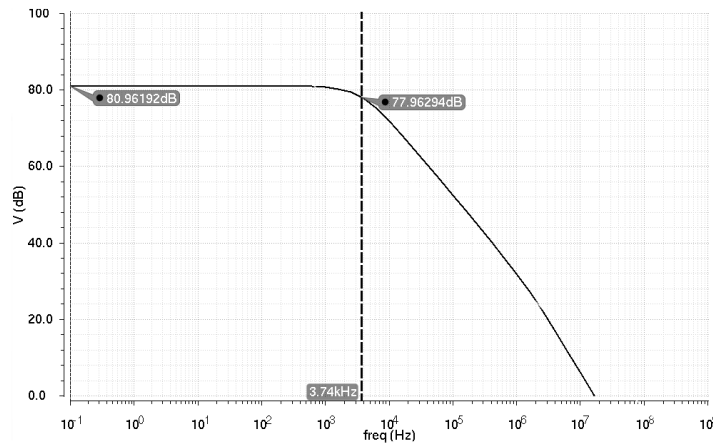


Fig. 6 Simulation result in bode plot (Photo/Picture credit: Original)

The presence of flicker noise is a significant concern for evaluating a low-noise circuit. Devices with large gate areas can be applied to reduce its effect on the overall performance of the system. To minimize the impact of flicker noise, all devices used in the design should have the maximum size possible. However, as devices M_{1-4} are made larger, C_2 increase, resulting in a lower phase margin. Also, as the sizes of $M_{1,4}$ go up, the input capacitance of the OTA C_{in} will increase.

The noise referred to input of the overall amplify system can have the relationship with the noise referred to input of the OTA as:

$$\overline{V_{n,amp}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 * \overline{V_{ni}^2} \quad (8)$$

The expression clearly indicates that increasing C_{in} will lead to a corresponding rise in the input-referred noise of the overall system [7]. To minimize flicker noise, an optimal gate area for $M_{1,4}$ can be determined. It is worth noting that for low-frequency applications, lateral p-n-p transistors can be incorporated into standard CMOS technology, showcasing superior performance in terms of lower flicker noise compared to MOS transistors [8]. However, in the input transistors $M_{1,4}$, P-N-P devices are not utilized due to the potential current flow from the base in the MOS bipolar device. This current variation affects the DC operating point of the MOS pseudo-resistors, resulting in a higher low-frequency cutoff and a reduced incremental resistance.

3. Further Amelioration of Previous Design

Fig. 7 illustrates the entire 60-dB amplifying system, incorporating the design circuits and techniques discussed earlier, which effectively optimize the trade-off between power dissipation and input-referred noise. Notably, the front-end amplifier employs large PMOS devices (300/1.5 μm) in its differential pair, a deliberate choice made to mitigate noise levels.

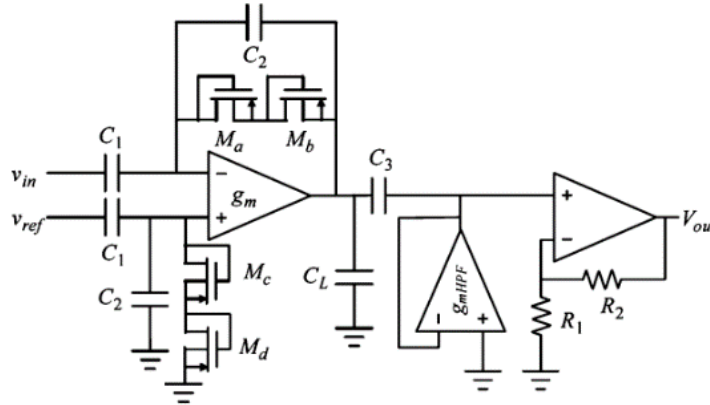


Fig. 7 Schematic of the ameliorated amplifier. A 40-dB front-end amplifier, g-C high-pass filter, and 20-dB gain stage follow (Photo/Picture credit: Original)

To ensure the removal of irrelevant low frequency signals before output, a g_m -C high-pass filter is incorporated after the initial amplification stage with a gain of 40 dB. The linear range of this circuit is extended by implementing "bump linearization" due to its operation in weak inversion [10]. The second gain stage provides an additional 20dB gain. A digital to analog converter is applied to provide the bias current of the high pass filter. This allows the pole frequency to be actively altered between 30 Hz and 1 kHz and be relatively easy to calibrate considering variations between chips. Fig.8 shows the logarithmic frequency-to-magnitude graph of this amplifier measured with different biasing current, creating high frequency poles at 300 Hz and 800 Hz [9].

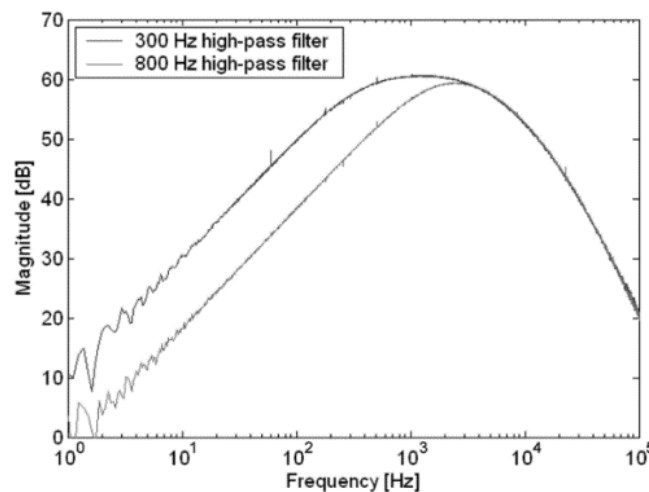


Fig. 8 Measured high-pass filter behaviour [9]

Cutoff frequencies exceeding 300 Hz may prove advantageous in scenarios involving the identification of nerve activity in the peripheral nerve next to large muscles. The electromyography signals produced by muscles exhibit considerable signal power in the frequency range below 1 kHz. Consequently, implementing a high-pass filter can effectively mitigate the interference caused by extraneous electronic signals and the system itself. The OTA at the initial gain stage establishes the 3 kHz cut-off frequency for the low-pass poles of the amplifier. Each amplifier in the two stages exhibits a current draw of less than 6 μA . The individual amplification system can be intentionally deactivated in order to conserve power while it is not being utilized.

4. Conclusion

Previously elaborated amplification system design for neural recording system treat noise proceeding and power consumption limiting as an emphasis rather than the amplification amplitude. So long as the signal swing remain in common range, the conventional design will always amplify the neural signal to an analyzable level. Due to the trade-off between power dissipation and noise reduction, achieving both low power and low noise design is currently infeasible. Effort needs to be made to reach an ideal balance between the two performance factors, whether from the aspect of circuit design or component design. If the CMOS process can be ameliorated, which stands for a greater transconductance for nearly all the components, the point of balance will surely be reduced to a much lower level. However, under current situation, further advances must be made under great difficulty.

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