

Advancements In Low-Power Technologies: Clock-Gated Circuits and Beyond

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Abstract. With the continuous advancement of the integrated circuit industry, there has been a steady rise in the level of integration and circuit scale. This inevitably leads to an escalation in power consumption by electronic devices, underscoring the growing significance of low-power technology. This comprehensive review initiates by elucidating the fundamental concept of low power, followed by an exploration of optimization measures utilizing clock-gated circuits as a prime example. Subsequently, it outlines the current challenges and prospects associated with low-power technologies. The core focus of this review revolves around the utilization of clock tree structures and triggers, which constitute the primary contributors to dynamic power consumption. These methodologies are presently the most prevalent and efficacious means to curtail power consumption through clock gating. The methodologies expounded in this review adeptly fulfill the objective of power reduction, ensuring that both present and future integrated circuits remain highly efficient. Thus, underscoring the critical role of low-power design in the realm of integrated circuit design.

Keywords: Integrated circuit, Low-power, technology, Clock tree, Trigger.

1. Introduction

Considering the advancement of technology, countries around the world attach great importance to the development of the integrated circuit industry. Integrated circuits have been widely applied, and the process technology of integrated circuits has improved rapidly, making innovation increasingly important. Due to the increasing integration density, the power consumption caused by chips is also increasing. Therefore, one of the most important aspects of integrated circuit design is how to lower the power consumption of integrated circuits.

Firstly, this paper explains the concept of power consumption, which mainly focus on dynamic power consumption and introduce low-power design techniques. Among many low-power designs, this paper chooses clock gating circuits for further analysis. When it comes to clock gating circuits, the two most critical points are the clock distribution network and flip-flops. This paper discusses the operation of double-edge-triggered flip-flops, which record data at both rising and falling edges of each cycle, outperforming single-edge-triggered flip-flops in terms of performance. Before introducing the clock distribution network, this paper also discusses an optimization measure that combines operand isolation and clock gating to effectively reduce dynamic power consumption. The network that distributes clocks is placed at the end of the second part as it is equally important. Gate-based clock gating technology may cause delays, thus an optimization solution based on a clock tree structure is proposed. In addition, several other clock gating techniques in detail are presented, which can be used to reduce dynamic power consumption. Finally, this paper mentions the existing challenges in low-power technology such as international situations, current technological level, and technological innovations. It affirms that there is still great development potential for low-power technology in the future as it follows the trend of the times. The primary goal of integrated circuit design is to reduce power consumption. Low-power technology has significant implications for the development and progress of integrated circuits.

2. Basic Theory of The Design

2.1. Power consumption concept

2.1.1 Power source

Static power consumption and dynamic power consumption together make up the circuit's overall power consumption. The process parameters of the transistor and the condition of the circuit's operation are also directly related to the overall amount of power consumed. For CMOS circuits, there are two main sources of power consumption, which are static and dynamic. Among them, the dynamic power consumption is made up of short-circuit power consumption and switching power consumption [1]. The static one is also called leakage power consumption. As shown in Figure 1. This is a CMOS inverter circuit. Take this circuit model as an example to analyze the power consumption.

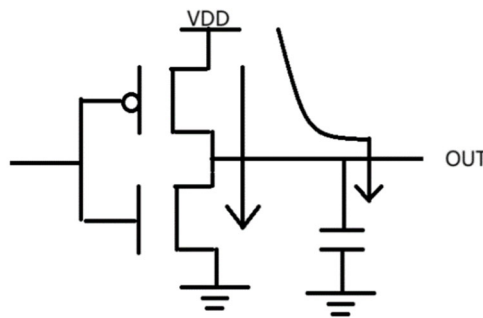


Fig. 1 leakage power consumption (Photo/Picture credit: Original)

2.1.2 Dynamic power consumption

The power supply charges and discharges the gate output capacitance to produce switching power $P_{switching}$ when a logic transition occurs in the CMOS logic gate's output node voltage. When the control signal changes from 1 to 0, the power line VDD charges the output load capacitor. When it changes from 0 to 1, the load capacitor discharges the ground VSS. In one charge and discharge cycle, the energy consumed is.

$$Energy/transition = C \cdot V_{DD}^2 \quad (1)$$

P_{trans} is the transition probability at the output when the clock changes. f_{clock} is the clock frequency. Switching power consumption $P_{switching}$ is

$$P_{switching} = C_L \cdot V_{DD}^2 \cdot P_{trans} \cdot f_{clock} \quad (2)$$

C_{eff} is the equivalent capacitance, which is the average capacitance switched per clock cycle. The switching power can be expressed as

$$P_{switching} = C_{eff} \cdot V_{DD}^2 \cdot f_{clock} \quad (3)$$

It is a common representation of switching power. Short circuit power is generated when there is a way from power line to the ground. The PMOS transistor turns off when the input voltage exceeds the difference between the threshold voltage of the PMOS transistor and the power line. The NMOS and PMOS tubes are both switched on simultaneously. There is a path created between the ground and the power line, which causes short-circuit power consumption.

2.1.3 Static power consumption

Leakage power consumption is another name for static power consumption. It occurs when the circuit is idle or inactive. Leakage current is mainly divided into four parts: reverse-biased diode leakage current, subthreshold leakage current, gate-induced leakage current, and gate-gate leakage current, which is shown in figure 2.

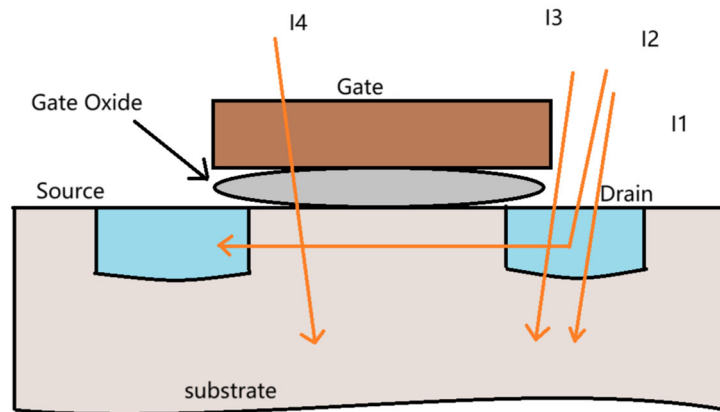


Fig. 2 Schematic diagram of four leakage currents (Photo/Picture credit: Original)

- (1) Reverse-biased diode leakage current. The device has a reverse biased diode. When a voltage is applied, a current travel from the source and drain to the substrate I1.
- (2) Subthreshold leakage current. A current I2 travels from the drain part to the source part through the weak inversion region, which is the subthreshold leakage current.
- (3) Gate-induced leakage current. When the source or drain diffusion region is different from the substrate potential, the leakage current I3 is generated. This leakage current is small compared with other leakage currents.
- (4) Gate-gate leakage current. Under the influence of the gate voltage, the current I4 travels directly from the gate through thin gate oxide layer to the substrate.

2.2. Low power design

Commonly used low-power design technologies include clock gating (Clock. gating) technology, multi-threshold device (MTCMOS) technology, power supply shutdown (PSO) technology and multiple supply voltage (MSMV) technology. Among them, the principle of gating clock technology is to reduce the flip rate of the flip-flop clock and thus reduce the dynamic power consumption. Multiple threshold device technology and power shutdown techniques for low leakage power consumption. The multi-supply voltage technology and power-off technology are generally used in the chip layout stage.

This article focuses on clock gating techniques. First of all, the clock network accounts for a sizable portion of the chip's dynamic power usage. Gated clock technology controls the opening and closing of a unit clock by adding a gated clock unit and reduces the dynamic power consumption of the clock network by reducing the total flip-flop rate. The clock distribution network and FF constituted by the clock matrix are the components that consume the most power in many VLSI digital systems. It consumes 30% to 60% of the system power, 90% of which is used in the final part of the FF and clock distribution network to drive flip-flops. Complementary clock power division of the system thanks to new generation frequency scaling and extensive pipelining. Due to the power consumption constraints of today's portable digital circuits, it is necessary to reduce the power consumption of clock networks and flip-flops [2].

2.3. History of Low Power Design Development

In the early stage of integrated circuit development, the circuit design scale was small, and the operating frequency was low. Chip performance is the designer's primary consideration. The level of integration and operation frequency of circuits have increased due to the semiconductor industry's rapid expansion, thereby increasing power consumption. Power consumption is dissipated in the form of heat energy, and excessive power consumption will increase the temperature of the circuit, resulting in failure. The need to use packaging materials with better thermal performance will increase the cost of chip packaging. The restriction of power consumption on the development of integrated circuits has prompted academic circles to pay attention to low power consumption design. In the early

stage of low-power design development, the primary source of chip power consumption is dynamic power consumption. Kaushik Roy analyzed the causes of power consumption in SOC chips, analyzed the power consumption indicators through mathematical modeling, and then proposed a variety of methods to reduce dynamic power consumption [3]. According to the principle of dynamic power generation, design methods such as multi-power multi-voltage and gating clocks have been applied to chip design. As the size of transistors gradually decreases, the leakage current of devices increases gradually, the amount of static power usage steadily rises as a percentage of total power consumption, and the low power consumption design of static power consumption has been paid attention to [4]. According to the principle of static power generation, power shutdown technology is applied. At the 16nm process node, the FinFET CMOS structure began to be used, which significantly reduced the leakage of the device. EDA is also developing with the development of low power consumption technology. In 2005, Cadence pioneered the Common Power Format CPF [5]. Subsequently, Synopsys introduced a unified power consumption format UPF [6]. After entering deep sub-nanometer design, major chip design companies attach importance to low-power design. With the progress of research, the research of IR Drop has gradually become a hot spot in the field of low power consumption. Foreign research on chip power supply network structures, such as Mesh structure and Tree structure, has proposed power network analysis methods based on pre-optimized conjugate gradient method and nested hierarchical network division [7] (Figure 3).

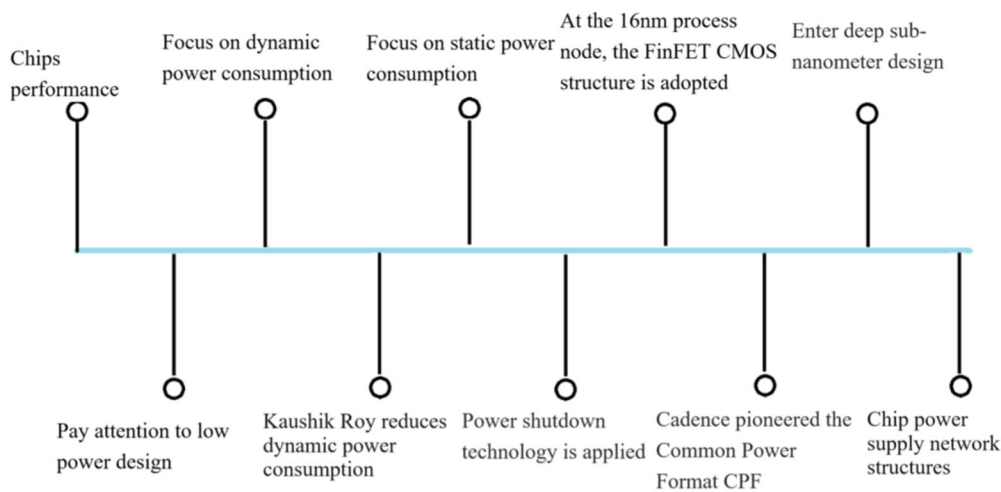


Fig. 3 History of low power design development (Photo/Picture credit: Original)

3. Techniques and Innovations in Clock Systems

Integrated circuits' power consumption typically consists of two main components: static power consumption and dynamic power consumption. This article primarily focuses on dynamic power consumption. Within dynamic power consumption, there are two subcomponents: one is due to the power dissipation of the load capacitance, referred to as switching power (or toggle power), which constitutes a significant portion of dynamic power consumption. The other component is mainly caused by short-circuit currents and is termed internal power. As indicated by Equation.

$$P_{switching} = t_{sc} \cdot V_{DD} \cdot I_{peak} \cdot f_{clock} \quad (4)$$

t_{sc} stands for the duration of the short-circuit current, while I_{peak} represents the total short-circuit current (including the current used for charging internal capacitors). The supply voltage, toggle rate, and load capacitance are all directly related to dynamic power consumption. Furthermore, in modern digital circuits like VLSI, the clock distribution network, and flip-flops (FFs) comprising the timing matrix are key contributors to power consumption [8]. As a result, a number of solutions have been suggested to lower clock system power consumption.

3.1. Double-Edge Triggering

Double-edge triggering refers to capturing data on both the rising and falling edges of each clock cycle, resulting in two data captures within one clock period. Given the substantial power dissipation stemming from clock lines, a novel low-power pulse generation circuit has been proposed [2]. This circuit, tailored for the 45nm technology node, employs signal propagation from input sources to internal nodes of latches. The clock generates short pulses at both ends of the clock cycle, allowing each pulse to capture data and generate results. This approach reduces transition time, balancing power, and speed performance. Compared to Static Control Discharge Flip-Flops (SCDFF), Double-Edge Triggered Static Pulse Flip-Flops (DETSPFF), and prior work on double-edge triggered flip-flops, this design exhibits superior power and delay characteristics under various parameters.

3.2. Clock Gating and Operand Isolation

Operational processes in actual digital circuit devices are typically carried out by functional units, making it possible to address power reduction at the level of individual processor units. A common logic unit within functional units is the Arithmetic Logic Unit (ALU). Rashmi Samanth et al. [9] introduced operand isolation and clock-gating techniques to lower dynamic power. Operand isolation prevents unnecessary logic transitions by isolating input logic, thereby minimizing redundant switching in data paths. Clock gating involves controlling clock signals to conserve energy when operations are not needed. By adding gate circuits to disable clock signals when unnecessary, capacitor charging is avoided. This method effectively reduces energy consumption in unused sections. Rashmi Samanth et al [9]. combined these techniques, incorporating functional unit isolation and enabling input to ALUs, ensuring ALUs only operate within specific time intervals determined by clock gating. RTL-level synthesis using Cadence 180nm technology demonstrated the effectiveness of this approach in reducing dynamic power.

3.3. Multi-Source H-Tree Clock Distribution Network

According to research, Clock Distribution Networks (CDNs) account for a sizeable amount of the chip power consumption in dual-core processors [10]. Reduced metal layer requirements, simplified routing, shorter clock network delays, and improved clock generator power are the main objectives of CDN. Conventional Clock Tree Synthesis (CTS), however, is associated with drawbacks like high power consumption, increased delay, and skew. Srivatsa V G et al [11]. proposed a Multi-Source Clock Tree Synthesis (MSCTS) scheme implemented at the 7nm process node, utilizing a symmetric H-Tree structure. MSCTS improves clock delay and skew by employing multiple clock sources based on the distribution of clock receivers, reducing the need for buffer insertion for timing optimization. This approach enhances overall power consumption and clock Quality of Results (QoR).

3.4. Clock Gating

Clock gating is one of the most used methods for reducing dynamic power in integrated circuits. As mentioned in, clock gating can be based on gate-level elements such as AND, OR, NAND, NOR gates, offering simplicity and ease of implementation [9]. However, gate-based clock gating can lead to glitches due to the longer rising transition time compared to falling transitions during signal conversion from low to high voltage levels, resulting in a higher probability of glitches during rising edge triggering [12]. Let's delve into these diverse techniques that further refine the art of clock gating.

The Latch-Based Clock Gating technique uses edge-sensitive latches. The clock signal is ANDed with an enable signal before reaching the latch's output and the system clock. This occurs when the clock signal is low, and it enable signal changes during a high level, causing circuit faults and subsequent delays. Flip-Flop-Based Clock Gating employs edge-triggered flip-flops for controlling the enable signal. Similar to latch-based gating, it involves an AND logic operation with the clock signal. Yet, longer dormancy periods and susceptibility to glitches demand larger capacitance, boosting dynamic power consumption and influencing design [13]. Synthesis-Based Clock Gating uses EDA tools to reduce power consumption by minimizing clock pulses. System-level clock enable

signals define module clock cycles, but manual addition for each flip-flop is often needed. High-level operational states can cause slow transitions, leading to power-hungry redundant activities. Data-Driven Clock Gating addresses redundancy in synthesis-based gating [14]. It employs OR gates to store a cycle's output, eliminating glitches. Both flip-flops are gate-controlled, resulting in less power consumption. XORing the flip-flop's clock gating signal with its input reduces power usage. Autogated Clock Gating (AGFF) uses master and slave flip-flops. During the clock's falling edge, the master flip-flop becomes transparent. An XOR gate determines if the slave flip-flop's state should change. Yet only the slave flip-flop is gate-controlled, leaving part of the clock load uncontrolled, and strict timing constraints affect critical path flip-flops [15]. Lookahead-Based Clock Gating (LACG), derived from Autogated Flip-Flops, predicts each flip-flop's clock gating signal a cycle ahead. This avoids tight timing constraints, reduces redundant clock pulses, optimizes gate logic, and significantly lowers power consumption compared to AGFF and data-driven techniques [15].

4. Challenges and Future Prospect

4.1. Challenge of Low Power Sign

One of the challenges is the application of integrated circuits. Different regions and countries have different strengths in technology in the integrated circuit industry. Due to globalization, advantageous technologies in various fields can be reasonably allocated so that the integrated circuit industry can develop rapidly. However, in recent years, the severe international situation caused by the global outbreak of epidemics and frequent international trade disputes has to some extent affected international academic exchanges. The obstruction of technical factors makes it difficult for demand chains and supply chains in various countries and regions to be perfectly connected. Each country faces challenges and tends to build a self-sufficient complete industrial chain [16]. In this regard, failure to optimally allocate resources will lead to a slowdown in the development speed of the integrated circuit field.

Another challenge lies in the technical means themselves. Firstly, it needs to understand that the biggest limiting factor for low-power technology in integrated circuit design is power consumption. Because power optimization can be done at many design hierarchy levels, there are many alternative optimization approaches and procedures that can be used.

Taking clock gating as an example, when our design goal is to minimize power consumption, we need to minimize the power consumption of clock distribution networks and flip-flops, because they are the most important components of the clock system and can significantly affect circuit power consumption. When we can successfully optimize the design of these two components, a large part of the optimization for clock gating has already been completed. But this means that the structure becomes more complex and takes up more area, which can cause resource waste. Although we have been able to successfully balance the impact between the two, there is still room for improvement in related technologies. How to further improve this is our next task to complete.

4.2. Future of Low Power Sign

In terms of future development, the development path required by Moore's Law has shifted towards a new feature of improving energy efficiency ratio, entering the "post-Moore era" [16]. Low-power technology aims to improve efficiency and reduce power consumption. The application of low-power technology in integrated circuits is in line with the development path and current trend. Undoubtedly, it will become a major driving force for the development of low-power technology with a bright prospect.

In the post-pandemic era, international exchanges have become more frequent than before, while frictions between countries persist. As a hot topic in the industry, the integrated circuit sector is investing more resources to stimulate development and avoid being restricted by others. The current core objective of integrated circuit design is high efficiency, thus continuous breakthroughs are

sought in this area. Timing circuits, as a major means of low-power consumption, will receive sufficient development and have great room for improvement in the future.

5. Conclusion

The conclusion of this paper is as follows. Firstly, several techniques are listed to reduce the power consumption of the clock system. In the aspect of Double-edge triggering. A novel low-power pulse generation circuit is designed and implemented for the 45nm technology node. Clock gating and operand isolation is created, because the possibility to reduce power at single processor unit level. As for Multi-Source H-Tree clock distribution network. Researcher made a Multi-Source Clock Tree Synthesis (MSCTS) scheme for 7nm process node by using a symmetric H-Tree structure. Clock gating is a widely used technique which is to reduce dynamic power. It can be based on gate-level elements. There are also other kinds such as latch-based clock gating, flip-flop-based clock gating, synthesis-based clock gating, lookahead-based clock gating (LACG), data-driven clock gating and autogated clock gating.

Secondly, the challenge of low power design should be faced. Overcome the difficulties that prevent optimal resource allocation. Know more about technical. Power optimization can be done in different levels, for example, we minimize the power consumption of clock distribution networks and flip-flops when we want low power consumption. Although good progress has been made in low-power design, there is still much research to be done. Due to the limited level of technology, low power consumption design requires more components.

Authors Contribution

All the authors contributed equally, and their names were listed in alphabetical order.

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