

Current Status, Development, And Application of Optimization Methods for Analog Circuits

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Abstract. The optimization of analog circuits has always relied on the experience and intuition of engineers to find suitable parameters to meet the requirements of the circuit, which is time-consuming and costly. This paper outlines and analyzes the optimization methods for analog circuits in recent years, and draws some summaries that can be used as references for subsequent optimization circuits. The optimization of analog circuits is mainly divided into the optimization of the performance of the hardware in the circuit and the optimization of the circuit structure. Hardware optimization, this paper mainly focuses on the optimization of diodes, transistors, field effect tubes and operational amplifiers, the four main hardware optimizations, from the material, structure, production process and other aspects of the analysis. For the optimization of circuit structure, this paper mainly analyzes from the aspects of algorithms, mathematical models, and the use of integrated methods. The significance of these optimization methods and the outstanding advantages and main application directions of different methods are further explained. The search for optimization methods can reduce the high time cost of analog circuit optimization that is purely dependent on experience and intuition, and is significant in increasing efficiency.

Keywords: Analog circuits; Hardware Optimization; Circuit structure optimization.

1. Introduction

Optimization of analog circuits must rely on the established experience and intuition of the engineer and cannot be achieved in one step through a wide range of methods that can be applied to a variety of situations. So, it is crucial to find various ways to optimize analog circuits. Analog circuits consist of both hardware and circuit structure. On the hardware side, finding the appropriate parameters for each part of the hardware is the most generalized method for optimizing hardware performance. However, as the size of the hardware becomes smaller and smaller and the performance requirements become higher and higher, it is difficult for the original manufacturing process or structure to meet the needs of the hardware to continue to optimize the hardware, so new structures and materials are proposed and applied to the components to break through the bottleneck of optimizing the performance of the components. Optimization of circuit structure, the search for the most suitable circuit form must rely on engineers, but through some algorithms or models to allow computer-assisted, thereby reducing the workload and increasing efficiency. As the use of analog circuits expands step by step, the search for these optimization methods is imminent.

2. Analysis of hardware optimization techniques for analog circuits

The basic devices in analog circuits are mainly diodes, transistors, field effect tubes and operational amplifiers. Improving the structure of these hardware can optimize the hardware function and thus optimize the circuit performance.

2.1. Optimization of Field Effect Tubes

The optimization of FETs has the following directions: doping, structure, and material. At the same time, in recent years, the optimization of FETs is not only based on traditional structures and

materials, but also many new FETs with good performance and prospects. Such as tunneling FETs, graphene nanoribbon FETs, carbon nanotubes, organic FETs, finned FETs and so on.

Improved doping is the main way to optimize field effect tubes. It can be categorized into improving doping concentration, doping strategy, utilizing new doping materials and techniques, etc. In terms of improving the doping concentration, the doping concentration is related to parameters such as forbidden bandwidth, which in turn affects the operating temperature, current gain, and so on. Therefore, selecting the appropriate doping concentration can improve the device performance. Improvement of doping strategy, doping strategies such as the traditional uniform doping strategy, linear doping strategy, gradient doping strategy, etc., to obtain the ideal distribution of the doping structure can optimize the device performance. In "Optimization of Carbon Nanotube Field Effect Tube Performance Based on Gradient Doping Strategy", a drain-side gradient doping strategy is proposed, where a light doped region and a heavy doped region are set up at the drain electrode, respectively [1]. After finding the appropriate doping concentration, the method effectively reduces the bipolar transmission characteristics of the device and improves the device switching current ratio. In terms of utilizing new doping materials and techniques, the device performance can be optimized by selecting appropriate doping materials and doping methods. In the "ferroelectric doped three-dimensional finned field effect transistor performance optimization study", the electrical doping technology based on ferroelectric materials is proposed, and the electrical doping technology to some extent solves the problem of lower doping accuracy of the traditional chemical doping technology in the small-size device, but it still faces the problem of not being able to effectively enhance the open-state current due to the pinning effect of the Fermi energy level [2]. In recent years, there have been innovations and breakthroughs in the selection of new doping materials and doping processes. With the device size getting smaller and smaller, improved doping is a major feasible way to break through the existing bottleneck, and there are many aspects that deserve to be in-depth.

Improvement of FET structure is an effective means of optimization, by changing the device channel and other parameters to improve the performance of the field effect tube, at the same time innovative non-traditional structure of the field effect tube, such as finned field effect transistor, graphene nanoribbon field effect tube, tunneling field effect tube [2-4]. Among them, the fin-shaped structure of finned field effect transistors can increase the control area, structurally solving the short channel effect that cannot be avoided by planar field effect transistors, with low leakage current, low threshold slope, etc., which has a promising prospect for optimization of devices with shrinking dimensions [5, 6]. In the previously mentioned study, finned field effect tube FinFETs were further optimized by improving the doping pairs [2]. In "Reliability Study of Finned Field Effect Transistors at the Atomic Scale", the process, design, and electrical reliability of 7 nm fin-width FinFET devices were investigated, and it was concluded that improving the insulation of the isolation layer and the stability of the top of the finned structure can improve the FinFET devices' Electrical reliability, process, FinFET devices still have some difficulties in high-precision etching [6]. In 2D fin field-effect transistors, 2DFinFETs with planar structures are studied, and it is envisioned that If current method to fabricate 2D fin structures can be applied to general vdW 2D semiconductors and p-type 2D FinFETs can be produced, The powers of 2D FinFETs in next-generation CMOS FETs will be significantly improved. FinFETs have a promising future as a device with improved structure [7].

Graphene is expected to replace silicon as the next-generation integrated circuit material due to its unique electronic properties. However, large-size flake graphene is a material with zero bandgap, which is not favorable for its application. In contrast, the banded graphene nanoribbons in the improved structure of graphene field effect transistors make the bandgap increase significantly, which can meet the demand of large switching current ratio of digital circuits [3].

The Tunneling Field-Effect Transistor (TFET) relies on the principle of band-tunneling of carriers to control the operating state of the device by controlling the gate voltage. Since the temperature has almost no effect on band-band tunneling, it can obtain better device power consumption, temperature characteristics, switching current ratio, etc., compared with conventional MOSFETs, and is a new type of device that is expected to realize ultra-low-power chips [4]. In further optimization of the

structure, an L-type TFET is proposed, which utilizes the principle of line tunneling to obtain greater advantages in open-state current and subthreshold swing [4].

As more new structures were proposed, the FETs gained more leaps and bounds in optimization from the improvement of the working principle. For material optimization, the purpose of optimizing the characteristics of the field effect tube is generally reached by improving the material processing process or proposing novel materials. For example, in 2022, a method to improve the contact condition at the interface of molybdenum disulfide by oxygen plasma treatment was proposed, in which the state of molybdenum dioxide was altered by the oxygen plasma treatment process, and the generated layer of molybdenum trioxide was utilized to protect the molybdenum dioxide while removing the organic impurities at the interface, thereby improving the device performance [8].

2.2. Diode Optimization

In recent years, the optimization of diode results are mainly focused on some specific types of diodes to do further in-depth research. The optimization is mainly carried out by improving the preparation process and innovating the diode structure. As for the improvement of the preparation process, the diode performance can be optimized by improving the preparation of certain key materials of the diode, which can improve the material stability, purity, etc., and make them more suitable for the working requirements. For example, in 2022 a preparation optimization method for platinum-doped diodes was proposed to find the preferred solution by adjusting the conditions of high-temperature diffusion, platinum diffusion, and other processes [9]. In 2021 a method to optimize chalcogenide light-emitting diodes was proposed. A more suitable method was searched by preparing chalcogenide thin films in one step and preparing various devices with electron transport layers by solution and vacuum vaporization methods [10]. In 2023, a method to optimize the film-forming flatness of chalcogenide materials was proposed to improve the film coverage by adjusting the chalcogenide grain size, as well as the innovative introduction of graphene quantum dots to increase the number of grains and improve the current efficiency of the devices [11].

The structural aspect of innovative diodes is generally achieved by adding a new structure or improving the original structure, which makes the diode gain higher in various performance aspects. For example, in 2022, a diode with an improved shape of the original electron barrier layer (EBL) was compared to be more effective in suppressing electron leakage when the structure was an inverted trapezoidal rectangle [12]. In terms of innovative new structures, a vertical GaN-based trapezoidal diode with a composite dielectric layer was proposed to improve the voltage resistance of the device, and in 2021, a scientific research team further optimized this by adjusting the width of the dielectric layer, the size of the trapezoidal bottom angle, and other parameters to find a better structure, which effectively improves the voltage resistance of the device [13].

2.3. Triode optimization

In recent years, there have been fewer studies on the optimization of triode, and its optimization method has similarities with the optimization of diode, and the optimization purpose is mostly reached from the aspect of improving or innovating the structure.

In 2018 a nano-gap channel tunneling triode structure was proposed, which initially realizes the ballistic transport of electrons in the nano-gap channel with excellent characteristics such as high switching current ratio, and this research is conducive to improving the possibility of device miniaturization [14]. An injection-enhanced gate transistor (IEGT) was proposed. This structure has dummy trench and larger cell pitch. This structure increases the carrier concentration at the N-emitter side, which results to lower on-state forward voltage drop compared to traditional structures [15].

2.4. Operational amplifier optimization

Operational amplifier optimization methods are more diverse, in addition to directly improving the hardware structure, there are also methods such as using algorithms, building models and simulation.

In terms of improving the hardware structure, the optimization is achieved by innovating the internal circuitry, etc. In 2019, a new type of low-noise bias current compensation circuit was proposed and applied to operational amplifiers. The operational amplifier designed using this structure effectively reduces the adverse effects of noise and gains on various parameters [16]. In optimization using algorithms and models, the main use is to abstract the optimization objective of operational amplifiers into a mathematical model and then apply different algorithms and improve the algorithms to achieve the optimization purpose. In 2020, a study was conducted to optimize operational amplifiers by improving the Gray Wolf algorithm. The study proposed an enhanced Alpha-oriented Gray Wolf algorithm while abstracting the mathematical optimization model with the objective of maximizing the open-loop low-frequency gain. The algorithm improves the Alpha wolf guidance mechanism and introduces a variation operator to enhance the algorithm's ability to jump out of the local optimum point [17]. In the same year, a study used the Salp Swarm algorithm to reduce the power consumption and area of a two-stage CMOS operational amplifier [18]. Due to the variety of algorithms, optimization using this method has a wide scope for research.

3. Optimization of Circuit Structures

In the optimization of analog circuits, the optimization of the circuit structure is mainly done by various methods to improve the circuit structure and to find a circuit form with lower delay and higher efficiency. Optimization of analog circuits relies on the experience and intuition of engineers to find the right parameters to meet the requirements of the circuit, which is time-consuming and costly [19]. Therefore, it is essential to find suitable methods to optimize circuits quickly.

3.1. Application of Algorithms and Mathematical Models to Circuit Optimization

Optimization methods for circuit structures are mainly focused on the use of algorithms, abstract mathematical models, simulation, and the use of new technologies. In 2010, a parameter optimization circuit optimization algorithm based on reinforcement learning was proposed, in which researchers improved the efficiency of training on different parameters and models through reinforcement learning, which in turn can be used in circuit optimization to improve the efficiency of circuit optimization [20]. In 2023, a logic circuit optimization method based on tree Mux was proposed, in which the number and level of Mux gates in the Mux tree are reduced by converting case statements to tree Mux, and then merge the case statements to achieve the reduction of the number and level of Mux gates in the Mux tree, and realize the streamlining of address recoding circuits by simplifying the address logic, and then realize the optimization of the area and delay of the mapped circuits [21]. In 2016, a circuit optimization based on the simulated annealing algorithm was proposed. The study is based on the idea of simulated annealing optimization algorithm, to establish the optimization model of the transfer function, and to optimize the objective function by using the piezoelectric shunt control method for vibration suppression, based on the analysis of the rotating beam piezoelectric shunt control equations using the simulated annealing algorithm for the optimization of the resistive and inductive originals in the circuit. Compared with the more traditional genetic algorithm, the simulated annealing optimization algorithm can not only achieve good optimization efficiency [22]. In 2017, a study presented the optimal design of analog integrated circuits based on genetic algorithm. Genetic algorithm as an optimization algorithm can be effectively used in the optimal design of analog circuits. This study applied genetic algorithm to multi-objective design, constructed a performance index fitness function, and completed the multi-objective circuit optimization design for four parameters: low-frequency gain, bandwidth, conversion rate, and current [23].

The use of algorithms and models to optimize circuits is one of the main methods, through the computer can assist the manual search for the structure of the circuit form more suitable for the requirements, at the same time in the multi-objective optimization has an extremely effective use.

3.2. Application of Integrated Methods to Circuit Optimization

Circuit optimization design can be solved more efficiently using integrated methods, which may use some cross knowledge from other fields or refer to methods mentioned in other scientific research. Most of the research is done by innovating some methods as a basis for the optimal design of circuits. They usually incorporate multiple aspects of technology, which, when synthesized, result in innovative circuit optimization methods and optimized performance.

In 2019, a study of a Zynq-based CMOS sensor interface logic circuit optimization design and image processing technique was presented. The study optimized the design of functional modules and achieved results such as hardware acceleration and optimized image processing [24]. In a 2021 study, correlation curves of parameters were established by resolving MOS tube parameters under different models as a starting point, through which the design flow and calculation were further simplified [25]. In 2023, a study of a molecular circuit optimization model based on DNA strand substitution was presented, which refers to a DNA circuit that uses the DNA molecule as a biocomputing material, and utilizes some knowledge from biological disciplines, and synthesizes a winner-take-all neural network, to achieve the optimization of this new type of biological circuits. In this case, the use of comprehensive knowledge from various disciplines has led to the achievement of innovative circuit forms and optimized circuits [26]. In 2020, a study of an optimization method for electromagnetic forming circuits based on finite element analysis was presented. Electromagnetic forming circuits and finite element analysis were utilized in the study, with the former being more widely used in the field of lightweight alloy processing, and finite element analysis as a mathematical simulation method playing an important role in this desired study. By cross-utilizing methods from different fields, new ideas for problem solving can be innovated [27]. The application of integrated methods reaches a more efficient optimization through methodological innovation.

4. Conclusion

This paper summarizes the optimization methods for the hardware aspect of analog circuits and the circuit structure aspect. On the hardware side, common optimization methods include adjusting and finding the right parameters, improving the structure, using innovative materials, and improving the manufacturing process. On the circuit architecture side, common optimization methods include using different algorithms, building mathematical models, and integrating knowledge from various fields and applying them together. Some of these methods are interoperable, for example, algorithms can be used to find the optimal solution for a hardware structure and so on. Optimization in different places can sometimes affect each other, such as the hardware that may need to be used after adjusting the circuit structure may be different, and the type of hardware that can be used to achieve a greater benefit may also be different. The comprehensive optimization of analog circuit performance can be better accomplished by optimizing both hardware and circuit structure.

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