Unlocking The Potential of Balanced Ternary Chips: A Paradigm Shift in Computing

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Abstract. The current landscape of digital computing predominantly relies on the binary system, limited to representing information using only 0 and 1. Nevertheless, the relentless progression in chip design and manufacturing technology has pushed traditional binary chips to the confines of Moore's Law. To transcend these limitations, alternative computing paradigms are being explored. Among these, balanced ternary chips have emerged as a disruptive concept, offering a fresh perspective. This paper delves into the fundamental principles of ternary computing, elucidates the reasons underpinning its adoption, and discusses chip design considerations. Additionally, it provides insights into the real-world applications of ternary chips, highlighting both research and practical cases. Furthermore, the paper explores the challenges currently faced by balanced ternary computing and outlines potential directions for future development. In conclusion, this research not only broadens our understanding of ternary computing but also underscores its significance in reshaping the landscape of computing technology, potentially overcoming the limitations of binary systems, and ushering in a new era of computational efficiency.

Keywords: Balanced Ternary; Logic Gate; Half-Adder.

1. Introduction

In the realm of contemporary digital computing, the binary system reigns supreme, relying exclusively on the simple, binary code of 0s and 1s to convey and manipulate information. This binary foundation has been the cornerstone of computing since its inception, offering a robust framework that has fueled remarkable advancements in technology. However, as it finds in an era characterized by relentless innovation and exponential growth in chip design and manufacturing capabilities, the boundaries of traditional binary chips are converging with the limits of Moore's Law [1].

To surmount the confinements of traditional binary computing, researchers and innovators have embarked on a quest to explore alternative computing paradigms. Among the myriad of promising approaches, one stands out as a disruptive and transformative concept: balanced ternary chips. Unlike the binary system, which adheres to a binary logic of only two Boolean values, namely 0 and 1, balanced ternary computing introduces a paradigm shift by incorporating three distinct states: 0, 1, and -1. This fundamental departure from binary's binary nature unlocks a treasure trove of new possibilities. Balanced ternary computing holds the potential to revolutionize the way we perform computations, offering not only the prospect of more efficient and versatile arithmetic but also the tantalizing promise of substantially reduced energy consumption [2]. This shift to ternary logic challenges conventional thinking and invites us to reimagine the very essence of computation itself. As balanced ternary chips gain prominence on the horizon of technological innovation, they have captured the imagination of researchers, engineers, and industry leaders alike. Their potential to redefine the boundaries of what is computationally possible has kindled a fervent interest in unlocking the power of ternary computing [3]. However, amid the excitement and promise, it is essential to acknowledge that practical application of balanced ternary presents its own set of challenges.

This article delves into the heart of balanced ternary computing, offering a comprehensive exploration of its foundational principles, the rationale behind its adoption, and the intricate considerations that underpin chip design in this novel paradigm. Additionally, it shines a spotlight on the real-world applications of ternary chips, elucidating both research-driven insights and practical use cases. Furthermore, this article ventures into the uncharted territory of challenges currently confronting balanced ternary computing and maps out potential trajectories for future development.

2. Ternary Basics and How Ternary Chips Work

2.1. Basic Theory

Balanced Ternary is a special kind of ternary and consists of 3 digits: -1, 0, and 1. In order to facilitate representation, "T" will be used in the following text to denote -1. Balanced Ternary has some advantages in certain specific applications, especially in hardware design because negative numbers can be represented without using complement codes.

Same as in traditional ternary, the weight of each digit in the balanced ternary is a power of 3. For example, a balanced decimal number 25 can be represented as $(10T1)_T$:

$$25 = 1 \times 3^3 + 0 \times 3^2 + (-1) \times 3^1 + 1 \times 3^0 \quad (1)$$

2.2. Reasons for Using Balanced Ternary

2.2.1 Mathematical Demonstration

The way to compare which numeral system is more efficient is to that given the same quantity of numbers to express, the one that consumes the least number of digits, is the most efficient. For instance, if we want to represent a hundred numbers from 0 to 99 in decimal, then we will need 10*2=20 digits, but if we want to represent them in binary, then we will just need 2*7=14 digit. So that binary is more efficient than the decimal. If we summarize this as a function, it can be got.

$$E(x) = \frac{n}{x \times \log_x n} \quad (2)$$

Where x represents the base of the numeral system, and n is a constant representing the quantity of numbers to be expressed.

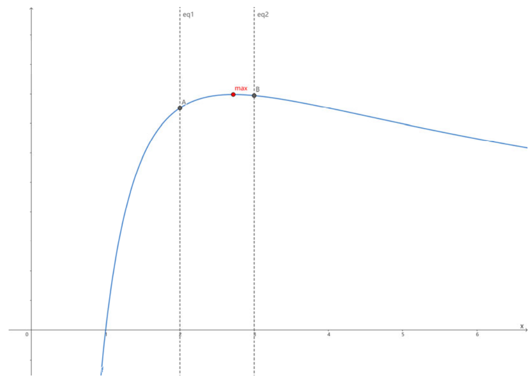


Fig. 1 Figure of the function of the numeral system base (Photo/Picture credit: Original)

As shown in Fig. 1, If x equal to e, then the efficiency of this numeral system is the highest. However, it is not possible for a numeral system to be equal to e. Nevertheless, it can be seen from the graph that the efficiency of the ternary system is greater than that of the binary system. In the following sections, we will explore practical applications and implementations with the ternary system.

2.2.2 Advantages in Circuit Complexity and Power Consumption

Balanced ternary chips could have the advantage of simplifying circuits and reducing power consumption [4]. This is of significant importance, especially in cases such as embedded systems, mobile devices, and other applications which is very sensitive to power usage. Unlike binary systems, which require additional bits to represent the same quantity of numbers, leading to increased electronic components in the circuit and subsequently raising power consumption and manufacturing costs, the use of balanced ternary systems caves circuit space and minimizes power consumption. This makes balanced ternary chips a better choice in resource-limited applications.

2.3. Chip Design

2.3.1 Truth Table for Balanced Ternary Logic Gates

In balanced ternary logic, -1 or T represents false, while 0 represents unknown, meaning it could be either true or false, and 1 represents true.

Table 1. AND Gate

AND	T	0	1
T	T	T	T
0	T	0	0
1	T	0	1

In the balanced ternary AND gate shown in the Table 1, if either of the two inputs is false, the result is always false. However, if one is true and the other is unknown, the result is unknown because it could be either true or false. Only when both inputs are true does the output become true. The AND gate can also be referred to as a MIN gate because the output result is always the minimum of the inputs. In the balanced ternary OR gate shown in the Table 1

Table 2. OR Gate

OR	T	0	1
T	T	0	1
0	0	0	1
1	1	1	1

The OR gate can also be referred to as a MAX gate because the output result is always the maximum of the inputs. The same, NOT, XOR, NAND, and NOR gate is shown in table 3-6.

Table 3. NOT Gate

NOT	T	0	1
	1	0	T

Table 4. XOR Gate

XOR	T	0	1
T	T	0	1
0	0	0	0
1	1	0	T

Table 5. NAND Gate

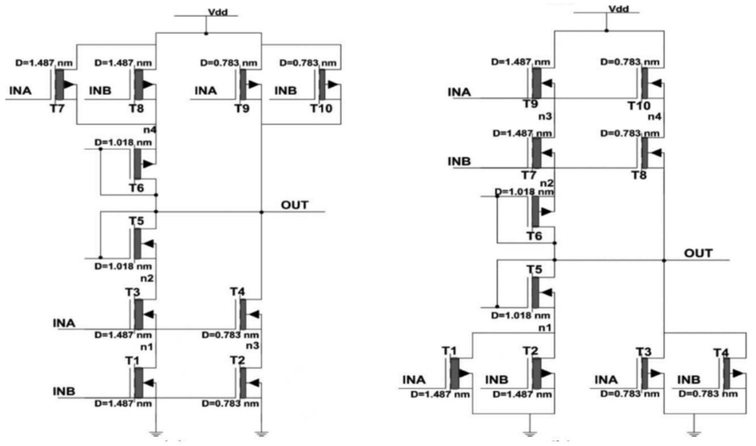
NAND	T	0	1
T	1	1	1
0	1	0	0
1	1	0	T

Table 6. NOR Gate

NOR	T	0	1
T	1	0	T
0	0	0	T
1	T	T	T

2.3.2 Ternary Logic Gates and Half Adder Design

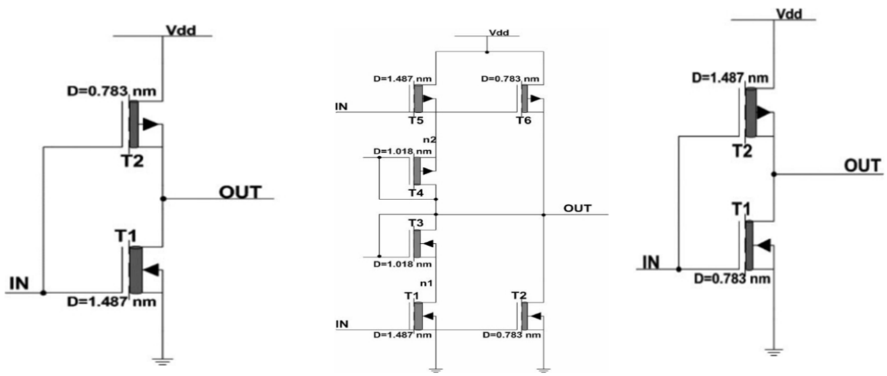
Sheng Lin and colleagues created a ternary half adder using CNTFETs, or Carbon Nanotube Field-Effect Transistors, in their article "CNTFET-Based Ternary Logic Circuits [1]. CNTFET are characterized by their small size, low power consumption, and high electron mobility, making them potentially valuable for future electronic devices.



(a) (b)

Fig. 2 Designed NAND gates and NOR gates using CNTFETs [1]

They designed NAND gates and NOR gates using CNTFETs with varying diameters, resulting in different threshold voltages, as shown in Fig. 2(a) and Fig.2(b) respectively in the figures.



(a) (b) (c)

Fig. 3 Designed three types of inverters named NTI, STI, and PTI [1]

They also designed three types of inverters named NTI, STI, and PTI, with circuit designs shown in Fig.3(a), Fig.3(b), and Fig.3(c).

The ternary gates discussed above offer versatility for creating ternary arithmetic circuits, including adders and multipliers. To meet the needs of these circuits, a novel ternary decoder design is introduced in Fig.4.

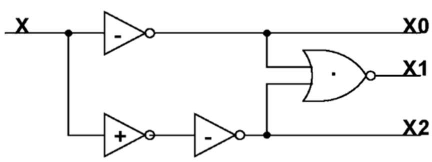


Fig. 4 A novel ternary decoder (Photo/Picture credit: Original)

This decoder generates unary functions from a combinational circuit with one input and three outputs based on input x. The following definition describes the decoder’s output to input x:

$$X_k = 1, \text{ if } x = k \quad (3)$$

$$x_k = -1, \text{ if } x \neq k$$

In this case, k may take the logic values -1, 0 or 1. Figure 4 shows the decoder's component parts, which are a PTI gate, two NTI gates, and a NOR gate. Based on the ternary decoder and ternary logic gates, this paper designed a ternary half-adder as shown in Fig.5.

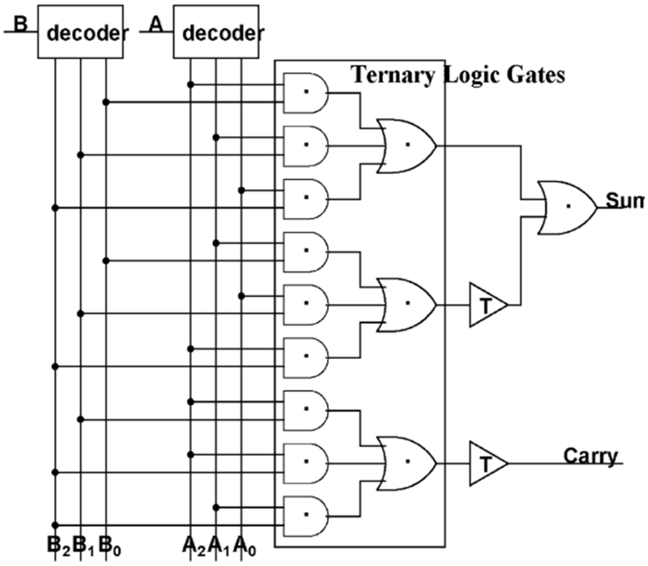


Fig. 5 Ternary half-adder [1]

3. Applications of Ternary Chips in Business and Research

3.1. Research Case Analysis

Adders are a crucial component in chip design, but in most published literature, the design of balanced ternary adders is more complex than binary adders. This paper will reference two simplified design approaches for ternary adders.

3.1.1 Ternary Integrated Circuit Design Using MoS_2

In order to create different ternary logic devices, Mingqiang Huang and his research group have investigated the use of 2D materials including MoS_2 and Black Phosphorus. These gadgets include conventional ternary inverters (STI), adverse ternary inverters (NTI), advantageous ternary inverters (PTI), and an original ternary decrement cycling inverter (DCI) [3]. In addition, they have created a simpler ternary ripple-carry adder, shown in Figure 6. In comparison to current ternary technology, this breakthrough reduces the number of transistors needed by 50%. The improvement of ternary integrated circuits as a result of this study might result in smaller chips with better logic data densities.

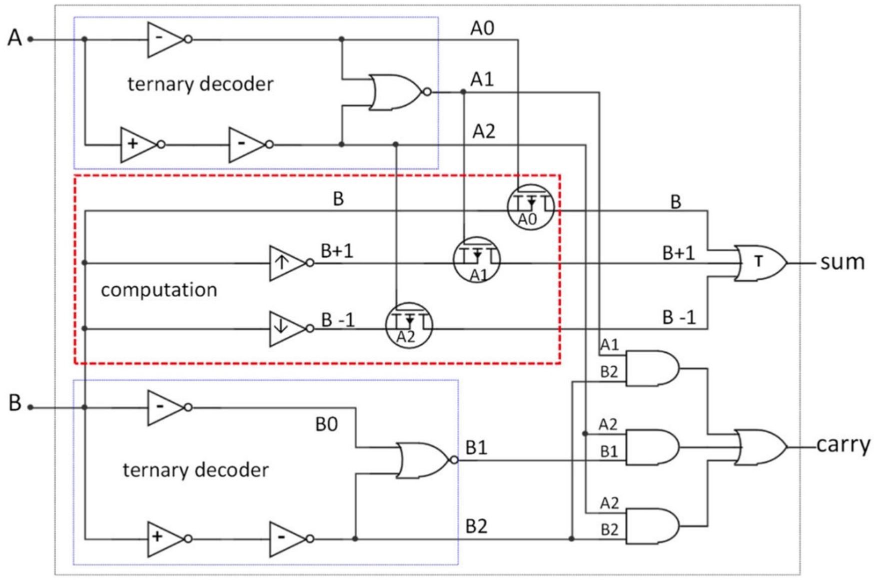


Fig. 6 Simpler ternary ripple-carry adder [3]

Following is a brief summary of the basic principle: 1. The first step produces the variables AB_sum and AB_carry by adding the inputs A and B in half-adder 1 which is depicted by the blue dashed box. 2. In the second phase, half-adder 2 which is depicted by the red dashed box combines the AB_sum and the input carry, Cin. The total sum of A, B, and Cin is shown by the resultant SUM. 3. In the third phase, an OR gate is used to connect the two created carry trits, ABC_carry from half-adder 1 and AB_carry from half-adder 2. The final CARRY, which is used as the new Cin for the future run of complete adders, is produced by this OR gate.

3.1.2 Balanced Ternary Full Adder Design

In a paper by Sunmean Kim and his colleagues, they designed balanced three ternary logic gates: the SUM gate, NCONS gate, and NANY gate, as shown in Fig.6 [5].

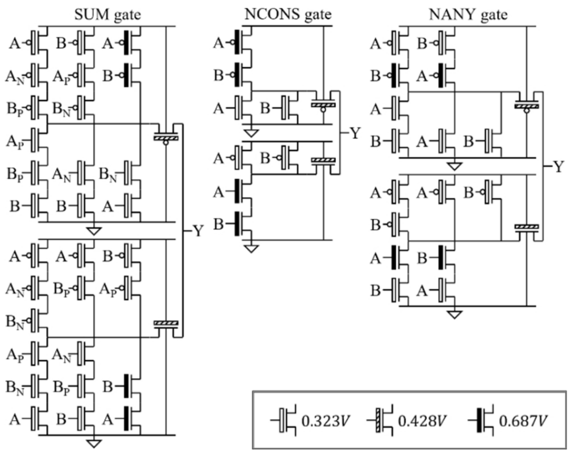


Fig. 7 The SUM gate, NCONS gate, and NANY gate [5]

The balanced ternary full adder consists of two half adders and a NANY gate. Each half adder is composed of an NCONS gate and an SUM gate. The recommended ternary arithmetic logic circuit designs have greatly lowered the average power consumption when compared to older designs. The average power consumption of the ternary half adder and ternary full adder has been significantly reduced in comparison to older versions. This exemplifies the effectiveness of the proposed technique for reducing power consumption in ternary circuit designs.

3.2. Real-world Applications Analysis

S. L. Sobolev conceptualized the idea of creating a portable digital computer called "Setun" in 1956. The goal was to develop a low-cost, easy-to-use computer that could be used in industrial control, research labs, design studios, and educational institutions. At the university's computer center, a group of young engineers and programmers made up of 4 MS and 5 BA graduates came together to work toward this aim. To discuss computer architecture optimization and technical implementation, they held joint seminars in which famous individuals regularly participated [6].

The team created quick components based on tiny ferrite cores and semiconductor diodes in order to overcome problems like the low dependability of vacuum tube-based computer components and the scarcity of transistors. These components served as regulated current transformers and served as a foundation for the use of threshold logic, particularly its ternary variant. Ternary threshold logic components were an appealing option for designing a ternary computer since they outperformed their binary counterparts in terms of speed, dependability, equipment needs, and power consumption.

A sequential computer known as "Setun" achieves performance comparable to parallel devices thanks to its high-speed multiplier. It features a small ferrite RAM that can exchange pages with the primary magnetic drum memory, functioning as a type of cache [7].

"Setun" employs a one-address architecture with a sole index register. The address modification trit's content can be either added to or subtracted from the address segment of an instruction, contingent upon its value (+, 0, -). The instruction set encompasses 24 instructions, encompassing shifts, mantissa normalization designed for floating-point calculations, as well as fused multiplication and addition operations.

In the history of computers, the advent of "Setun" was crucial. "Setun" achieved excellent performance and reliability by utilizing ternary technology and an optimized hardware architecture. It also contributed new concepts and examples to the field of computing.

4. Challenges and Future Development Directions

Balanced ternary currently faces several challenges: 1. Manufacturing: Producing balanced ternary chips requires entirely new processes and materials. Previous research in the field of chips needs to be essentially reinvented [8]. 2. Software Programming: Software programming becomes a significant challenge since ternary chips are fundamentally different from binary. This necessitates the development of assembly and high-level languages designed specifically for ternary systems. The migration of existing software from binary to ternary also raises compatibility issues. 3. Reliability: Balanced ternary introduces an additional zero voltage level, unlike binary, which has only high and low levels. As a result, ternary chips may be more sensitive to electronic interference, demanding advanced technology to achieve high stability.

Ternary chips are expected to play a significant role in deep learning and artificial intelligence in the future, as they offer faster model training due to their three Boolean types [9]. Also, humans will need to develop semiconductors with three states that are suitable for balanced ternary chips, which will greatly improve the efficiency of existing ternary chip designs [10].

5. Summary

This article explores the efficiency and potential of balanced ternary systems in modern computing. Balanced ternary theoretically offers higher efficiency compared to binary systems. Challenges in manufacturing, software programming, and reliability pose obstacles that must be overcome for the widespread application of balanced ternary systems. Addressing these challenges, ternary chips still hold significant advantages in reducing circuit complexity and power consumption, making them an ideal choice for resource-sensitive applications.

The article delves into chip design, introducing balanced ternary logic gates and half-adder designs. It discusses research cases, analyzing innovations in ternary logic circuits and adders, emphasizing potential energy-saving applications. Furthermore, it explores the historical significance of the "Setun" computer, a pioneer in ternary computing. "Setun" exemplifies the possiblity of achieving high performance with balanced ternary systems.

In conclusion, despite the challenges, balanced ternary systems hold great promise in reshaping the future of computing, particularly in resource-efficient applications such as embedded systems and mobile devices. As research in ternary technology advances, it is poised to play a pivotal role in the evolution of computer architecture.

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