

Design of a Crossroad Traffic Light System

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Abstract. Nowadays, the situation of traffic jams is gradually increasing, and the demand for intelligent traffic lights is increasing as well. This paper designs a crossroad traffic light based on sequential logic using NI Multisim 14.0 virtual simulation software. The design includes: using 555 timer to build a second pulse oscillator circuit which outputs clock signal. Using 74LS169 counting chip to build timing circuit. Set up state control with 74LS74D trigger. Using nixie tubes and 74LS47 decoder chips to build the timing display circuit. Finally, logic gate and LED lights are used to build the display circuit of traffic lights. Next, how to design intelligent traffic lights is discussed based on this design combined with image monitoring technology. The feedback bit of image processing technology is added to the designed circuit, so that the circuit can change the green light duration with the traffic flow, and the designed circuits are also becoming smarter.

Keywords: Crossroad traffic light, Sequential logic circuit, NI Multisim 14.0, image processing.

1. Introduction

As the car industry developing rapidly, it's common to see people go out by car. In 21st century, the number of cars increases sharply, and this exerted more and more stress on city transportation. More traffic jams will occur without intelligent traffic coordination system. Traffic jams will cause many adverse effects on society. For example, serious traffic jams will increase the occurrence of traffic accidents [1], which may cause economic losses and even casualties. In addition, traffic jams will pollute the environment. This is because the braking and restarting of cars in traffic jams will emit many harmful substances into the air, and waiting for traffic lights for too long will also cause excessive harmful gas emissions [2]. Therefore, it is very important to use intelligent transportation system to alleviate traffic jams.

In this article, firstly a design of crossroad traffic light will be shown. The whole circuit design was done on NI Multisim 14.0 virtual circuit simulation software. This circuit simulates the traffic conditions of two traffic lanes in a crossroad [3]. The traffic lights on both sides can change from green to yellow, from yellow to red, and finally goes back to green. When the traffic light on one side is green or yellow, the other side is red, so as to manage the traffic of the two traffic lanes in order. Both sets of traffic lights are equipped with two 2-bits digital tubes to display the countdown function. When one digital tube is working, the other digital tube is in the closed state. The circuit can be divided into 5 sections: second pulse circuit, Countdown timer, states control system based on synchronous sequential logic, Timing display circuit, and traffic light display circuit.

After introducing the designed circuit, this paper will discuss about the intelligent traffic lights. Based on understanding the technology of real-time image monitoring, which can monitor number of cars, the further improvement of digital traffic light design in this paper is discussed [4, 5]. The new control bits provided by the image monitoring technology is added to the traffic light control system to make the circuit more intelligent.

2. Traffic Light Design

The diagram of the crossroad traffic lights is shown in Fig. 1.

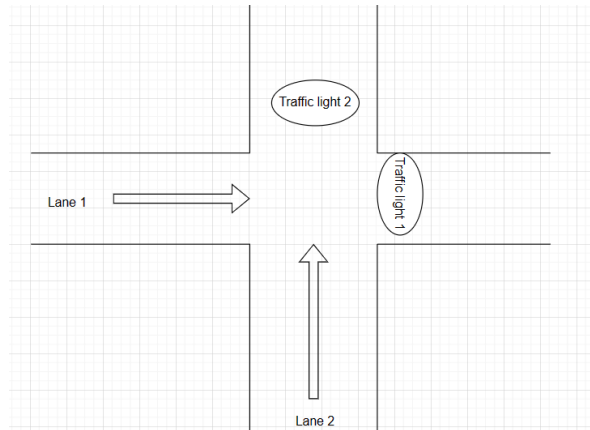


Fig. 1 Illustration of the crossroad.

2.1. Second pulse signal generator

This part is mainly made up of 555 timer chip, and resistor R_1 of $6.8k\ \Omega$, R_2 of $1k\ \Omega$, and capacitor C_1 of $100\mu F$, C_2 of $0.01\mu F$. To generate second pulse signal, the value of outer capacitors and resistors can be changed to control output signal's period. According to the equation, the output signal's pulse period T_{pulse} can be calculated by [6]:

$$T_{pulse} = 0.693 \times (R_2 + 2 \times R_1) \times C_1 \quad (1)$$

The value of R_1 , R_2 , C_1 , and C_2 are decided through weighing between the equation and E series of preferred numbers. Substituting the components' value above into the equation, the output second pulse signal's period is 1.0118s, which can be roughly equal to 1 second. The circuit diagram of the second pulse signal generator is shown in Fig. 2.

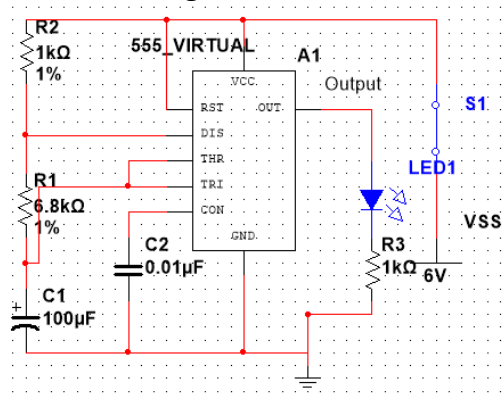


Fig. 2 Second pulse signal generator.

2.2. Countdown timer

This part of the circuit is mainly built of a counter chip 74LS169 which has the function of both counting up and counting down. 74LS169 chip lead 1 is the sequential or reverse counting control end. Lead 2 is the CLK clock input end, which will be connected to second pulse signal. Leads 3 to 6 is the setting end of the counting preset value. Leads 7 and 10 is the stop counting control end. Lead 9 is the control end to activate the preset value. Leads 11 to 14 are the counting output end (lead 11 is the highest position), lead 15 is the counting carry end, leads 8 and pin 16 are the grounding end and the connecting end respectively. The diagram of SN74LS169B chip is shown in Fig. 3.

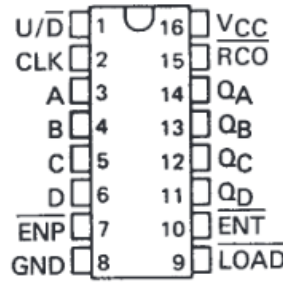


Fig. 3 SN74LS169B [7].

The function table of 74LS169 chip is shown in Table 1.

Table 1. Function table of 74LS169 chip

$\overline{ENT} + \overline{ENP}$	$U / \overline{D}$	$\overline{LOAD}$	CLK	$Q_D Q_C Q_B Q_A$
1	ϕ	1	ϕ	Maintain
0	ϕ	0	Count	Preset
0	1	1	Count	Count up
0	0	1	Count	Count down

This part of the circuit uses two 74LS169 chips U_1 to achieve 30 seconds countdown function. To match the nixie digital display circuit, both chips are set to decimal counting, where U_1 is in the tens and U_2 is in the ones. The input end of the U_1 and U_2 clock CLK is connected in series and connected to second pulse signal to realize synchronous counting function. The preset value of U_1 is set to 0010, so as to countdown from 2. Set the U_2 preset to 1001, thus counting down from 9. The RCO end of U_2 is connected with its own LOAD end to realize the function of reset counting after counting to 0. At the same time, it is connected to the ENP end of U_1 , and the ENT end of U_1 is connected to a high level. Since the RCO end has a low level effective output, the output is always 1 when the countdown count is completed, so that U_1 stops counting. When U_2 (the one digit count) is finished, RCO outputs 0 to reset itself on the next clock rise edge, so that U_1 (the ten digit end) begins to count. The RCO end of U_1 is connected to its own LOAD end, and when the output of $U_1 U_2$ is "00", they resets together. In general, they count from 29 to 0, which is 30 second in total.

2.3. State control circuit

The state control circuit is a synchronous sequential logic circuit composed of D flip-flop. The chip used by the D flip-flop is 74LS74. The characteristic equation of a D flip-flop is [6]:

$$Q^{n+1} = D \quad (2)$$

74LS74 consists of two D flip-flops, lead 1 and lead 7 are clock input terminals. lead 2 and lead 6 are input terminals of two D flip-flops. leads 3 and 5 are low logic level active, so that the D flip-flop output is the preset value. Leads 14 and 8 are the preset value setting terminals of two D flip-flops, and leads 13 and 9 are the output terminals of two D flip-flops. Leads 12 and 10 are the output non-ends of the two D triggers. The diagram of SN74LS74A is shown in Fig. 4.

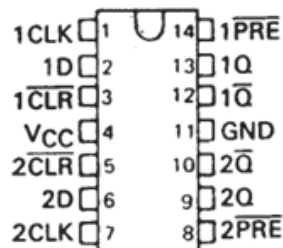


Fig. 4 SN74LS74A [8].

In this design, the overall traffic lights are divided into four states: 00,01,10,11, which are represented by the output of two D triggers.

00 is the green light on traffic light 1 and the red light on traffic light 2.

01 is the yellow light on traffic light 1 and the red light on traffic 2.

11 is a red light for traffic light 1 and a green light for traffic light 2.

10 is red for traffic light 1 and yellow for traffic light 2.

The transition control between states consists of outputs T_1 , T_0 in the countdown timer circuit. T_1 is the “not” logic of the RCO carry end of the counter U_1 . Set $T_1 = \overline{RCO_1}$, that is, T_1 equals to 1 at the end of the 30-second count and 0 at the rest of the time. Set $T_0 = Q_{1A} \times \overline{Q_{1B}} \times \overline{RCO_2}$, that is, T_0 equals to 1 when U_2 carries meanwhile U_1 is 0001. T_0 is 0 in the rest of time, that is, T_0 equals to 1 when counting to “09” in reverse order.

When T_1T_0 is 00, the state does not change.

When T_1T_0 is 01, the state 00 is changed to 01, and the status 11 is changed to 10.

When T_1T_0 is 10, the state 01 is changed to 11, and the state 10 is changed to 00.

When T_1T_0 is 11, it is a irrelevant state.

The state transition diagram of the control system is shown in Fig. 5.

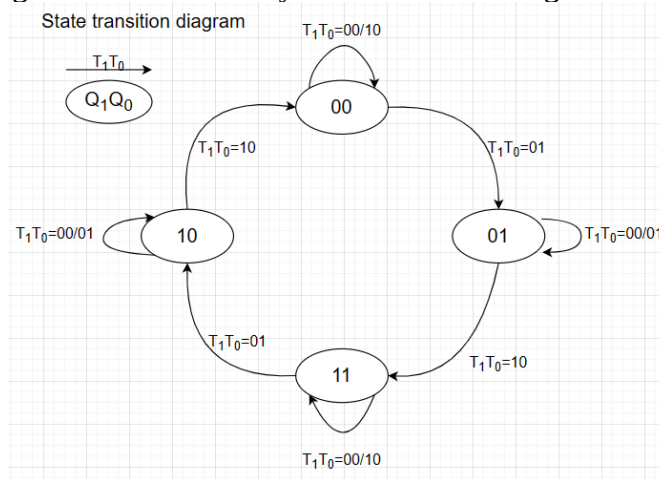


Fig. 5 State transition diagram.

The truth table of the control system is shown in Table 2.

Table 2. Control system’s truth table

Q_1^n	Q_0^n	T_1	T_0	D_1	D_0	Q_1^{n+1}	Q_0^{n+1}
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	0	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	0

After listing the truth table of control system, two input expressions of D flip-flop can be obtained. The expressions are shown in equation (3) and (4).

$$D_1 = Q_1^n \times \overline{T_1} + Q_0^n \times T_1 \quad (3)$$

$$D_0 = Q_0^n \times \overline{T_0} + \overline{Q_1^n} \times T_0 \quad (4)$$

The CLK input of two D-flip-flops is connected with the second pulse signal to form a synchronous sequential logic circuit. When building the control system circuit, several not gates, and gates and or gates are used. The whole circuit realizes the conversion control function of four states of traffic lights.

2.4. Timing display circuits

This circuit is composed of digital tubes and integrated decoders. The digital tubes are a common anode CA type digital tubes, because the output of the decoder is low logic level active. Therefore, the common anode digital tubes are used. Each traffic light is connected with two one-digit digital tubes to display the timing. The tubes represent ten and one digit respectively. The integrated decoders are 74LS47 seven-segment display decoder. Leads 1,2,6,7 are its four-bit input terminal, which can be connected with the four-bit output of the counter chip 74LS169 in countdown timer circuit; The BI side can be used to control the output switch, when the BI input is 0, the decoder output is completely off; When the BI input is 1, the decoder works normally. The lead 3 LT and lead 5 RBI are connected to high logic level signal to ensure that the decoder works normally. The diagram of SN74LS47 is shown in Fig. 6.

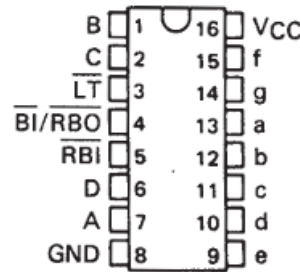


Fig. 6 SN74LS47 [9].

The 9-15 leads of 74LS47 are connected to the a, b, c, d, e, f, g leads of the digital tubes respectively, which realizes the output of the decoder controls the digits displayed by the digital tube. Since the BI terminal can control the decoder on or off, one traffic light's two decoders' BI terminals are connected together. Suppose that two decoders of the first traffic light is Y_1Y_2 , two decoders of the second traffic light is Y_3Y_4 , the BI terminals of Y_1Y_2 are connected to $\overline{Q_1}$, and the BI terminals of Y_3Y_4 are connected to Q_1 . When the system state is 00 or 01, The digital tubes of the first traffic light are working, and the digital tubes of the second traffic light are off. When the system state is 11 or 10, the digital tubes of the first traffic light are closed, and the digital tubes of the second traffic light are working, so as to realize the function of displaying the countdown clock separately in the two traffic lanes. The circuit of countdown timer and timing display circuits is shown Fig. 7.

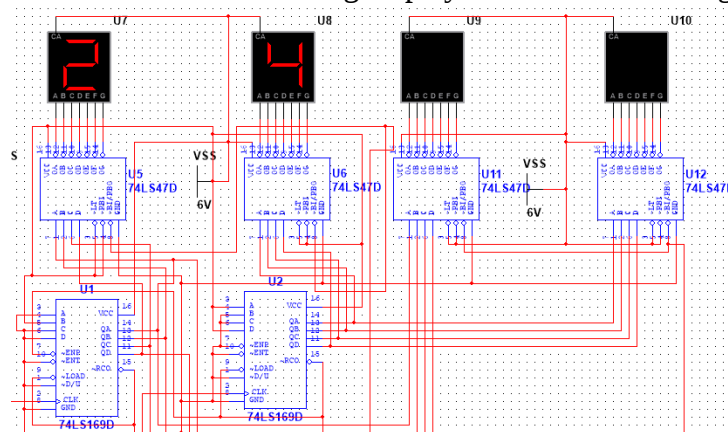


Fig. 7 Countdown timer and timing display circuits.

2.5. Traffic light display circuits

This circuit consists of red, yellow and green LED lights, protection resistors and decoders composed of logic gates. Through listing the truth table of red, yellow, green LED lights and two D flip-flops' output terminals Q_1 and Q_0 , the logical expression of each traffic light can be obtained.

Suppose the three LED lights of the first traffic light are G_1 , Y_1 , R_1 respectively. The three LED lights of the second traffic light are G_2 , Y_2 , R_2 . The truth table is shown in Table 3.

Table 3. Truth table of traffic lights

Q_1	Q_0	G_1	Y_1	R_1	G_2	Y_2	R_2
0	0	1	0	0	0	0	1
0	1	0	1	0	0	0	1
1	1	0	0	1	1	0	0
1	0	0	0	1	0	1	0

According to the truth table, the logic expressions of each LED light can be obtained.

The first traffic light is described by (5)-(7).

$$G_1 = \overline{Q_1} \times \overline{Q_0} \quad (5)$$

$$Y_1 = \overline{Q_1} \times Q_0 \quad (6)$$

$$R_1 = Q_1 \quad (7)$$

The second traffic light is described by (8)-(10).

$$G_2 = Q_1 \times Q_0 \quad (8)$$

$$Y_2 = Q_1 \times \overline{Q_0} \quad (9)$$

$$R_2 = \overline{Q_1} \quad (10)$$

According to the logic expressions, logic gates can be connected as decoders. After connecting the circuit through the logic gates, the decoders' output end are connected to the positive pole of LED lights, and $1k\Omega$ resistors are connected in series at the positive pole of each LED light as protection resistors. Finally, the negative electrode of the LED lights is grounded together. The traffic light display circuits realizes the function of changing two traffic lights to different color with the change of state.

At the end of this topic, the complete diagram of traffic light circuits is shown in Fig. 8.

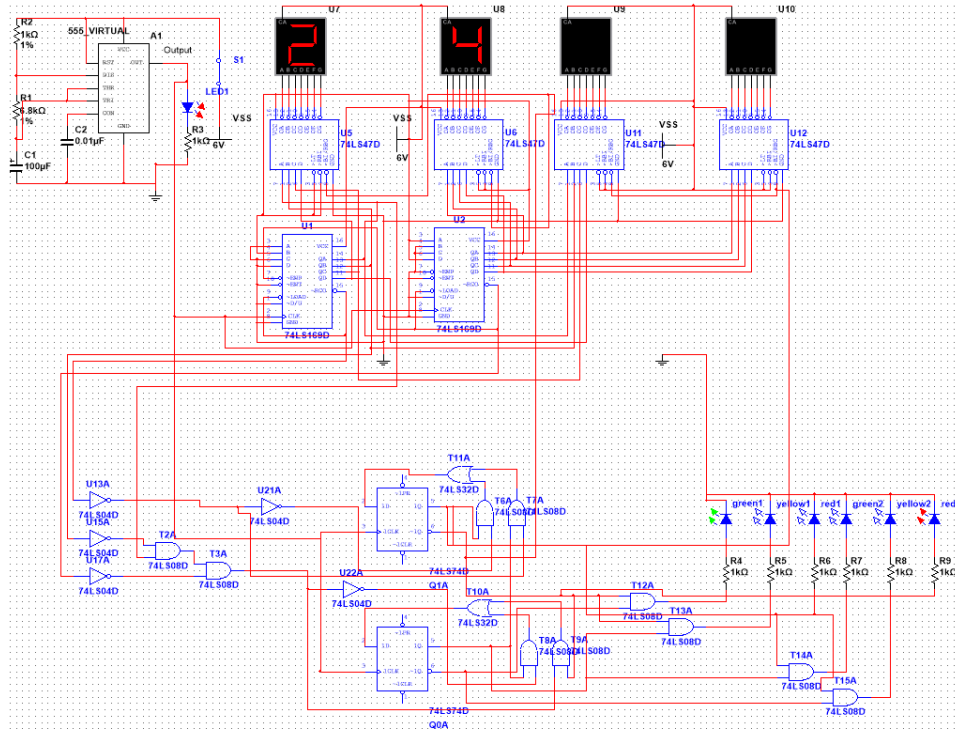


Fig. 8 Complete circuit diagram.

3. Circuit Simulation and Testing

3.1. Second pulse signal output testing

First of all, the second pulse generator circuits provides clock signal for the whole circuits. Therefore, it's very important to know if it is working properly. Whether the second pulse signal output of 555 chip is normal can be known by connecting the lead 3, which is the output terminal of 555 chip, to the oscilloscope to observe the output signal waveform. The output waveform of the second pulse signal is shown in Fig. 9.

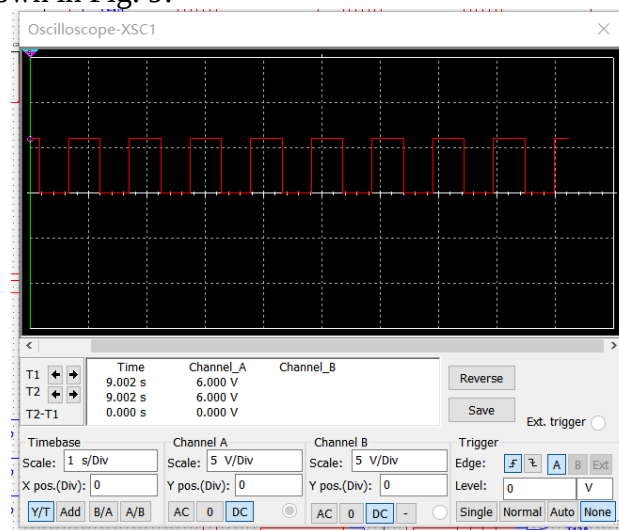


Fig. 9 Second pulse waveform.

As shown above, the second pulse signal generator works successfully. The output pulse signal's period T_{pulse} is close to 1 second. Since in this design T_{pulse} equals to 1.0118 second, the output waveform agrees with the theoretical calculation.

3.2. Timing display and states transition testing

In this part, the working condition of nixie tubes, the countdown timers and LED traffic lights in four different states will all be the test object.

3.2.1 State “00”

The diagram of working condition “00” is shown in Fig. 10.

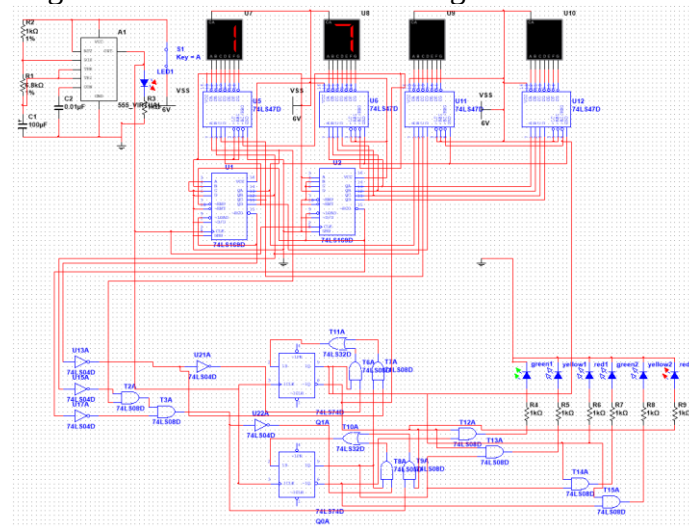


Fig. 10 State “00”.

The "00" state means that the timing is between 29 and 10 seconds and the nixie tubes of the first traffic light are on. In this period, green light is on in traffic light 1, and red light is on in traffic light 2. As shown in the diagram Fig.9 above, the digital tubes and LED lights are all working normally. The second traffic light's digital tube is off, and the first traffic light's digital tube is counting down. Meanwhile, green light of traffic light 1 G_1 and red light of traffic light 2 R_2 are on, and other lights are off.

3.2.2 State “01”

The diagram of working condition “01” is shown in Fig.11.

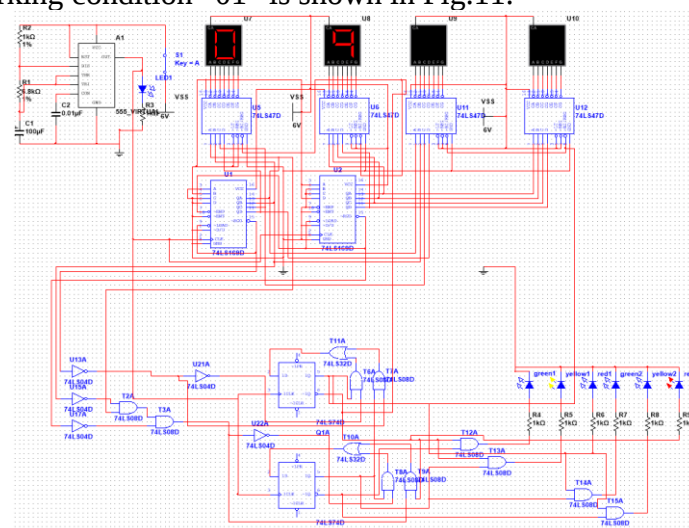


Fig. 11 State “01”.

The “01” state means that timing is between 9 and 0 seconds and the nixie tubes of the second traffic light are on. In this period, yellow light is on in traffic light 1, and traffic light 2 is still red. As shown in the diagram Fig.10 above, both the digital tubes and LED lights are working normally. It’s worth noting that the yellow light in traffic light 1 Y₁ is on when the timing comes to “09”. This

shows that the circuit changes state successfully. The second traffic light's digital tube is off and its red light R_2 is still on. Other lights are still off.

3.2.3 State "11"

The diagram of working condition "11" is shown in Fig. 12.

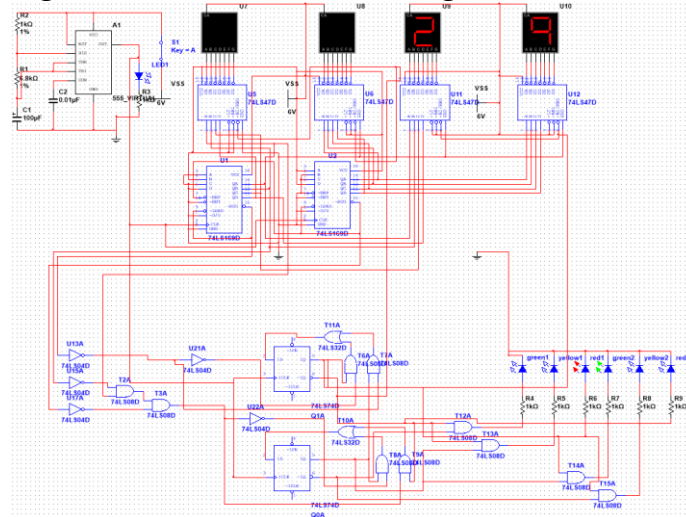


Fig. 12 State "11".

The state "11" is the opposite of state "00". The second traffic light's nixie tubes count from 29 seconds, and the first traffic light's nixie tubes are off. In this state, G_2 and R_1 are on, the rest lights are off. As shown in Fig.11 above, the circuits is working as expected.

3.2.4 State "10"

The diagram of working condition "10" is shown in Fig. 13.

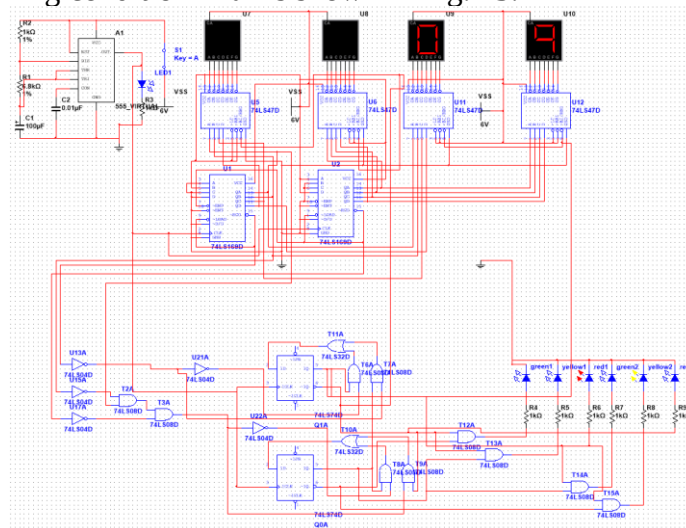


Fig. 13 State "10".

The state "10" is the opposite of state "01". The second traffic light's nixie tubes are counting as the first traffic light's tubes are off. When the timer counts to "09", the second traffic light's yellow light Y_2 is on. The red light R_1 is still on. Other lights are all off. According to Fig. 12 shown above, the circuits is working as expected. When the circuits go to the end of this state, it will go back to state "00" and start again.

4. Intelligent Traffic Light

Nowadays, image monitoring technology is a kind of traffic monitoring technology which is widely used in daily life. Traffic lights on many roads are now equipped with real-time cameras to

monitor traffic. This allows people to know the traffic conditions at any times, which is also beneficial to traffic management.

The image detection technology is to shoot the road through the real-time camera and transmit the obtained picture data to the control system for processing [4]. After comparing the traffic flow of real-time photos with the traffic flow of reference photos, the system feedback the current traffic situation to people [4]. This feedback could be a message or just a high or low level signal. This paper will further improve the intelligence of the circuit by adding the feedback value of the image monitoring system to the state control system of the circuit [10].

Suppose that the feedback bits of traffic light 1 and 2 are F_1 and F_2 . $F=1$ means that there are too many cars and may cause congestion. $F=0$ means that everything is good. Adding F_1 and F_2 into the design circuits' state control system, the improved state transition diagram of the state control system is shown in Fig. 14.

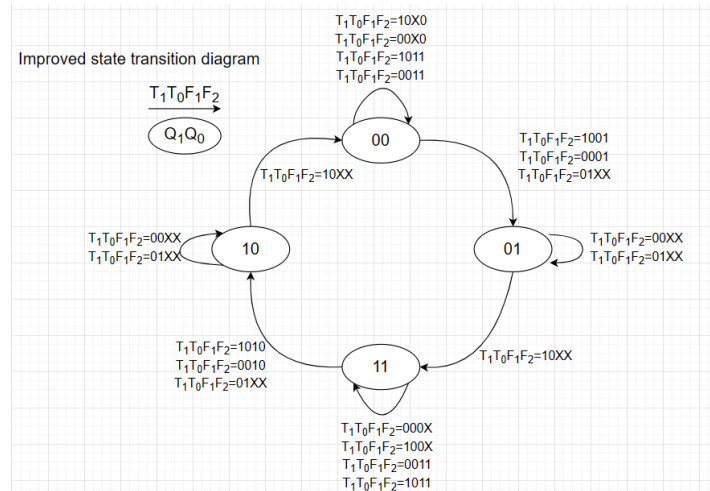


Fig. 14 Improved state transition diagram.

The "X" bits in the diagram indicate that the bit is irrelevant with state transition, either 1 or 0 is OK. The basic idea of the improvement is that when the feedback signal of one road is too many vehicles and the traffic light on that road is red, the traffic light on the other road will immediately change to yellow. It is not affected if the road with too many cars is green. When the traffic light turns yellow, it is not affected, no matter if there is too much traffic on the other road. Finally, if both roads have too many cars, the traffic lights stay still, giving both roads' cars more time to pass.

5. Conclusion

In this paper, the traffic light at the intersection is simulated at first, and a sequential logic traffic light based on 555 chip is designed accordingly. Through the simulation test, the results show that the designed traffic light can jump between red, yellow, green lights and can manage the traffic of two roads. Finally, the design is improved by combining the real-time image monitoring technology, so that it can allocate the green time of the road according to the traffic flow.

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