

Application Research Progress of LDO Chips

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Abstract. LDO chip is one of the key topics in the research of integrated circuits. In response to the demands of portable electronic devices for low power consumption, high integration, and environmental sustainability, the low-voltage linear regulator, exemplified by LDO has stood out. It delivers swift transient response with minimal static current, and boasts a high power supply rejection ratio, all while being cost-effective and featuring a relatively straightforward design. However, in the case of high voltage differences, LDO is less efficient and is not suitable for high-power output applications. Therefore, aiming at the low efficiency of LDO under large pressure differences, the research method of this paper is to analyze the basic principle and performance of LDO chips at home and abroad and propose a design scheme of low voltage difference linear regulator with ultra-low power consumption and wide input range, so as to meet the needs of portable equipment, industrial automation, automotive electronics, communication equipment, and other fields.

Keywords: LDO chip; wide input-low power consumption; integrated circuit field.

1. Introduction

In recent years, China has gradually increased its investment and research intensity in the semiconductor field, but because our industry has been monopolized by foreign giants for a long time, the diversity of product structure is insufficient. There is still a big gap between domestic enterprises and the world's advanced level in a design environment, tools, talents and design experience. Based on China's huge population base and high-speed economic development, downstream demand continues to increase, promoting the rapid rise of China's emerging industries (such as 5G, Internet of Things, artificial intelligence, new energy vehicles, etc) [1]. The development of these industries has spawned a large demand in the fields of big data, cloud computing, and high-speed information transmission, which has promoted the further development of China's power chip industry. In these application scenarios, the power supply typically needs to deliver voltages of 12V or higher. Although DC-DC switching power supplies offer high efficiency, they are prone to output voltage ripple and significant noise [2], potentially causing electromagnetic interference with nearby devices during operation. To mitigate these issues, a commonly adopted approach is to integrate an LDO (Low-Dropout) low-voltage differential linear voltage regulator at the output stage of the switching power supply. This integration ensures a highly stable output voltage, minimizing errors during analog-to-digital (AD) sampling processes. Therefore, in the Internet of Things, biomedical sensors, and other fields, low-voltage differential linear regulators (LDO) are widely used.

Early electronic devices needed to maintain a stable voltage output under different operating conditions to ensure normal circuit operation. With the continuous progress of integrated circuits and semiconductor technology, it is possible to realize efficient voltage stabilization functions inside the chip. The development of LDO technology began with bipolar transistor technology, using NPN Darlington tube or NPN or PNP type power tube [3]. In voltage reduction applications, it can achieve fast response at low input-output voltage differences. In the field of integrated circuits, MOS process, an important semiconductor technology, provides the basis for the realization of high-performance and low-power circuits. The maturity of this control theory technology makes the LDO chip composed of PMOS plus op amp circuit become the mainstream product in the market, and there is more research on this kind of device.

At present, most of the enterprises mainly engaged in analog chips in the foreign market have power management chip product lines, among which the leading enterprises such as Texas

Instruments, NXP, ON and Infineon [4] have launched a variety of types and multi-functional high-voltage LDO products. Due to the structural characteristics of LDO at input high voltage and output low voltage, its conversion efficiency is relatively low [5]. In order to reduce energy consumption and reduce the impact on the environment, it is necessary to reduce the static current during no-load operation.

The continuous improvement and innovation in LDO technology can drive the development of the entire electronic device field, providing fundamental support for the R&D of new electronic products. This paper analyzes the working principle, main performance and key index of LDO, and puts forward a design idea of LDO with wide input and low power consumption. It is capable of better meeting the market demand for low power consumption, high efficiency, and miniaturization, which is conducive to the market promotion and application expansion of electronic products. Therefore, research on wide-input-range low-power linear regulators hold significant importance for both technological advancement and market economic benefits.

2. Basic Principles of Low-voltage Differential Regulator

LDO usually consists of the following five modules: 1) Reference circuit; 2) Error amplifier; 3) Power tube; 4) Feedback resistance network; 5) Auxiliary circuit [6]. As shown in Figure 1. However, modern mobile devices require large-scale integration and fast running speed, which increases the power consumption of internal modules. Al-Shyouke et al [7] further enhanced the transient response by introducing a voltage buffer with adaptive biasing between the error amplifier and the power transistor to increase the slew rate at the gate terminal of the power transistor.

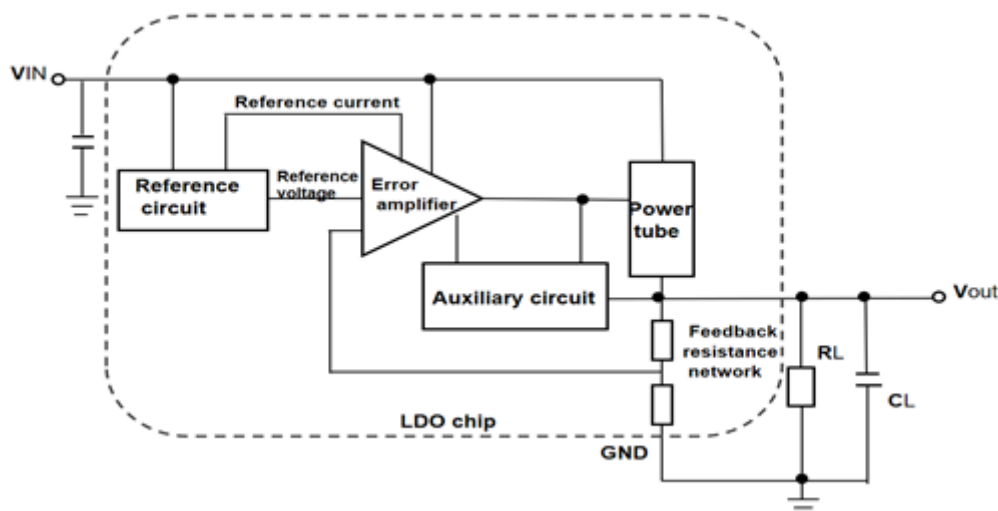


Figure. 1 Internal structure of LDO chip

The reference circuit is the core of LDO, which generates a stable reference voltage and provides a reference for the whole system. The error amplifier is responsible for comparing the output voltage with the reference voltage, amplifying the error signal, and driving the power tube to adjust the output to maintain stability. The power tube is the key component responsible for controlling the voltage and adjusting the output voltage according to the output of the error amplifier. The feedback resistance network is used to adjust the feedback signal to ensure the stability and reliability of the system. The auxiliary circuit provides additional features, such as overload protection and short circuit protection, to ensure that the LDO works properly under a variety of conditions. The LDO chip module generates a stable reference voltage through a reference circuit. A feedback network compares the output voltage with the reference voltage and amplifies any differences through an error amplifier. This amplified error signal then drives the power transistor to maintain a stable output voltage. Auxiliary circuits provide necessary functions such as overload protection and short-circuit protection to ensure the stable operation of the LDO.

During normal operation, as the power supply voltage changes, the gate-source voltage of the power transistor adjusts to keep the output stable. This adjustment is influenced by the difference between the feedback voltage and the reference voltage. The output of the error amplifier regulates the gate-source voltage of the power transistor to ensure that the output remains unaffected by changes in the power supply. When the load changes, variations in the feedback voltage cause the error amplifier to adjust the gate voltage of the power transistor to maintain a stable output voltage. Additionally, the LDO features protection mechanisms that can disconnect the input and output connections in cases of abnormal temperature, output voltage, or power transistor current, ensuring the safety and stability of the circuit system.

3. LDO Classification

According to different application scenarios, the characteristics of LDO have different requirements, which can be generally divided into the following categories: high power LDO, high supply voltage rejection ratio (PSRR) LDO, fast transient response LDO, low static power consumption LDO [3].

Among them, high-power LDOs generally have better stability, lower voltage drops, and higher efficiency, which make them favored in power-sensitive applications. They are widely used in control chips, memory, motherboards, graphics cards or automotive electronics, with a maximum load current of several amps. The high supply voltage rejection ratio (PSRR) type LDO has an excellent high supply voltage rejection ratio. PSRR is the ability of the LDO to suppress the output voltage in the face of the input voltage change. This type of LDO can effectively suppress high-frequency noise and changes in the input power supply, thereby maintaining the stability of the output voltage. PSRR-type LDOs typically perform well in applications that are sensitive to power supply noise, such as audio amplifiers, RF modules, and sensor interfaces. This design usually adopts a special circuit structure and filtering technology to improve the suppression ability of input power supply noise.

For the fast transient response type LDO, most designers choose to use the design feature of no off-chip capacitance. It is able to achieve a stable output without external capacitors and generally offers a more simplified board design and a smaller package size. Researchers from Jiangnan University developed a fast transient response low dropout linear regulator without external capacitors using an operational trans-conductance amplifier (OTA)[8] with high gain and a local common-mode feedback structure (CFRFC). They increased the trans-conductance of the amplifier and boosted its DC gain. At present, the development of most smart electronic devices is limited by battery capacity, so most of them use LDO chips designed with low static power consumption. Reducing the power consumption of LDOs helps to extend battery life, enable device miniaturization, and reduce heat, and is a hot topic for future LDO research.

4. LDO Application

LDO is widely used in a variety of electronic devices in the field of power management, such as smartphones, tablets, wearables, etc, to provide a stable power supply and reduce system power consumption to extend battery life. In integrated circuit design, LDO is often used to provide stable power supply voltage for analog circuits, digital circuits, RF circuits, etc. Its low noise and high-efficiency characteristics make it an ideal choice for integrated circuit design. In the field of communication, LDO is used to provide a stable power supply for RF modules and baseband processors to ensure the normal operation of communication devices. In automotive electronics [9], LDO is widely used in automotive entertainment systems, and body control modules to ensure the stability and reliability of automotive electronic systems. In the field of industrial control, LDO is used in PLC, sensor interface, etc, to provide a stable power supply for industrial control systems and ensure the normal operation of industrial equipment. Based on the understanding of the application requirements of LDO in different fields, designers can optimize the design of LDO to meet the power

management requirements of electronic devices and systems for specific application scenarios. The difficulty in designing wide-input, low-power LDOs lies in their poor circuit stability and slow response speed. To address this challenge, some researchers employ nested Miller compensation and dynamic zero compensation schemes. These methods involve rapidly detecting the voltage overshoot/undershoot of the output to increase the drive current at the gate of the power transistor [10]. Alternatively, other researchers utilize a circuit design technique [11] based on active filtering principles to optimize LDO noise and power supply rejection ratio. This helps reduce loop noise and enhance circuit stability.

When designing a wide-input low-power LDO, several factors need to be considered, including power consumption, stability, efficiency, and application scenarios. Here is an overview of a basic low-power LDO design: First, select an LDO with a low voltage difference to ensure operation under low input voltage conditions. Next, choose the power supply voltage carefully. Then, minimize the output current by utilizing low-power operational amplifiers and resistors to decrease overall circuit power consumption and dynamically adjust the output current. During idle periods, reduce the output current to lower power consumption. Ensure precise reference voltage by employing high-stability reference voltage sources to maintain output voltage stability. Consider using devices with temperature compensation functionality to mitigate the impact of temperature changes on output stability. Additionally, reduce the output capacitance to minimize the effect of load current variations on output stability. Designing control loops is crucial to enhance the system's transient response and adapt to rapid load changes. Improving the power supply rejection ratio (PSRR) is important; proper power filtering capacitors at the LDO input enhance its ability to suppress power supply noise. Entering a low-power mode during device idle times helps reduce overall power consumption. Finally, integrate precise over-current and overheat protection mechanisms to ensure automatic shutdown of the LDO under unsafe operating conditions, safeguarding both the device and the power system.

5. Conclusion

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