

Research On Reducing or Eliminating Body Effects in Amplifier Circuits

Hanxin Zhang *

School of Health Science and Engineering, University of Shanghai for Science and Technology,
Shanghai, Shanghai, China

* Corresponding Author Email: thetoychang@gmail.com

Abstract. When designing common amplifier circuits, the body effect is a factor that cannot be ignored. The main impact of the body effect is to modulate the threshold voltage (V_{th}), thereby affecting the switching characteristics of the device. First, the analog device is introduced, and the structure of the analog device is analyzed. Then the basic principles of the volume effect are introduced. For the problem of body effect, effective solutions are proposed to optimize the working state of transistors and reduce or eliminate the body effect in amplifier circuits. This article aims to deeply explore how to effectively reduce or eliminate body effects in amplifier circuit design to improve circuit stability and performance. First, the article introduces the basic principles of body effect and then proposes a series of methods to eliminate body effect.

Keywords: Body effect; amplifier circuit; MOSFET.

1. Introduction

The quasi-integrated circuit (IC) plays an important role in the design and work of modern circuits. The advent of transistors made it possible to miniaturize circuits. The Complementary Metal-Oxide-Semiconductor (CMOS) device is an important technology in the field of analog circuits. Originally, CMOS technology was applied in the field of digital circuits for the manufacture of low-power, high-integration digital integrated circuits. With the increasing demand for low power consumption and high integration, analog CMOS has been widely used in analog circuit design. Its advantages include low power consumption, low static power consumption, high anti-interference ability, etc. After half a century of continuous development, the development of analog CMOS devices has experienced expansion from digital to analog, from low power consumption to high performance, and from traditional to RF field expansion. This development has enabled analog CMOS technology to be widely used in multiple fields, including communications, healthcare, wearable devices, smart cars, and more.

This paper will summarize the concept of bulk effect by analyzing the structure of each part of the simulator and doing circuit analysis of common amplifying circuits. This study will review the common methods to eliminate or reduce bulk effects at present and take PMOS source followers as an example to analyze the idea of eliminating bulk effects in detail.

2. Transistor

Since the advent of the transistor, the shape has undergone many major changes. Generally speaking, it is from the bipolar type to the unipolar type. Among them, is the unipolar type, from FET to MOSFET. From the structural point of view, from PlanarFET to FinFET, and then to GAAFET. Shockley's Junction Transistor, invented in 1948, is called a Bipolar Junction Transistor (BJT) because it uses both hole and electron carriers to conduct electricity. The working principle of BJT transistors is more complex and is rarely used today. In essence, the main function of this transistor is to make a larger current change at the collector through a small current change at the base, which has an amplification effect. The advantages of BJT transistors are high operating frequency and strong driving ability. However, it also has disadvantages, such as high-power consumption and low integration. Its manufacturing process is also more complex, and the use of

planar technology has some drawbacks. When a JFET transistor works, only one type of carrier is needed, so it is called a unipolar transistor. MOSFET transistor, also known as IGFET (Insulated Gate FET). MOSFET transistors are divided into "N type" and "P type", that is, NMOS and PMOS. According to the type of operation, it can be divided into enhanced type and exhausted type.

In summary, transistors can be divided into bipolar type and single-stage type, of which bipolar type can be divided into bipolar junction (NPN and PNP) two. The unipolar type can be divided into junction-type field effect transistors (JFET) and insulated gate-type field effect transistors (MOSFET). While JFET has a depletion type, MOSFET has a depletion type and an enhanced type.

3. MOS Structure and Bulk Effect

Take NMOS for example. As shown in Fig.1, P-type silicon semiconductor material is used as the substrate, two N-type regions are diffused on its surface, and a layer of silicon dioxide (SiO_2) insulation layer is covered on it. Finally, above the N zone, two holes are made by etching. Three electrodes, G (gate), S (source), and D (drain), are made on the insulation layer and in two holes by means of metalization. The P-type silicon substrate has a terminal (B) connected to the source S by a lead.

The working principle is as follows: Under normal circumstances, a neutral depletion zone is formed between the N region and the substrate P due to the natural recombination of carriers.

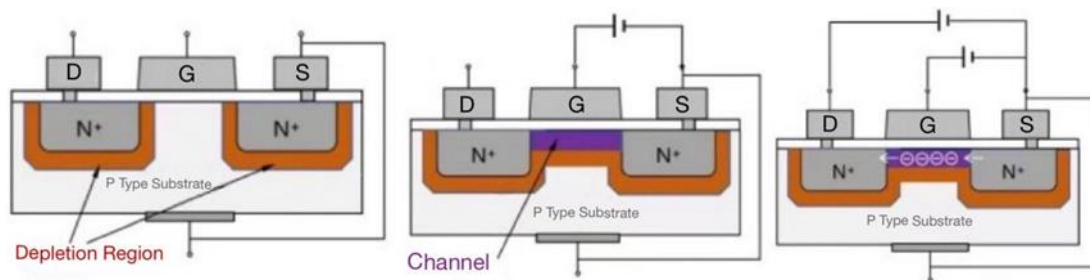


Fig. 1 NMOS Working Principle

After the forward voltage is provided to the gate, the electrons in the P-region will gather under the gate silicon oxide under the action of the electric field, forming a region with many electrons, that is, a channel. If a voltage is applied between the drain and the source, the current will flow freely between the source and the drain, achieving the on-state. The gate G is similar to a gate that controls the voltage. If a voltage is applied to gate G, the gate opens, and current can be passed from source S to drain D. Remove the voltage from the gate, the gate closes, and no current can pass through. In the above process, the gate level voltage corresponding to the formation of the channel is called the threshold voltage (V_{th}). Threshold voltage is one of the key parameters of MOSFET, which has an important effect on the performance and behavior of MOS devices. For example, in terms of power consumption, the change in threshold voltage will also affect power consumption. A lower threshold voltage generally means easier on-off, resulting in greater static power consumption when the MOSFET is on. In some low-power designs, it is important to precisely control the threshold voltage to reduce static power consumption. In terms of noise tolerance, the uncertainty and change of threshold voltage will also affect the noise tolerance of the device. This is an important aspect to consider in analog circuit design. In terms of temperature sensitivity, threshold voltages are usually temperature sensitive. The temperature change may lead to the drift of threshold voltage, so the effect of temperature on device performance should be considered in the design.

When receiving the paper, we assume that the corresponding authors grant us the copyright to use the paper for the book or journal in question. When receiving the paper, we assume that the corresponding authors grant us the copyright to use.

4. MOSFET Body-effects

In analog integrated circuit design, the "body effect" refers to a phenomenon in a metal-oxide-semiconductor field-effect transistor (MOSFET). This effect mainly involves charge transfer and control between the insulated gate and the semiconductor in the field-effect transistor. The main influence of the bulk effect is the modulation threshold voltage (V_{th}), which affects the switching characteristics of the device.

This effect is due to the performance effect caused by the potential difference between the substrate (body) and the source/drain region. Specifically, in MOSFET, the control of the transistor is achieved through the gate voltage. When a voltage is applied to the insulated gate, the gate's electric field affects the electrons and holes in the semiconductor. When a positive voltage is applied to the insulated gate, electrons are attracted to the surface, forming an N-type channel, while holes are pushed deeper. Conversely, when a negative voltage is applied to the insulated gate, the electrons are pushed deeper, and the holes form a P-channel.

In addition to the main influence on threshold voltage (V_{th}), the bulk effect also has different effects and influences on other factors of the device. For example: 1. Causes current leakage. Due to the bulk effect, there will be some current leaking from the source/to the bottom. This current is commonly referred to as bulk leakage current. It can usually be ignored, but in some low-power designs, such as mobile phone chip design, current leakage is a key reference factor. 2. Generate capacitance effect. Volume effects introduce capacitance effects, which have an impact on applications and dynamic circuits. 3. The effect leads to increased temperature sensitivity of the device. With the change in temperature, the device parameters are unstable.

5. Body Effects and Their Defects

In CMOS design, Common Source, Common Drain, and Common Gate are the three common amplifier circuit configurations.

The basic structure is shown in the following fig 2(a) (b)(c):

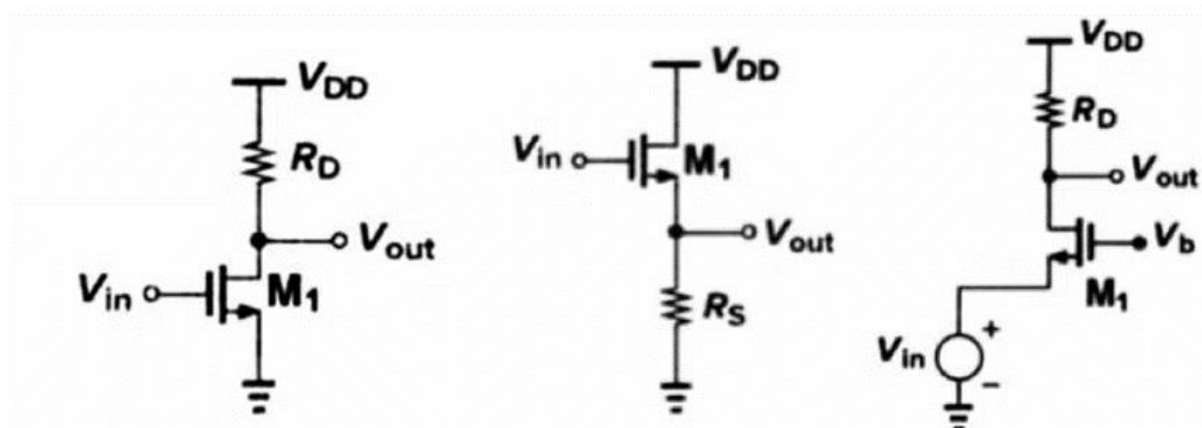


Fig. 2 a) Common Source b) Common Drain c) Common Gate

It is worth noting in the fig that the MOS tube has four terminals, which are the source, drain, gate, and substrate. The substrate pole is generally either connected to GND (NMOS) or V_{DD} (PMOS), so the MOS tube generally has three main terminals.

Table 1 and Table 2 respectively introduce the advantages and disadvantages of these amplifiers and compare their performance. Among them, Table 1 shows the characteristics of the above three amplifiers. In Table 2, the advantages and disadvantages of the above three amplifiers are described.

Table 1. Shows the characteristics of common amplifiers.

	$\lambda=0$ Ignore the channel modulation effect		
	Gain	Input impedance	Output impedance
Common Source	$-gmRD$	∞	RD
Common Drain	$RL/(1/gm + RL)$	∞	$RL/(1/gm)$

Table 2. Comparison of advantages and disadvantages of common amplifiers [1]

	Advantages	Disadvantages
Common Source	High voltage gain High input impedance	High output impedance Phase reversal of the input signal
Common Drain	High input impedance Phase-free inversion High output impedance	Low voltage gain High power consumption
Common Gate	High voltage gain Phase-free inversion Low distortion	Input impedance is low High output impedance

6. Reducing or Eliminating Bulk Effects

In integrated circuit (IC) design, there are some ways to reduce or eliminate bulk effects: 1. N-Well/P-Well design [2]: Use N-Well or P-Well to isolate NMOS (N-Channel MOS) and PMOS (P-Channel MOS) devices to reduce the potential difference between substrates. This reduces the effect of the volume effect. 2. Well-Tie connection: A Well-Tie connection is introduced between N-Well and P-Well to join them together, thus balancing the potential of the two substrates. This helps to reduce the influence of the volume effect on the device. 3. Body-bias technology: Body-bias technology is used to adjust the threshold voltage by applying different voltages to the substrate [3]. This can be achieved by adding additional pins to the device to adjust the overall voltage at run time. 4. Deep well design: In chip manufacturing, the influence of the volume effect is reduced by choosing a deeper well (well) structure. 5. Special processes: Choose to use some special processes specifically designed to reduce the volume effect. This may include high voltage CMOS [4] (HVC MOS) processes or other optimized processes. 6. Power supply voltage adjustment [5]: By adjusting the power supply voltage, it can produce a certain impact on the threshold voltage of the device, thereby reducing the body effect to a certain extent [6]. 7. Temperature compensation: Consider the use of temperature compensation technology to reduce the impact of temperature on device performance.

The following examples illustrate the elimination of the Body effect by PMOS source follower, N-Well/P-Well design, and body-bias technology. The PMOS source follower is taken as an example to analyze the elimination of body effect.

The structure of NMOS and PMOS is as follows: all the NMOS in the existing CMOS integrated circuit process are directly on the substrate (the substrate is P-doped), and the voltage of the source will be different because of the different connection structure of the NMOS at different positions in the circuit. At this time, the substrate is short-circuited with all the sources. So the NMOS is not connected and the source is extremely short-connected.

Fig.3 shows the layout and structure of PMOS and NMOS.

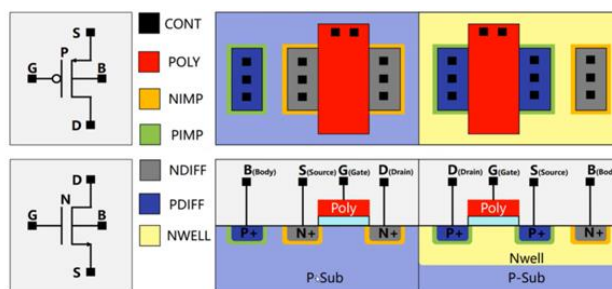


Fig. 3 layout and structure of PMOS and NMOS

The PMOS needs to make an N-well on the substrate first, and then make the structure of the PMOS, so in theory, the N-well of each PMOS can be directly connected with the source pole of each PMOS separately. Therefore, PMOS can eliminate the bulk effect.

In some current processes, there are also special practices to add a deep n well to NMOS, as shown in Fig.4.

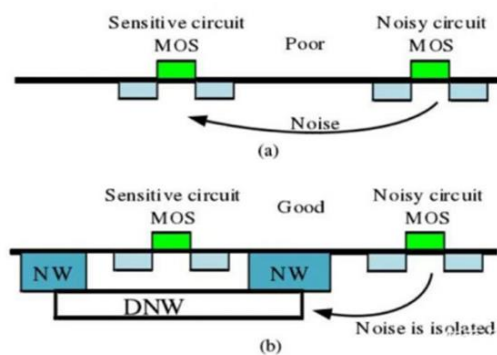


Fig. 4 Deep N Well Principle

Using such a process, the body of the NMOS can be shorted with the Source while ensuring the correct bias of the DNW, thus eliminating its body effect, on the other hand, increasing the DNW can also block the noise crosstalk generated by other MOS in the circuit.

Among the above-mentioned techniques for reducing or eliminating Body effects, the Well-Tie connection and body-bias technique are frequently used in analog integrated circuit design. N-Well and P-Well are regions used to isolate NMOS (N-Channel MOS) and PMOS (P-Channel MOS) devices, where the potential difference between the two Wells causes bulk effects. A Well-Tie connection is usually a way to connect N-Well and P-Well by adding a wire to the chip. This connection is usually implemented at the edge of the chip or other appropriate location.

The functions of the Well-Tie connection include Potential balance: By connecting N-Well and P-Well, the potential difference between the two substrates can be balanced, reducing the influence of the volume effect. Reduce threshold voltage fluctuations: Bulk effects typically cause threshold voltage fluctuations in MOS transistors. The Well-Tie connection helps to reduce this fluctuation and improve device consistency. By providing a more stable substrate potential, the Well-Tie connection helps improve the overall stability of the integrated circuit. The body bias technique is a technique used in integrated circuit (IC) design to adjust the threshold voltage of a field-effect transistor. This technique adjusts the performance of the transistor by introducing a bias voltage to the substrate of the transistor to change the threshold voltage. Body-bias technology is often used to optimize power consumption, performance, and reliability.

There are two common Body-Bias techniques: 1. Positive Body-Bias: A positive voltage is applied to the substrate so that it is corrected relative to the source/drain zone, thereby increasing the threshold voltage. It is commonly used to reduce leakage current, reduce power consumption, and improve the stability of the supply voltage. 2. Negative Body-Bias: A negative voltage is applied to the substrate to make it more negative relative to the source/drain zone, thereby reducing the threshold voltage.

This is often used to increase the switching speed of the transistor and increase performance. Table 3 shows the implementation methods and advantages of the two Body-Bias technologies.

Table 3. Comparison of two Body-Bias techniques

Forward Body-Bias (FBB)	Reverse Body-Bias (RBB)
V _b Increase	V _b decrease
V _{th} reduce	V _{th} rise
Increase the conduction speed	Reduce static power consumption

7. Conclusion

In a MOS FET, the threshold voltage of the transistor determines when the transistor starts to switch on. Thus, the working state of the device is affected. The bulk effect is one of the important factors affecting the threshold voltage. The influence of the bulk effect on the device is not only the influence on the threshold voltage but also restricts the swing of the output voltage in some circuits, resulting in the deterioration of the performance of the device. At the same time, the volume effect may also increase the sensitivity of the device to temperature, because the temperature change of the substrate voltage will cause a change of the threshold voltage, which will affect the performance of the device. Therefore, it is very important to study how to eliminate or reduce the bulk effect for the device.

In this paper, the structure of each part of the simulator is analyzed layer by layer, and the concept of bulk effect is outlined. Then, the circuit analysis is done for common amplifier circuits. Finally, the common methods to eliminate or reduce bulk effects are summarized. When we delve into bulk effects in amplifier circuits, we are not just solving current technical challenges, but exploring new possibilities for future electronic devices. With the continuous progress of science and technology, we are expected to take greater steps in the field of amplifier design. Future developments may involve the exploration of new materials that can more effectively reduce the effects of the bulk effect, thereby improving the performance of amplifier circuits. The exploration of emerging fields such as nanotechnology and quantum technology will also provide us with more tools and methods to further optimize the design of electronic components. In summary, the research on reducing or eliminating bulk effect is not only the solution of current technical problems but also the lead for the development of future electronic technology. By continuing to deepen our understanding of the bulk effect, combined with the application of emerging technologies, we can expect even more outstanding achievements in the field of amplifier circuits, opening up new possibilities for performance improvement and innovation in electronic devices. In the future journey, the development of amplifier circuits will become an important engine to promote the entire field of electronic science and technology.

References

- [1] Zhong Tao, Wang Haocai. CMOS integrated circuit power consumption and low power design optimization technology. Journal of microelectronics, 2000, 030 (002) : 106-112.
- [2] Ezaki.Y, GOI improvement in analog CMOS split gate process,Semiconductor Manufacyuring.2003.
- [3] Hu Rongbin, Wang Yonglu, Zhang Zhengping, et al. A deep submicron CMOS boot-up switch for eliminating contrast bias effect ,2000.
- [4] Cai Chaobo, Jiang Xing, Song Shuxiang, et al. A dual-well CMOS complementary switch for eliminating bulk effect and substrate leakage,2011.
- [5] Duan Jihai, Zhu Zhiyong, Xu Weilin, et al. Bandgap reference source for eliminating bulk effect,2008.
- [6] Duan Jihai, Deng Dongyu, Xu Weilin, et al. A eliminate body effect of nava level all CMOS voltage reference source. Journal of microelectronics and computers, 2015, 32 (7) : 5.