A Study on The Application of PSR In Circuit Design

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Abstract. The power supply rejection ratio (PSR) is an indicator that reflects the sensitivity of a circuit to power supply noise and directly affects the stability and performance performance of the circuit. The aim of this study is to go through the concept of PSR, and the derivation methodology, and to propose a design methodology to enhance PSRR, focusing on the application in the design of stand-alone amplifiers and other circuits. The study uses mathematical derivation and circuit simulation to analyze the effects of different design options on PSRR. Through experimental and theoretical analyses, this paper proposes a series of effective methods to enhance PSRR in stand-alone amplifiers and other circuit designs, including optimizing the power supply line, introducing filters, and adopting suitable power supply decoupling capacitors. The results show that through reasonable circuit design and optimization, the PSRR of the circuits can be significantly enhanced and their resistance to power supply noise can be strengthened, thus improving the stability and performance of the circuits.

Keywords: Power supply rejection, power supply rejection ratio, differential amplifier, common-source amplifier, source follower.

1. Introduction

With the increasing performance and stability requirements of electronic systems, the study and optimization of PSRR have become an important topic in circuit design. In circuit design, Power Supply Rejection (PSR) is an important performance indicator. It reflects the sensitivity of a circuit to power supply noise, i.e., the degree of change in the output of the circuit when the power supply changes. In this study, mathematical derivation and circuit simulation are used to analyze the effect of different design options on PSRR. In amplifier design, a lower PSRR can more effectively suppress the effect of power supply noise on the output signal, thus improving the stability of the amplifier and the purity of the signal. In the design of bandgap reference circuits, the PSR value determines how much noise and fluctuation on the power supply line can be suppressed by the circuit to ensure the stability of the output voltage.

In 2016 Raheleh Hedayati and Luigia Lanni et al. proposed a bandgap reference with a wide temperature range of 25 C to 500C through 4H-SiC technology that provides a stable reference voltage with a minimum temperature coefficient of 46 ppm/C. In 2018 Kamal Jeet Singh and Rajesh Mehra et al. proposed an ultra-low power bandgap reference reference source without resistor and trimming circuitry, using a series MOS tube structure instead of resistors to achieve the benefits of reduced power consumption and area[1].In the design of low dropout regulators (LDOs), which are a common class of power management devices, the reduction of PSR is critical for stabilizing the output voltage, especially in noise-sensitive applications. Such as Avinash Dinesh Shylaja and Gabriel A. Rincón-Mora have mentioned the LDO's regulated output can be used to power noise sensitive Analog loads. PSR measures how much input ripple is suppressed by the LDO[2]. In this paper, we will introduce in detail the concept of PSR, the derivation method, and the methods to enhance PSRR in stand-alone amplifiers and various circuit designs, while emphasizing the importance of simulation verification and theoretical derivation.It will help engineers and designers to better understand and optimize PSRR in practical applications, so as to improve the stability and performance performance of circuits and meet the demand for high-quality power management in modern electronic systems.

2. Introduction and Simulation of PSR

2.1. Power Supply Rejection Ratio and Power Supply Rejection

Power Supply Rejection Ratio (PSRR) is a crucial performance indicator in circuit design, which describes how sensitive a circuit is to power supply noise. In the actual power supply system, power supply noise may have many causes, such as due to the power supply chip used to regulate the voltage of its own output is not particularly stable, there will be ripples appearing [3]. These noises, if not effectively suppressed, will directly affect the output quality and performance of the circuit. In order to solve the problems in terms of its noise and PSRR performance Zhou Qianneng and others[4] referenced a new direction module in the circuit and Alhasssan[5] eliminated the effect of ripples on its output voltage through the structure of negative feedback technique.

PSR is usually expressed in decibels (dB) and is defined as the gain of the output signal relative to the power supply noise. Specifically, PSR can be calculated using the following formula:

$$\mathrm{PSR} = 20 \cdot \log_{10}\left(\frac{\Delta V_{\mathrm{output}}}{\Delta V_{\mathrm{power}}}\right) \tag{1}$$

whereΔVoutput is the change in output voltage andΔVpower is the variation of the supply voltage. Since it is desirable to have as little supply noise as possible present in the circuit, the smaller the value of PSR the better according to the definition of the PSR equation [6].

Power Supply Rejection Ratio (PSR) and Power Supply Rejection Ratio (PSRR) are closely related but slightly different concepts.PSR is primarily concerned with the ability of a circuit to reject power supply noise, whereas PSRR takes a broader view of the relative change between power and ground. The relationship between the two can be understood through proper mathematical derivation and circuit analysis.PSRR is the ratio, that is equal to the gain from the input to the output over the gain from the upper power supply to the output, PSR is directly equal to the gain from the power supply to the output:

$$\mathrm{PSR}=\mathrm{A}=\frac{V_{out}}{V_{dd}} \tag{2}$$

When designing circuits, simulation verification of PSR through simulation software is essential. Through simulation, design engineers can visualize the response of the circuit under different operating conditions and verify whether the design meets the performance requirements of PSR. Meanwhile, the theoretical derivation provides basic theoretical support for the circuit design to ensure the feasibility and stability of the design. By analyzing the common circuits and its small signal model, we can derive the expression of its PSR, which can help us to better study the aspects to reduce the value of PSR when experimenting, and get the circuit with better performance and less affected by noise. Simulation is carried out using cadence and the theoretical and simulated values are compared at low frequencies to find out and validate the ways to reduce the PSR.

2.2. PSR Simulation of Common Circuits

2.2.1 NMOS Differential Amplifier

Common NMOS differential amplifier, by analyzing the small signal model of the circuit, it is not difficult to conclude that at low frequencies the gain of the differential amplifier from VDD to the voltage output is 1. In order to verify the above gain, this NMOS differential amplifier is simulated in Fig 1, where it is assumed that the NMOS tubes are 10 μm wide and 4 μm long and that the PMOS tubes are 10 μm wide and 3 μm long. to simulate the circuit. The input voltage Vin of the circuit is 1.2V, VDD is 3V, and the reference current is 1uA, since the amplification is 1, the current flowing through the M1, M2, Min1 and Min2 tubes is 0.5uA. By analyzing the relationship between Vdsat and Vd of NMOS and PMOS, it can be seen that both NMOS and PMOS are working in saturation regions. The related data can be obtained by simulation as Table 1.

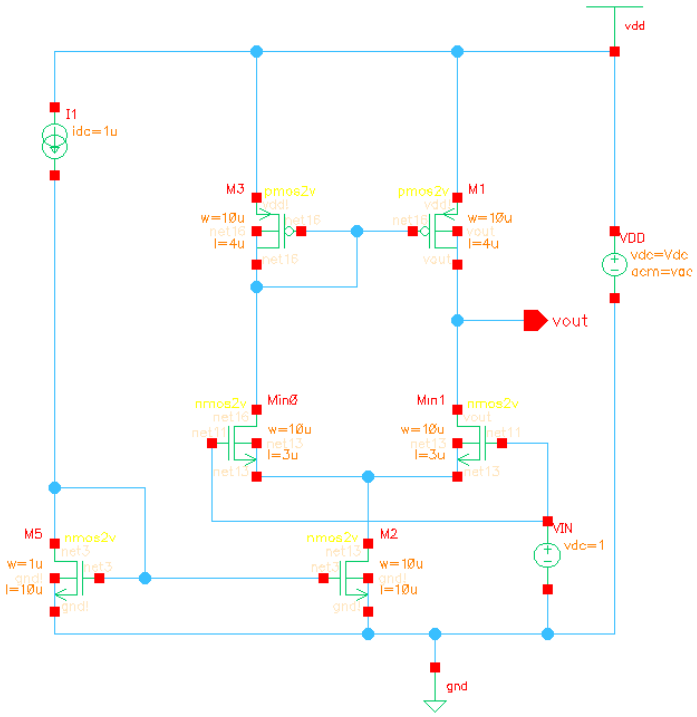

Fig. 1 Simulation of NMOS differential amplifier using Cadence.

Table 1. Cadence simulation of NMOS differential amplifier to obtain g_m, r_o

	W/μm	L/μm	g_m /uS	r_o /MΩ
M1	10	4	38.51	7.65
M2	10	4	38.51	7.65
Min1	10	3	76.44	6.81
Min2	10	3	76.44	6.81

At low frequencies, the PSR of this circuit has a value of 1, which is the same as the theoretical calculation. A gain of 1 at this point is equivalent to the noise at the power supply being replicated at the output and does not suppress the noise at the power supply.

2.2.2 NMOS Common-Source Amplifier

Similarly, for the NMOS common-source amplifier analyzing his small-signal model, an expression for the low-frequency PSR of the circuit is obtained.

$$PSR_2 = \frac{g_{m_1,M_1} + \frac{1}{r_{0,M_1}}}{\frac{1}{r_{0,M_0}} + \frac{1}{r_{0,M_1}}} \tag{3}$$

Using Cadence to simulate the circuit, in Fig2, the circuit input voltage Vin is 500mV, M1 tube gate voltage is 1.5V, V_{DD} for 2.5V, the circuit simulation data as follows Table 2, through the value of g_m , r_o and the PSR value can be calculated through the PSR expression, it is 1.208610, and the simulation of the PSR is 1.208208, it can be seen that the gain of the power supply V to the voltage output is more than 1, then not only the noise on the power supply is not only 1, the gain of the power supply to the voltage output. 1.208208, we can see that the gain from the power supply V_{DD} to the voltage output is greater than 1, at this time, the noise on the power supply is not only not suppressed, but also amplified and transmitted to the output, and the circuit's ability to suppress the noise on the power supply is very poor.

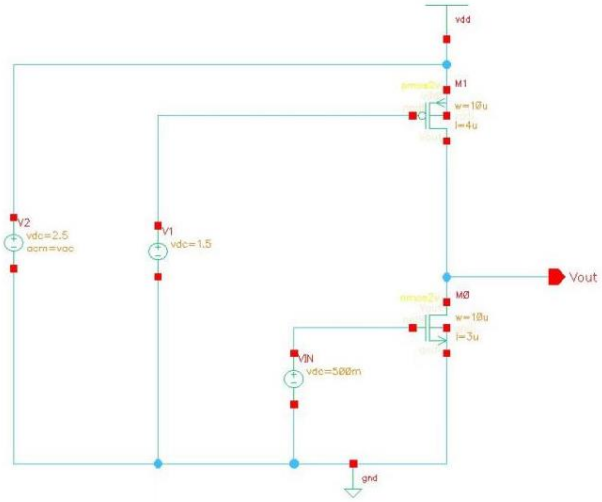

Fig. 2 Simulation of NMOS common-source amplifier using Cadence.

Table 2. Cadence simulation of NMOS common-source amplifier to obtain g_m, r_o

	W/μm	L/μm	g_m /uS	r_o /Ω
M0	10	4	55.58	10.75M
M1	10	3	10.86	19.41K

2.2.3 NMOS Source Follower

For the NMOS differential amplifier, the same analytical small-signal model yields its low-frequency PSR equation:

$$PSR_3 = \frac{\frac{1}{r_{0,M_0}}}{g_{m,M_0}+\frac{1}{r_{0,M_0}}+\frac{1}{r_{0,M_1}}+g_{mb,M_0}} \tag{4}$$

Simulate the NMOS source follower, in Fig3, where V_{DD} is 3V, the gate voltage of M0 is 2V, and the Vin voltage is 600mV. The data obtained from the simulation are shown in Table 3, and the PSR of the NMOS source follower can be obtained from the data in the table and the NMOS source follower formula to be 0.001491. It can be seen that the gain is less than 1 at this time, and the noise at the V_{DD} end is suppressed at the output end, and the power supply noise suppression ability of the circuit is good at this time.

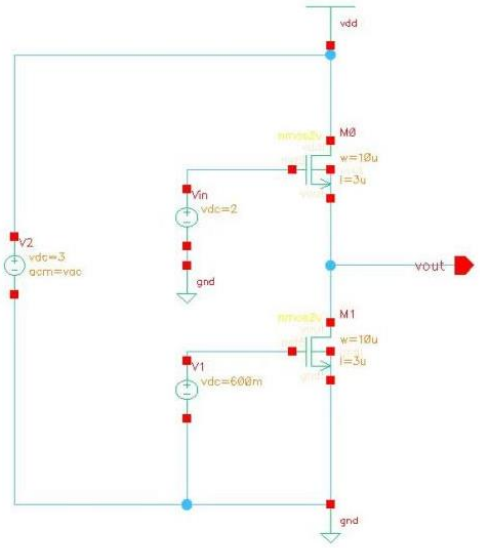

Fig. 3 Simulation of NMOS source follower using Cadence.

Table 3. Cadence simulation of NMOS source follower

	W/μm	L/μm	g_m /uS	g_{mb} /uS	r_o /MΩ
M0	10	3	38.51	34.50	4.16
M1	10	3	38.51	34.48	3.96

2.2.4 Programs to Reduce PSR

For circuits with weak noise rejection, there are schemes that can improve the PSR value of the circuit because the small signal model can be used to derive an equation for the PSR of the circuit, and we can adjust the PSR of the device by using the equation. e.g., for an NMOS source follower we can adjust the transconductance by resizing the MOS tubes, changing the voltage, etc., or by changing the dimensions in order to change the channel length of the MOS tubes, thus affecting the value of r channel length, which affects the value of ro . Theoretically, we can optimize the expression of PSR to reduce the effect of power supply noise on the output.

As can be seen from the simulation, the PSR value of the NMOS common-source amplifier is greater than 1. The power supply noise is amplified at the output and the noise suppression is poor. It can be considered to change the structure of the circuit to try to solve this problem. For example, Lu et al. proposed a new source follower structure to achieve better power supply rejection [7]. increase the equivalent resistance between the power supply terminal VDD to the output terminal, the large resistance can provide a higher voltage divider, this method can effectively improve the power supply rejection characteristics of the amplifier. On the original circuit NMOS common source amplifier, add a resistor between the power supply VDD and the output or add a PMOS for voltage dividing, so as to increase the dividing voltage between the power supply terminal VDD to the output, which can improve the power supply rejection capability of the circuit.

The above conclusions are verified as in Fig4 and Fig5, where the circuit and PMOS are added between the power supply side VDD to the output side of the original circuit and the gain is simulated. The PSR of the circuit in Fig4 is 0.007909, and the PSR of the circuit in Fig5 is 0.821378. It can be seen that, after changing the circuit structure so that the equivalent resistance between the power supply terminal VDD and the output terminal is increased, the value of the PSR of the new circuit is lower than that of the original one, and the original NMOS common-source amplifier has amplified the noise and has poor suppression ability, whereas the new circuit has a PSR of less than 1, and the ability to suppress the power supply noise is better than that of the original circuit. The PSR of the new circuit is less than 1, and the ability to suppress power supply noise is also better than that of the original circuit.

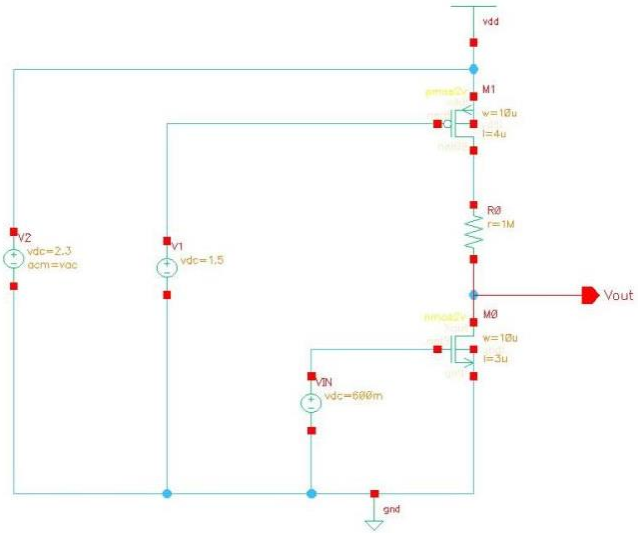

Fig. 4 Adding resistors to improve PSR of the circuit.

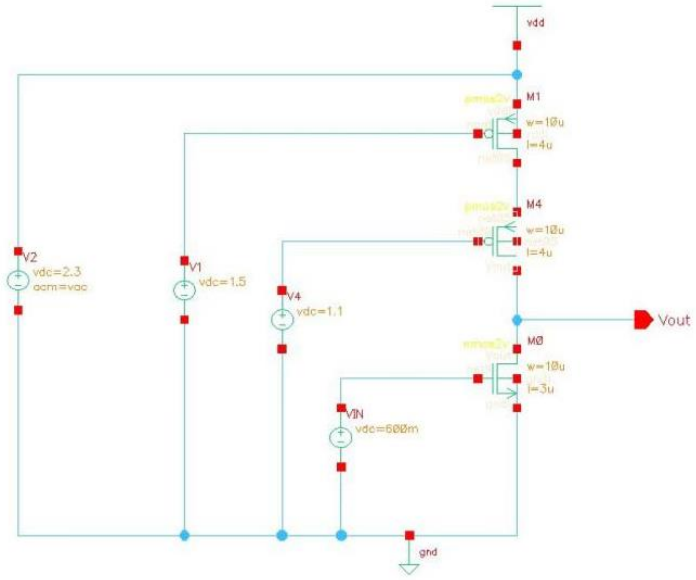

Fig. 5 Adding PMOS tubes to improve PSR of the circuit.

2.3. Methods to Reduce PSR

It is important to reduce PSR in order to minimize sensitivity to power supply noise, reduce power, and simplify the design. The following are some common methods used to reduce the PSR of a circuit:

Reducing the PSR is one of the more critical steps in circuit design. To optimize the PSR, the designer can take a number of steps. First, reduce the value of the coupling capacitor. The coupling capacitor transmits AC signals as well as power supply noise, so reducing its value helps to minimize the extent to which power supply noise propagates into the circuit. Second, reducing the value of the power supply capacitance can also accomplish the corresponding goal. Although the power supply capacitance reduces the transmission of power supply noise, too small a capacitance increases the impedance of the power supply line, thus limiting the propagation of power supply noise and lowering the overall PSR. It is also possible to cut down on a large amount of low-frequency flicker noise by using low-noise BJTs instead of MOS tubes as the operational amplifier input tubes, and to introduce a new feedback loop that suppresses the effect of power supply ripple on the core circuit, obtaining a higher PSRR[8] . Using smaller decoupling capacitors in the selection of decoupling capacitors can reduce the PSRR because smaller capacitance values reduce the sensitivity to power supply noise, but make sure that the signal and noise requirements are fully considered in the design. Single-ended input structures can also be considered. Although a differential input structure can improve PSR, using a single-ended input structure may be more appropriate in certain low-cost applications, especially scenarios that are not sensitive to power supply noise. Therefore, choosing the right input structure in the design is also a strategy to optimize PSR.

In the process of reducing PSR, designers need to make appropriate choices based on specific application needs and system requirements. During the design process, simulation verification and actual testing can provide a better understanding of the impact on PSR after adopting these methods to ensure the validity and reliability of the design.

3. Conclusion

This paper introduces the calculation method of power supply noise suppression, based on the analysis of several common simple circuits and simulation using Cadence, the theoretical PSR calculation and simulation results were compared, from the analysis of the circuit to obtain the PSR expression through theoretical calculations, by analyzing the expression to change the parameters of the device to improve the power supply noise suppression ability of the circuit. Methods. A method to reduce the PSR by changing the circuit structure and increasing the equivalent resistance from the

power supply to the output to improve the power supply rejection capability is also obtained and verified by simulation.

Authors Contribution

All the authors contributed equally and their names were listed in alphabetical order.

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