Characteristics and Improvement Methods of Carbon Nanodevices

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Abstract. Whether the trend of increasing integration density of integrated circuits indicated by Moore's Law can continue to develop, especially now that feature sizes have entered the nanometer range, shrinking sizes face greater challenges. Since entering the "post-Moore" era, the development of carbon-based nanoelectronics has attracted attention. This paper explores the application of carbon-based nanomaterials in carbon-based nanoelectronic devices and integrated circuits. It introduces the structure, properties, and preparation methods of single-walled carbon nanotubes and graphene, demonstrating their importance to carbon-based nanoelectronic devices and integrated circuits. The synthesis methods of carbon nanotubes mainly include arc discharge method, laser ablation method, and chemical vapor deposition metho. Subsequently, it summarizes the advantages, applications, and challenges of carbon-based nanoelectronic devices. The applications of carbon-based nanoelectronic devices and integrated circuits include digital integrated circuits, optoelectronic integrated circuits, electrochemical sensors, carbon-based radio frequency devices, and smart integrated systems. Furthermore, starting from the preparation methods, improvement methods are summarized, focusing on chemical vapor deposition, to optimize carbon nanomaterials for application in carbon nanodevices. It elucidates the promising prospects of carbon-based nanoelectronics.

Keywords: Single-wall carbon nanotube, graphene, carbon nanoelectronic devices, chemical vapor deposition method, micro-nano integrated circuits.

1. Introduction

At the 1991 Very Large Scale Integration (VLSI) Technology Symposium, Masaki Yoshio summarized the development trend of integrated circuits based on Moore's Law proposed by Gordon Moore and typical products of some semiconductor companies, pointing out that the growth rate of memory integration density is four times every three years[1], which is the well-recognized Moore's Law in the world.

Compared with traditional circuits, integrated circuits have smaller size, lighter weight, lower cost, and higher performance. In the context of the information age and the rapid development and popularization of technologies such as 5G communication, the demand and requirements for integrated circuits continue to increase. Silicon-based integrated circuits can no longer meet practical needs. Research has shown that the development prospects of carbon-based nanoelectronics are promising, and the potential of nanoelectronic technology in the "post-Moore" era is limitless. Currently, one-dimensional carbon nanotubes (CNTs) and two-dimensional graphene are the main carbon-based nanomaterials used. In the past, people have been committed to researching various methods for synthesizing structurally controllable carbon nanomaterials and have made a lot of efforts in this regard.

This paper analyzes the application of carbon-based nanomaterials to the development of integrated circuits under the challenges of the post-Moore era. Firstly, it briefly introduces the structure, properties, and preparation methods of single-walled carbon nanotubes and graphene. Secondly, it explores the development of carbon-based nanotechnology and its application in carbon-based nanoelectronic devices and integrated circuits. Then, it summarizes how to improve the preparation methods and optimize carbon nanomaterials to achieve the improvement and development of carbon-based nanoelectronic devices under various challenges.

2. Materials of Carbon Nano-Devices

2.1. Single-Walled Carbon Nanotubes

2.1.1 Structure

Single-walled carbon nanotubes (SWCNTs or SWNTs) consist entirely of carbon atoms, and their geometric structure can be viewed as curled single-layer graphene. In solid physics, it can be represented by the vector C=na_1+na_2, where a_1=a($\frac{\sqrt{3}}{2}$,$\frac{1}{2}$) and a_2=a($\frac{\sqrt{3}}{2}$,-$\frac{1}{2}$).

Because the structure determines the properties, single-walled carbon nanotubes have excellent electronic, mechanical, and mechanical properties. At the same time, according to the curl structure, single-walled carbon nanotubes have three types: armchair, zigzag, and chiral; according to the electronic structure, single-walled carbon nanotubes have semiconductor type and metallic type (including quasi-metallic and metallic). Fig. 1 is the structures of armchair, zig-zag and chiral SWNTs.

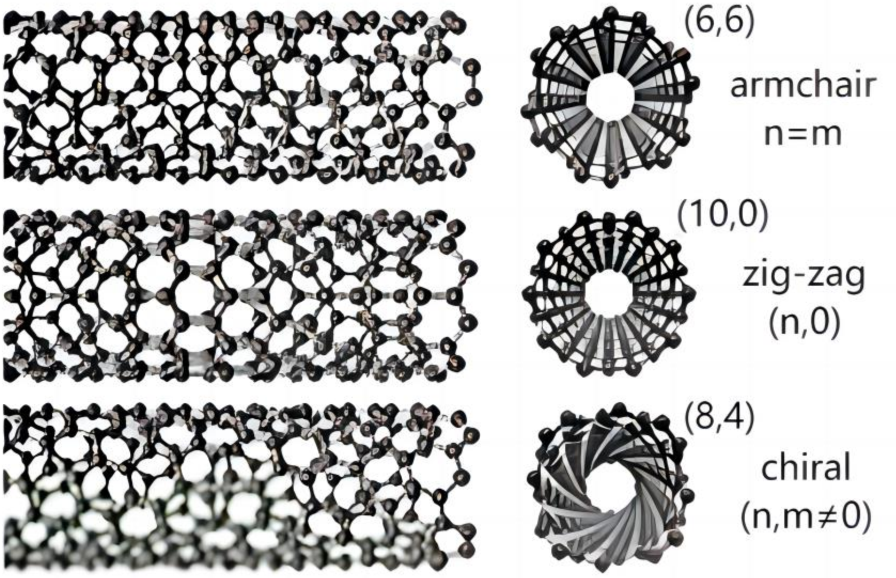

Fig. 1 The structures of armchair, zig-zag and chiral SWNTs [2].

2.1.2 Properties

The unique band structure of carbon nanotubes gives them special electrical and optical properties.

The properties of metallic carbon nanotubes are similar to graphene . At room temperature, the conductivity can reach 4e2/h, close to the quantum conductivity[3]. Moreover, metallic single-walled carbon nanotubes can carry a current density of up to 109 A·cm^{-2}, which is 1000 times that of traditional copper wires and can be used as interconnects between devices to achieve smaller integrated circuits [4].

Semiconductor-type carbon nanotubes have ultra-high carrier mobility (>105 cm^{2}·V^{-1}·s^{-1}) [5]. Due to the one-dimensional quantum confinement effect of carbon nanotubes, resulting in a low scattering probability of carriers. The average free path is high. The surface of semiconductor-type carbon nanotubes has no dangling bonds, so the probability of surface scattering and interface scattering of carriers during transmission is low. And the metal electrodes will not produce Fermi pinning on the surface of carbon nanotubes, making it possible to form good Ohmic contacts between them[2].

In addition, n-type transistors and p-type transistors have matched high performance because the conduction band and valence band of carbon nanotubes are symmetric, and the effective masses of electrons and holes are equal. This makes Complementary Metal Oxide Semiconductor (CMOS) integrated circuits perform excellently [6]. s-SWNT is a direct bandgap semiconductor material, so its absorption and luminescence efficiency are much better than silicon materials. Moreover, it has a natural one-dimensional structure, so the exciton binding energy is large, about 0.4−0.5 eV, so carbon nanotubes also have the potential to play a role in optoelectronic applications.

2.1.3 Preparation

The synthesis methods of carbon nanotubes mainly include arc discharge method, laser ablation method, and chemical vapor deposition method (CVD).

Arc discharge is essentially a gas discharge phenomenon, which requires using a higher temperature to allow carbon atoms to evaporate and become plasma, that is, under certain conditions, making the gas space between two electrodes conductive, converting electrical energy into heat and light energy.

The laser vaporization method involves placing a target made of metal catalyst/graphite powder mixture inside a quartz tube reactor, which is then positioned within a horizontal furnace. At a certain temperature, inert gas is introduced, and the target is heated using a laser beam. Under laser irradiation, solid carbon source generates gaseous carbon, which, catalyzed by the catalyst, grows into single-walled carbon nanotubes, eventually condensed in the carrier gas flow.

CVD method operates within the temperature range of 600-1100 ℃, where carbon-containing compounds decompose on catalytic nanoparticles to provide a carbon source for the growth of carbon nanotubes. Due to its lower growth temperature and easy-to-control parameters, CVD has demonstrated superiority in the controlled preparation of carbon nanotubes.

2.2. Graphene

2.2.1 Structure

Graphene, as a single atomic layer two-dimensional crystal, involves an electron in a 2s orbital transitioning to the $2p_z$ orbital, while another electron in 2s forms three σ bonds with electrons in $2p_x$ and $2p_y$ through sp^2 hybridization. Each carbon atom combines with three neighboring carbon atoms within the plane, forming three equivalent σ bonds, thus, the angles between these bonds in the plane are 120°. The $2p_z$ electrons form π bonds perpendicular to the plane. In graphene, carbon atoms are connected through sp^2 hybridization with adjacent carbon atoms via σ bonds, forming a regular hexagonal structure with a carbon-carbon bond length of approximately 0.142 nm and a thickness of approximately 0.35 nm for a single layer of graphene [7].

2.2.2 Properties

Graphene is a typical zero-bandgap semimetal material, with its electron energy spectrum showing a linear relationship between energy and momentum, known as Dirac fermion characteristic at a certain point K (K'). Near the Dirac point, the static effective mass of electrons is zero, typical of Dirac fermions, with Fermi energy velocity reaching up to 10^6 $m \cdot s^{-1}$, which is 1/300 of the speed of light [7]. Furthermore, electron wave transport in graphene is confined within a thickness of a single atomic layer, exhibiting characteristics of a two-dimensional electron gas. Finally, the carrier concentration and polarity of graphene can be effectively controlled through doping methods, commonly using atomic substitution doping and surface doping, both of which can yield high carrier concentrations of n-type or p-type graphene.

2.2.3 Preparation

Methods for preparing graphene mainly include mechanical exfoliation, SiC epitaxial growth, CVD, and reduction of graphene oxide.

Mechanical exfoliation involves mechanically peeling graphene layers from fresh graphite crystals and transferring them onto a substrate to obtain graphene.

Epitaxial growth on SiC is a method to prepare single-crystal graphene on a single-crystal substrate. The basic principle involves high-temperature treatment of silicon carbide, evaporating silicon atoms from silicon carbide, allowing the remaining carbon atoms to undergo structural rearrangement, thus forming graphene.

The basic principle of chemical reduction involves treating graphite in solution with strong acids to form graphite intercalation compounds, then adding strong oxidants to oxidize it, introducing oxygen-containing functional groups on the graphene surface to obtain dispersible graphene oxide, and finally reducing it through various methods to obtain graphene with different sheet sizes and dispersions.

CVD utilizes carbon-containing compounds such as methane as carbon sources, which decompose on the substrate surface at high temperatures to grow graphene. From the perspective of growth mechanism, it mainly includes carbon diffusion and surface growth mechanisms. Table 1 is the comparison of the four preparation methods of graphene.

Table 1.Comparison of the four preparation methods of graphene.

Production Methods	Product Dimensions	Product Quality	Manufacturing Costs	Suitability for mass production
mechanical exfoliation	Medium /small	Molecular structural integrity	low	no
SiC epitaxial growth	large	Flakes are not easily separated from SiC	high	Suitable for small batch production
reduction of graphene oxide	large	The molecular structure is easily destroyed	low	yes
Chemical Vapor Deposition	large	Structural integrity and better quality	high	yes

3. Carbon-Based Nanoelectronic Devices

3.1. Advantage

Based on current research on carbon-based nanoelectronic devices, their technical advantages can be summarized in the following five aspects:

The technique has a relatively high efficacy. Carbon nanotubes are one-dimensional quantum materials, characterized by lightweight, small capacitance, high thermal stability, large specific surface area, and high carrier mobility. Devices based on carbon nanotubes exhibit higher comprehensive performance. Compared to traditional electronic devices, the performance-power consumption advantage can reach 5 times or more. In the field of integrated circuits, the theoretical performance-power consumption advantage can reach 50 times or more [8].

The technique is highly adaptable. Carbon-based nanomaterials possess strong radiation resistance and thermal stability, allowing stable operation in environments with high radiation intensity or large temperature variations. Carbon-based nanoelectronic devices demonstrate strong environmental adaptability. Research has found that carbon-based chips can withstand irradiation of 9 Mrad and operate normally in environments ranging from -273°C to 130°C [8].

This technique has a relatively high performance. Researchers can utilize carbon-based nanotechnology to manufacture electronically diverse devices to meet various application demands of carbon-based nanoelectronic devices in different scenarios, such as transparent electronic chips, transient electronic chips, sensing devices, analog circuit devices, and logic control circuit devices.

The technique has a relatively short process flow. When producing carbon-based nanoelectronic devices, simple processes can be employed to prepare highly efficient devices in a short time. For example, using traditional integrated circuit production equipment and simple processing techniques can produce carbon-based integrated circuits with equivalent or even higher efficiency within a general process flow.

This technique has a relatively high heterogeneous integration performance. Carbon-based nanomaterials and related devices can overcome obstacles such as temperature and energy consumption in the preparation of 3D heterogeneous integrated circuits. The effective application of carbon-based nanoelectronic devices is conducive to realizing 3D integrated circuits.

3.2. Applications

With the continuous improvement of carbon-based nanoelectronic device and integrated circuit technology and deepening understanding of their working principles, their application scope is expanding, and their application value is increasing. The applications of carbon-based nanoelectronic devices and integrated circuits include digital integrated circuits, optoelectronic integrated circuits, electrochemical sensors, carbon-based radio frequency devices, and smart integrated systems.

Digital integrated circuits are widely used in information systems and are electronic components for digital signal processing based on digital logic design. According to their scale, they can be divided into Small-Scale Integration (SSI) circuits, Middle-Scale Integration (MSI) circuits, Large-Scale Integration (LSI) circuits, Ultra-Large-Scale Integration (ULSI) circuits, and Grand-Scale Integration (GSI) circuits.

Optoelectronic integrated circuits are electronic devices that integrate optical functional devices and electronic functional devices on a single chip or incorporate integrated optoelectronic components into circuits to form electronic devices. Carbon-based nanomaterials have excellent optical properties. For carbon nanotubes, they are direct bandgap semiconductors, capable of producing high-performance electroluminescent and photoluminescent devices, meeting the requirements of optoelectronic integrated circuits.

3.3. Challenges

Firstly, performance challenges: Although carbon-based nanoelectronic devices demonstrate strong environmental adaptability, they are susceptible to changes in performance under unsealed conditions, which may reduce the stability, reliability, and safety of carbon-based nanoelectronic devices. However, integrated circuits, especially large-scale and ultra-large-scale integrated circuit systems, have high requirements for uniformity. The currently mastered carbon-based nanoelectronic integrated circuit technology cannot well balance all the performance requirements of integrated circuits, and the uniformity of carbon-based nanoelectronic integrated circuits is restricted.

Next is the cost challenge. The key to the preparation of carbon-based nanoelectronic devices and integrated circuits lies in the preparation of carbon nanotube array films. Currently, the purification rate of carbon nanotube solution can reach over 99.9999%, and the density can reach approximately 100-200 tubes/μm[9], which basically meets the requirements of large-scale integrated circuits. However, to achieve stable and high-efficiency ultra-large-scale integrated circuits, the purity of carbon nanotube solution needs to be further increased by 2 to 3 levels. In terms of current processes, achieving this requirement requires higher costs and more time investment .

Finally, there is the challenge of standards. Different electronic devices or integrated circuits have different requirements for carbon-based nanomaterials. In order to promote the stable, healthy, and long-term development of carbon-based nanoelectronic devices and integrated circuits, it is necessary to strengthen the establishment of relevant standards. Examples include standards for the purity of carbon nanotube semiconductors, the length distribution of carbon nanotubes, and the selection of integrated circuit substrate materials [8].

4. Improvement and Prospects of Carbon Nanoelectronic Devices

4.1. Optimized CVD Method

The Advanced Carbon Materials Research Department of the Institute of Metals, Chinese Academy of Sciences, led by Sun Dongming and Liu Chang, proposed a continuous synthesis, deposition, and transfer technique for SWCNT films, realizing the continuous preparation of high-quality SWCNT films with millimeter-scale dimensions. Based on this, they constructed high-performance all-carbon thin-film transistors (TFTs) and integrated circuit (IC) devices. Researchers used the floating catalyst chemical vapor deposition method to continuously grow SWCNTs in the high-temperature zone of the reactor. Then, through gas-phase filtration and transfer systems, the prepared carbon nanotubes were collected at room temperature and transferred to flexible PET substrates by roll-to-roll transfer, obtaining SWCNT films with lengths exceeding 2 meters. Fluid simulation of the filtration deposition process showed that when adjusting the outlet speed to achieve equilibrium during the filtration process, the airflow in the filtration system exhibited a uniform airflow velocity distribution. SWCNT films prepared by this method exhibited excellent optoelectronic properties and uniformity, with a transmittance of 90% at a wavelength of 550 nm and a sheet resistance of 65 Ω. Researchers used the prepared SWCNT films to construct high-performance all-carbon flexible transparent transistors as well as flexible all-carbon integrated circuits such as XOR gates and 101-stage ring oscillators [10].

Birrell et al. conducted optimized research on the CVD method and successfully prepared high-quality monolayer graphene using this method. The optimized experimental process first chemically polished and pretreated copper foil for 8 minutes and annealed it in a protective gas atmosphere. Then, the copper foil was processed into a purse shape. In a hydrogen atmosphere, using methane as the carbon source, chemical vapor deposition was performed. When the methane and hydrogen flow rates were 10 cm^3/min and 20 cm^3/min, respectively, the growth was carried out for 20 minutes at 1030 °C. The pretreatment of the copper foil effectively improved the surface properties of the substrate, facilitating the uniform nucleation and growth of graphene. The use of purse-shaped copper foil substrates effectively improved the flow state of the gas in the growth chamber, facilitating the uniform growth of graphene. Appropriate gas flow rate, growth temperature, and growth time were conducive to the growth of structurally complete graphene products. Results characterized by scanning electron microscopy and Raman spectroscopy showed that the samples prepared by this method were large-area continuous monolayer graphene, laying the foundation for further preparation and research of graphene micro nano electronic and sensor devices [11].

4.2. Prospects and Outlook

In the post-Moore era, Si-based CMOS technology is steadily advancing by scaling down proportionally, and the chip integration density has reached hundreds of billions of transistors. Currently, in the bottom-up development route, molecular electronics, carbon-based nanoelectronics have emerged, achieving significant breakthroughs in scientific research after more than twenty years of development. A landmark achievement in the development of one-dimensional carbon nanotubes in nanoelectronics is the alignment of CNT arrays with a purity greater than 99.9999%, a density of 100-200 CNT/μm, and the integration of 14,000 transistors in a 32-bit CPU, and the application of Si CMOS technology for 3D integration. Two-dimensional graphene also has new progress in RF flexible electronics, with a strain limit of 2.0% for GFETs, intrinsic f_t of 95 GHz, and f_{max} of 28 GHz [12].

There is still a significant gap between carbon-based nanoelectronics and Si-based nanoelectronics in terms of integration density. To address this, new architectures such as "chiplet" and 3D integration complementary to Si CMOS technology may be adopted, or efforts may continue to overcome the semiconductor CNT purity issues that constrain its integration density development. In summary, carbon-based nanoelectronics still have a long development stage before becoming a substitute for Si-based nanoelectronics.

5. Conclusion

Although it is unlikely that Moore's Law will continue indefinitely, efforts can be made to extend its duration as long as possible. The significance of carbon nanomaterials for carbon-based electronic devices was discussed, and single-walled carbon nanotubes and graphene were introduced, analyzing carbon-based nanotechnology. For carbon nanomaterials, this paper summarized improved preparation methods to produce superior carbon nanomaterials. However, under various challenges, there is still significant room for the application of carbon nanomaterials in carbon-based electronic devices and integrated circuits. The rise of carbon-based nanomaterials provides more possibilities for the development of integrated circuits and chip industries. In the future, researchers should focus on addressing the aforementioned deficiencies, overcoming performance challenges, reducing production costs, and standardizing processes and device standards.

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