Design Of a High Gain Three-Stage CMOS Operational Amplifier for EEG Signal Processing

Siyuan Feng *

College of Electronics and Information Engineer, Shanghai University of Electric Power, Shanghai, 201306, China

* Corresponding Author Email: fengsiyuan@mail.shiep.edu.cn

Abstract. Recently, research on brain science has led to rapid development in Electroencephalography (EEG) signal processing. However, it is really hard to capture, amplify and measure the EEG signals from the human brain during the signal acquisition and amplification. Therefore, this paper introduces a newly-designed high gain three-stage CMOS operational amplifier to measure and amplify the EEG signals precisely. The main circuit structure is built in CoolSpice with the TSMC 0.18um CMOS technology. During the simulation in CoolSpice, the open-loop DC gain reaches to 90.04dB and its power consumption is around 19.8 mW. With the help of the frequency compensation applied in the circuit, the bandwidth of the op-amp achieves to 363Hz, which is able to amplify all sorts of EEG signals and measure them, and the phase margin with the value of 177 degrees, making the circuit system stable. This three-stage op-amp makes its circuit system stable and avoids the unnecessary oscillations during the EEG signal amplification, which lead to a precise measurement on EEG signals and provide the precise diagnosis for the patients.

Keywords: EEG signal; signal amplification; CMOS operational amplifier; open-loop DC gain; frequency compensation.

1. Introduction

Electroencephalography (EEG) measures the electrical activity of the human brain through potentials. It is an objective method that provides valuable insights into brain function [1]. In recent years, research on brain science has led to rapid development in EEG signal processing technology. For instance, EEG signal processing has a wide range of applications in the field of clinical medicine, including the diagnosis of brain disorders such as epilepsy or brain tumor and the monitor which supervises the sleep state of a patient. EEG signal processing technology has been also applied in the recent advances in an integrated circuit for the field of brain-computer interface, which gives a possibility for patients to control the mouse on the screen by using their thoughts. However, it is difficult to capture the EEG signals from the human brain. One of the reasons is that during Amplification in EEG signal pre-processing, the interferences from noises (e.g. noises inside a human body) causes distortion of the EEG signals and affects the quality of them, so that some errors remain in the measurement of the EEG signals, which lead to the incorrect diagnosis for the patients. In order to solve this difficulty, a high-gain three-stage CMOS op-amp using the topology of nested Miller compensation using nulling resistor (NMCNR) is designed for EEG signal processing.

Section 2 simply describes the basic characteristics of EEG signals and the simple principle of EEG signal processing. Meanwhile, by describing the pre-processing of EEG signals in detail, the essential role of amplification during the signal processing is vitally emphasized. Section 3 mainly introduces the design of an open-loop three-stage CMOS operational amplifier for amplifying EEG signals and its main structure and principles. Then the different methods for frequency compensation mainly used in the three-stage operational amplifier are introduced. The best frequency compensation method is selected through circuit simulation and applied in this amplifier. Finally, Section 4 mainly lists the contributions of the op-amp and what are able to be improved in the future research. Not only is this newly designed three-stage CMOS operational amplifier able to provide a high gain for amplification of EEG signals, but also it has a low-power consumption which highly save its energy. This op-amp may offer a precise amplification and measurement of EEG signals.

2. Brief Review of Electroencephalogram (EEG) Signal Processing

EEG refers to the electrical signals generated by neuronal activity inside the human brain. Neurons are concatenated to by synapses, so that the complex neural networks are formed. When neurons are activated, they generate bioelectric phenomena, which is able to be collected by electrodes deployed on the scalp or implanted directly under the skull. However, it is much more important for researchers to work out how to precisely complete the work of EEG signal processing in case of incorrect measurement or diagnosis.

2.1. Basic Characteristics of the EEG signals

When capturing and amplifying the brain's main biological electric signals, which reveals the activities inside the brain, from the scalp with the help of precise medical electronic instruments, the graph of EEG signals can be created as is shown in Fig. 1 [2].

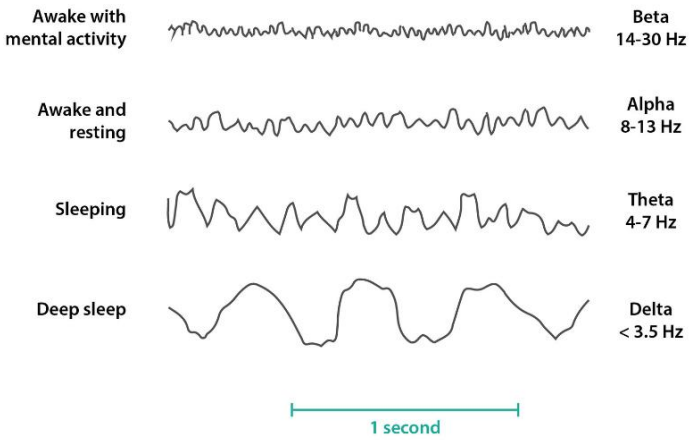

Fig. 1 the waveforms of beta, alpha, theta and delta in EEG signals [2]

Relying on the frequency range, research is able to classify the EEG signals into five sorts, each of which shows different neural activities [2]. Table 1 displays the frequency ranges of five kinds of EEG signals [3].

Table 1. Different classification and main details of EEG signals

Frequency (Hz)	IFCN-2017 Glossary	Corresponding brain activity
Delta	0.1 - <4	Deep relaxation and restorative sleep
Theta	4 - <8	Improvement of creativity, wholeness and intuition
Alpha	8 - 13	Coordination and communication
Beta	14 - 30	Cognitive reasoning, calculation, reading, communication and thinking
Gamma	>30 - 80	Learning, memory, and knowledge processing

The ionic currents that flow between the neurons in the human brain frequently produce the EEG signals. On the scalp's surface, this electrical activity can be monitored after passing through the skull. The electrical activity's amplitude and frequency are roughly 2 - 200 μV and 0.1 - 100 Hz, respectively. [4]. The neuron voltage is measured within the range of 0 to 200 mV [5].

2.2. EEG Signal Processing

The main sections of EEG signal processing are as follows: signal acquisition, signal pre-processing, feature extraction, feature analysis and visualization. The brief flowchart of the EEG signal processing is shown in Fig. 2.

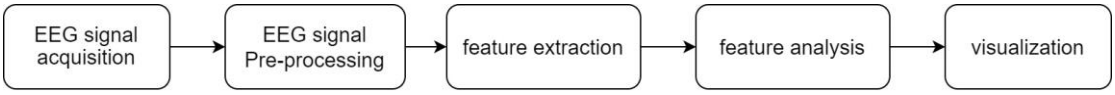

Fig. 2 General schematic diagram of EEG signal processing (Photo/Picture credit: Original)

According to the main schematic presented in Fig. 2, the initial two steps of EEG signal processing involve acquisition and pre-processing. During acquisition, the original EEG signals are sampled and amplified using hardware equipment such as an amplifier. Subsequently, a filter is applied to remove any signal noise. The final three steps, namely extraction, analysis, and visualization, utilize computer algorithms such as short-time Fourier transforms, vector machines, and neural networks for identification and subsequent signal processing.

Among the main schematic of EEG signal processing displayed in Fig. 2, the EEG signal Pre-processing is of importance before algorithmic processing of EEG signals such as feature extraction and analysis. EEG signal pre-processing is the first step in EEG signal processing, which aims to remove noise and artefacts from the original EEG signal, improve the signal-to-noise ratio, and lay the foundation for subsequent analysis [6]. The main pre-processing of a general biomedical signal is shown in Fig. 3.

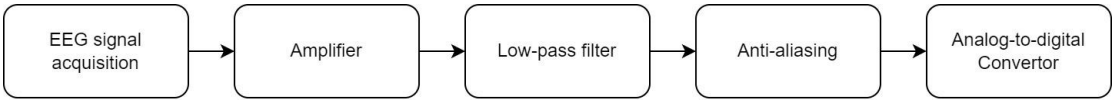

Fig. 3 General schematic of biomedical signal pre-processing (Photo/Picture credit: Original)

According to the main schematic displayed in Fig. 3, EEG signals usually have low voltage amplitudes and require amplification using an operational amplifier for further processing. To ensure a reliable signal and eliminate interference, it is necessary to filter and anti-alias the signal. Common filtering techniques include bandpass, trap, and notch filtering. The analog EEG signals are converted to digital using an ADC, allowing for computer analysis of the pre-processed signals.

2.3. Amplification, a key part of the EEG signal processing

As is mentioned above, the brain produces electrical signals with weak amplitudes, typically ranging from a few microvolts to hundreds of microvolts. To satisfy further processing and analysis, the EEG signal requires its amplification. Amplification increases both the amplitude of the EEG signal and the Signal-to-Noise Ratio (SNR), thereby improving the accuracy of the following processing and analysis. Hence, thanks to the recent improvements in VLSI technology, the high gain, low power applied in EEG signal collection and pre-processing systems have been swiftly discovered and improved. As a result, the amplification of bio-medical electronics has rapidly advanced in recent years [6].

Based on the design of the instrumentation amplifier (IA) in [6] and [7], the IAs are primarily applied in amplification of the small differential voltage signals produced at the output of transducers, making the signals collected more dependable and simpler for biomedical signal processing (e.g. EEG). The typical three op-amps IA is commonly used in EEG signal pre-processing thanks to the low DC offset, high gain, high common-mode rejection ratio (CMRR), and high input impedances [6]. Fig. 4 displays a typical schematic of a three op-amps instrumentation amplifier [6].

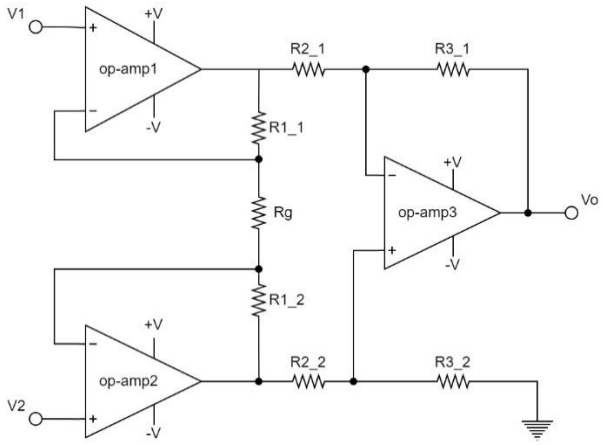

Fig. 4 typical circuit diagram of a three op-amps IA [6]

3. Modelling and Analysis

The significance of amplification for EEG signal processing cannot be underestimated. Achieving a high DC gain is one of the most essential features for a CMOS operational amplifier. However, in order to boost the DC gain of an op-amp, the technique of multi-stage cascading is now favored over than the typical vertical gain enhancement topology method (cascode and telescopic) to improve the gain of an op-amp, with the advancement of CMOS technology [7]. This section aims to expand the op-amp stages from two to three and add compensation components. An optimal solution is achieved by comparing various compensation methods used within the op-amp. This section describes the design of the operational amplifier using transistors manufactured in TSMC's 0.18μm technology. The basic structure of a two-stage CMOS operational amplifier is shown in figure 5.

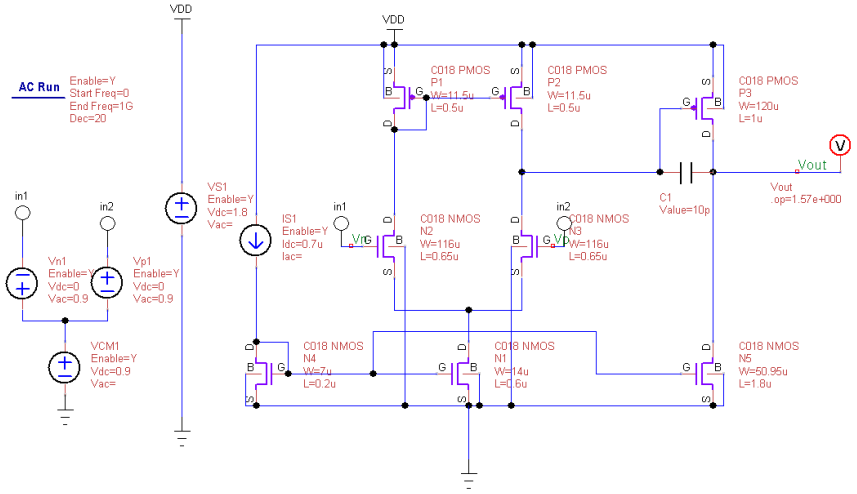

Fig. 5 The basic structure of a two-stage CMOS operational amplifier (Photo/Picture credit: Original)

3.1. Initial Circuit Modelling

The designed three-stage open-loop CMOS operational amplifier consists of three parts as is displayed in Fig. 6: the first stage (i.e. the differential transconductance stage, including a differential amplifier consisting of transistors P1, P5, P6, N1 and N2 to accept two inputs and provide the required high gain), the second stage (i.e., another differential transconductance stage, which is the main part of the op-amp and also includes a differential amplifier consisting of transistors P2, P3, N3, and N4, mainly to produce a higher voltage gain), and the third stage (i.e., the high-gain stage, which is basically a common-source amplifier including transistors P4 and N5) [8].

Comparing the two-stage op-amp in Fig. 5 and the three-stage op-amp in Fig. 6, where each stage of the three-stage operational amplifier is driven by the same DC bias voltage source set to 0.6V by triggering the gates of the transistors P1, N4, and P4 in Fig. 6 at a certain voltage level, instead of using a current mirror with a bias current source [8].

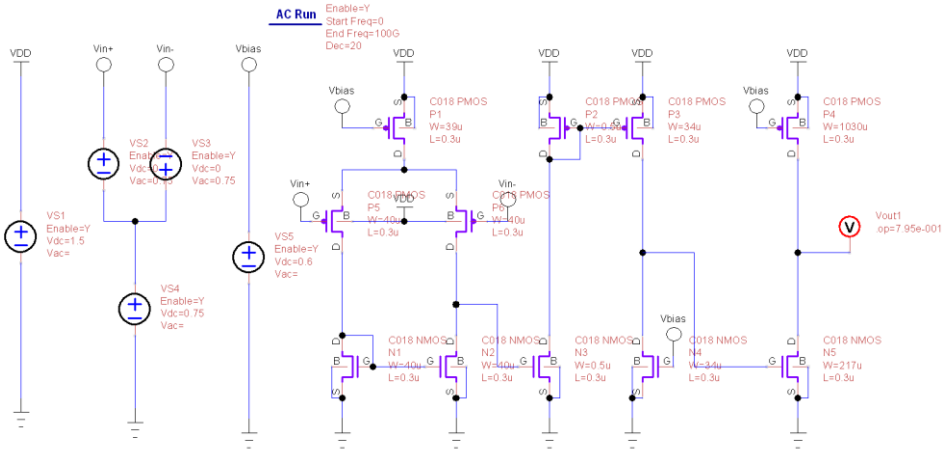

Fig. 6 the main structure of designed open-loop three-stage CMOS operational amplifier (Photo/Picture credit: Original)

After finishing creating the circuit structure in Fig. 6, each transistor's aspect ratio (W/L) is initially set to 40/0.3. Then the op-amp achieves its required DC gain and high voltage swing by increasing and adjusting each aspect ratio of each transistor in each stage.

3.2. Comparison of compensation methodologies

Theoretically, incorporating more stages in an operational amplifier can result in a higher gain. However, the most formidable challenge lies in frequency compensation. As the stages in the operational amplifier increases, the complexity of implementing the frequency compensation technique escalates correspondingly [9]. This is a critical aspect to consider in the design and optimization of operational amplifiers. Several compensation methods are introduced and compared in this section.

3.2.1 Nested Miller Compensation (NMC)

The NMC technique is a frequency compensation method that aims to approximate the system as a first-order integrator as much as possible. According to the main structure of a three-stage operational amplifier using NMC topology displayed in Fig. 7, the internal amplifiers g_{m2}, g_{m3}, and the internal compensation capacitor C_{m2} of the amplifier are regarded as an integral amplifier.

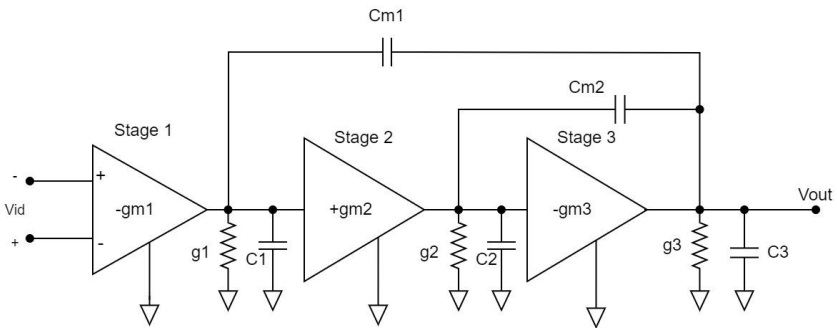

Fig. 7 the main structure of a three-stage NMC op-amp [10]

This integrator contains an amplifier g_{m3} that maintains the approximation of the integrator in the integrator through negative feedback C_{m2} [10]. However, the well-known NMC topology is only appropriate to the three-stage amplifier, where the second stage is non-inverting, and the third stage is inverting [9].

According to the analysis in [10], the conditions of C_{m1} and C_{m2} are obtained:

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_3 \tag{1}$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_3 \tag{2}$$

Then the gain-bandwidth product (GBW) is then given by:

$$GBW = \frac{g_{m1}}{C_{m1}} = \frac{1}{4}\left(\frac{g_{m3}}{C_3}\right) = \frac{1}{4}GBW_{single-stage} \tag{3}$$

As shown in formula (1) and (2), smaller values of C_{m1} and C_{m2} are required when g_{m3} is much greater than g_{m2} and g_{m1}. According to the analysis and AC simulation of NMC in [10], this condition is crucial for an NMC amplifier to work stably, without any unnecessary oscillations [10]. However, achieving this condition is challenging, particularly in designs of circuit with low power consumption. The structure of NMC can also bring about the problem of right-half-plane zeros (RHP zeros), which is essentially due to the cancellation of the feedforward current on the output stage current, and it may lead to the problem of instability of the op-amp system. Moreover, if the compensation capacitance is too large, it may introduce a zero point in the mid-low frequency range [10].

3.2.2 NMC using nulling resistor (NMCNR)

The structure of an NMCNR (NMC using a nulling resistor) amplifier is shown in Fig. 8. According to the comparison between NMC and NMCNR in [10], the NMCNR structure can effectively solve the problem of right half-plane zeros (RHP zeros) caused by the NMC structure. This problem is mainly due to the cancellation of the feedforward current on the output stage current [10]. Thanks to the zeroing resistor, the NMCNR amplifier can shift this unfavorable current balance position.

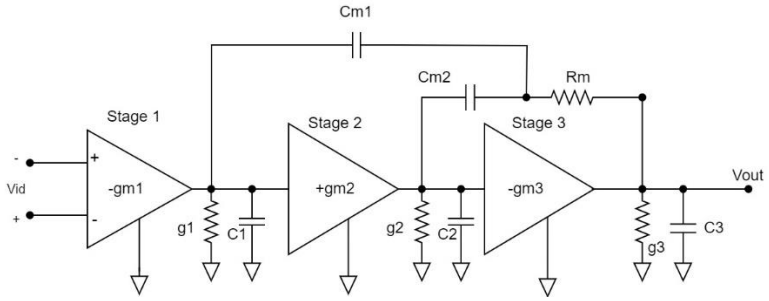

Fig. 8 the structure of NMCNR amplifier [10]

3.2.3 NMC with Feedforward Transconductance Stage and Nulling Resistor (NMCFNR)

Although the NMCNR topology uses a nulling resistor to eliminate the right half-plane zeros (RHP zeros), thereby improving the bandwidth reduction and poor transient response issues of the NMC amplifier, the bandwidth improvement of NMCNR is still limited compared to NMC.

In order to address this issue, the NMCFNR topology method is suggested in [11]. Fig. 9 displays the NMCFNR structure utilizing a feedforward transconductance stage and a nulling resistor to enhance frequency and transient response, as well as the power supply rejection ratio (PSRR), without raising consumption of the power or complexity of the circuit. Based on the analysis in [11], the NMCFNR can improve both the GBW and phase margin (PM) simultaneously, resulting in better performance of this advanced op amp compared to NMC and NMCNR.

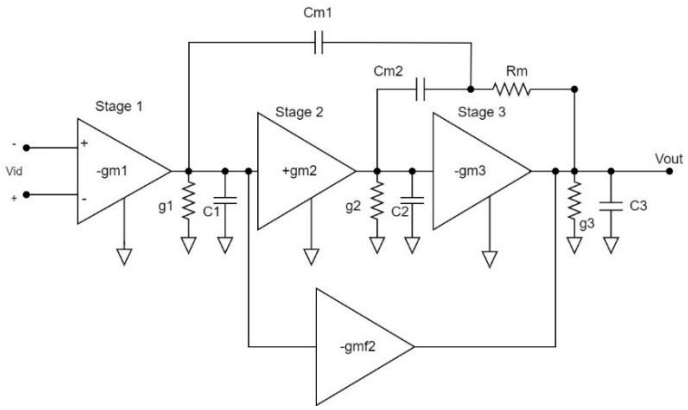

Fig. 9 the structure of NMCFNR amplifier [11]

3.3. Circuit Schematic re-modification and Simulation Results

As is measured in the DC simulation result in Fig. 10, the total current consumption is around 0.0132 A. Therefore, the total power consumption of the open-loop three-stage op-amp is

$$P_{total} = 1.5V \times 0.0132A = 19.8mW \tag{4}$$

which is a low-power consumption for an EEG amplifier.

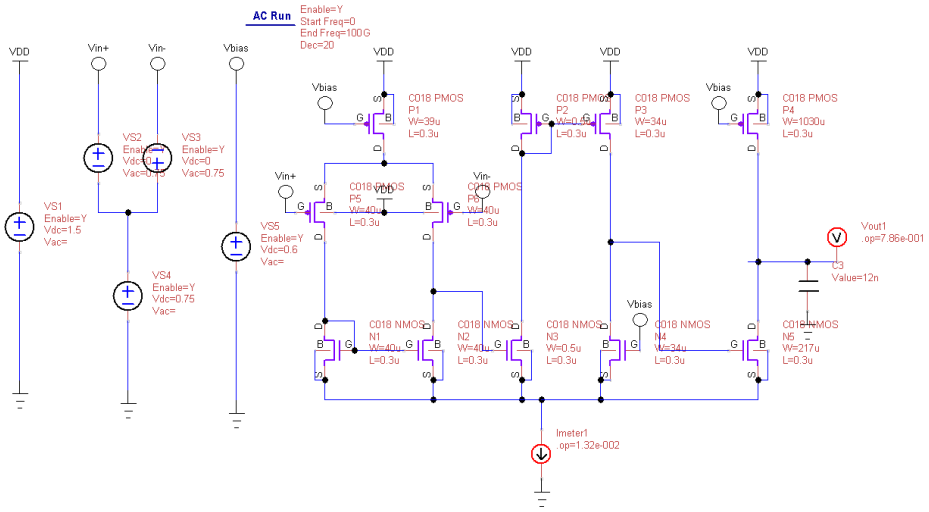

Fig. 10 the DC simulation of the open-loop op-amp in Fig. 6. (Photo/Picture credit: Original)

During the AC simulation of it shown in Fig. 11, the open-loop DC gain reaches 90.04dB and its -3dB bandwidth is approximately 2.05MHz. However, the simulation result indicates that the phase margin of this op-amp system is less than 0 degrees. Therefore, it is really essential to add frequency compensation to the system.

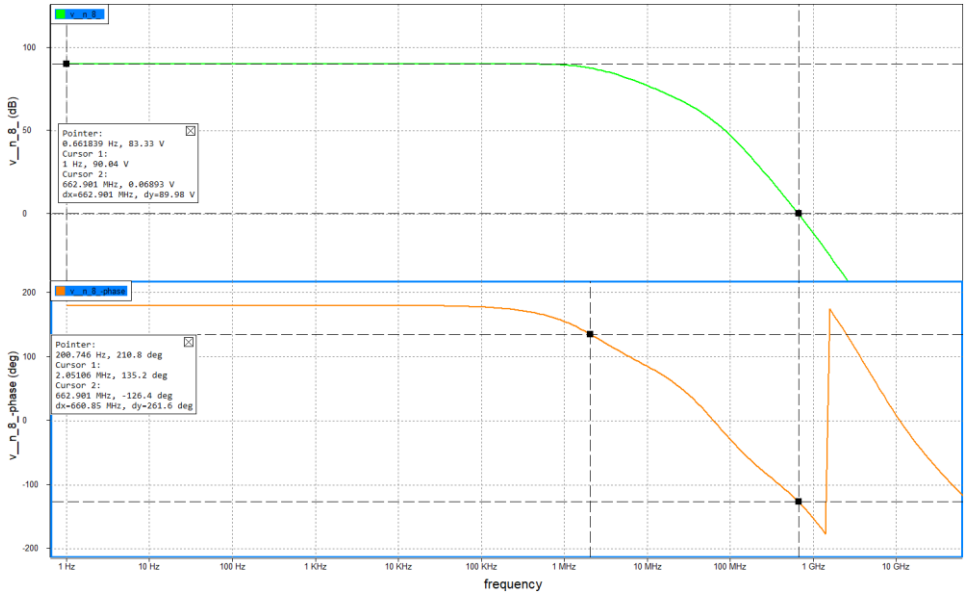

Fig. 11 the AC simulation result of the open-loop operational amplifier in Fig. 6. (Photo/Picture credit: Original)

Based on the analysis presented above, the schematic in Fig. 6 will be modified by adding the NMCFNR topology. The feedforward stage (gmf2, consisting of transistor P4) and the third stage (gm3, consisting of transistor N5) forms the push-pull output stage, as the schematic shown in Fig. 12. This circuit design refers to the one in [10].

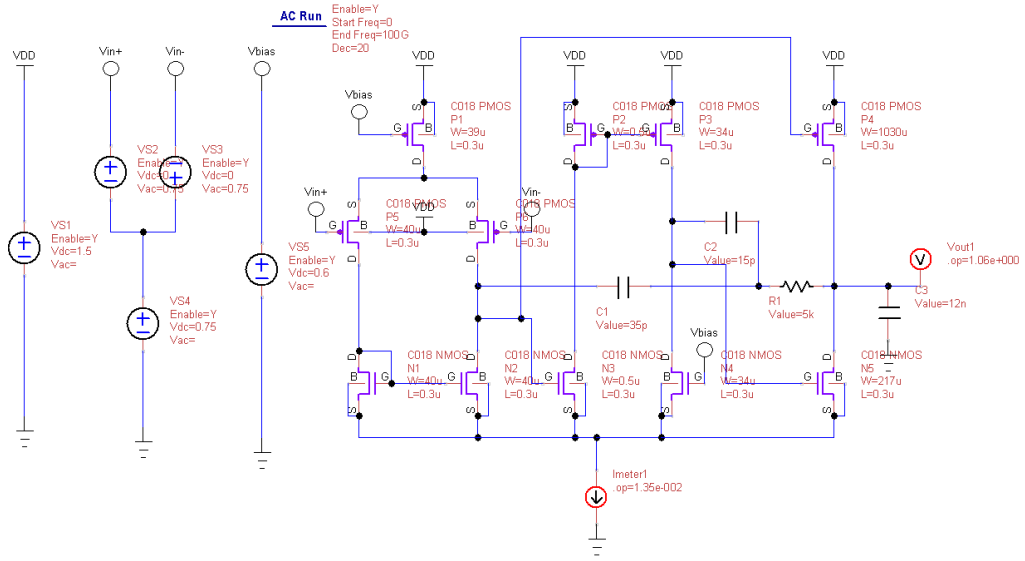

Fig. 12 the structure of NMCFNR EEG amplifier based on Fig. 6. (Photo/Picture credit: Original)

However, the AC simulation results in CoolSpice show that the GBW of the NMCFNR amplifier is lower than that of the open-loop amplifier, as shown in Fig. 13, because the DC gain is reduced by less than 80 dB and the -3 dB bandwidth is reduced to about 1.74 kHz. In addition, the phase margin remains less than 0 degrees, which still causes instability in the op-amp system.

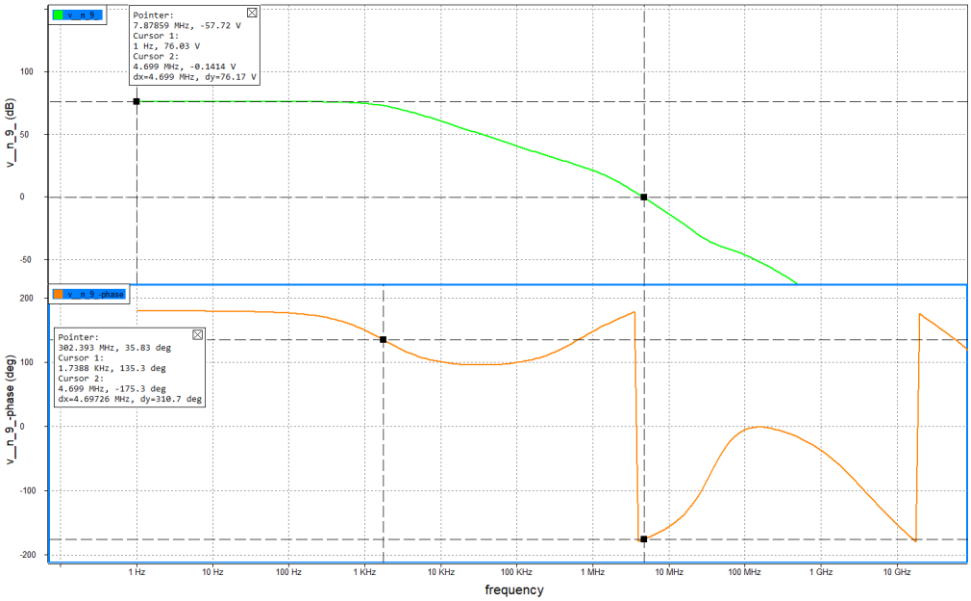

Fig. 13 the AC simulation of the NMCFNR amplifier in Fig. 12. (Photo/Picture credit: Original)

To address the issue of instability in the circuit system of op-amp, the transconductance in NMCFNR amplifier is decided to be cancelled and the circuit becomes an NMCNR amplifier, as the circuit schematic of it is shown in Fig. 14.

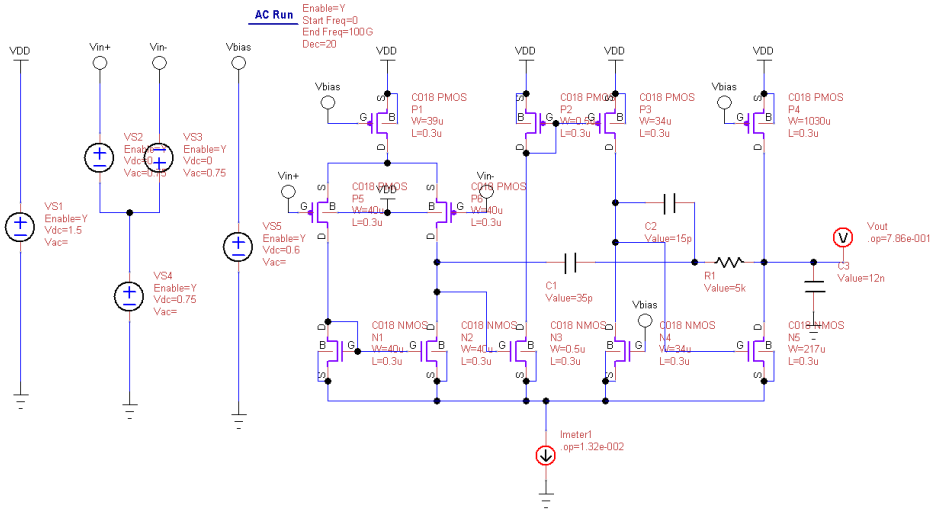

Fig. 1 the structure of NMCFNR EEG amplifier based on Fig. 6. (Photo/Picture credit: Original)

As its AC simulation is displayed in Fig. 15, the DC gain of it is same as the one of the open-loop operational amplifier in Fig. 6. The -3dB bandwidth is around 363 Hz, which is exceeds the range of EEG signal frequency and allows the amplifier to capture all the EEG signals. The phase margin reaches to 177 degrees, leading to the perfect stability of the system.

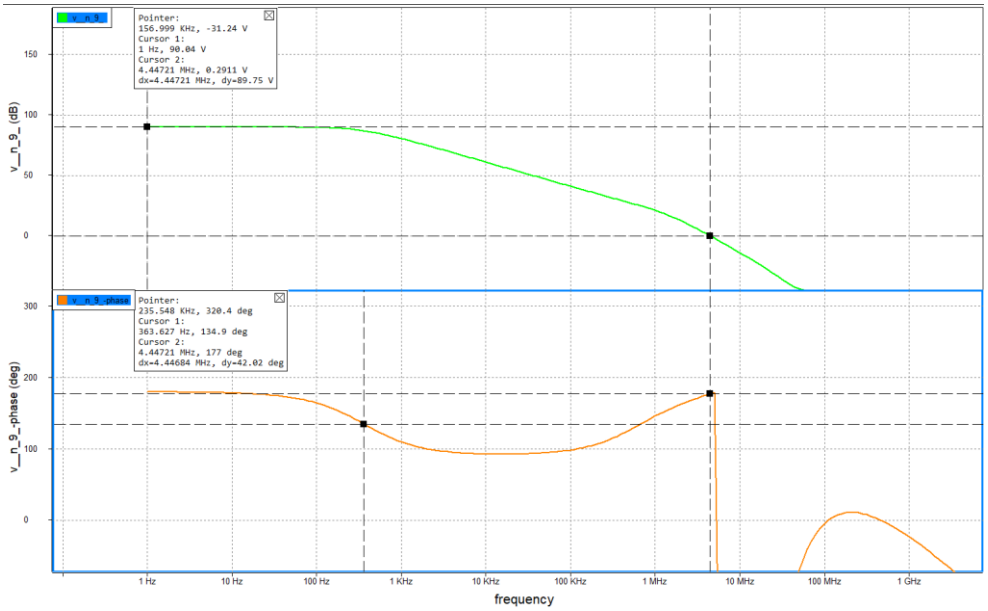

Fig. 2 the AC simulation result of NMCNR amplifier in Fig. 14 (Photo/Picture credit: Original)

In results, this EEG amplifier, which has the gain of 90.04 dB and the bandwidth of 363 Hz, works stably and is able to capture all of the EEG signals and amplify them during the EEG signal processing, for the reason that according to the Nyquist Sampling Theorem, in order to be able to recover an analogue signal in its entirety, the sampling frequency must be at least twice the highest frequency of the signal. Therefore, the highest frequency of the EEG signal is 100 Hz, then the sampling frequency must be at least 200 Hz, so that the bandwidth of the EEG signal amplifier must be designed larger than 200 Hz.

4. Conclusion

During the circuit simulation of the designed three-stage op-amp in this paper, it achieves a high open-loop gain with the value of 90.04 dB, which is able to amplify the EEG signals larger than 30000 times. As the DC simulation analyzed in the paper, the op-amp has a low-power consumption of 19.8mW, which save the energy of the whole op-amp system. With the help of frequency compensation – nested Miller compensation using nulling resistor (NMCNR), applied in the open-loop op-amp, the value of the bandwidth of the op-amp reaches to 363 Hz, which has the capability of amplifying all sorts of EEG signals and measuring them. This op-amp has the phase margin of 177 degrees, which makes the op-amp circuit system stable and avoids the unnecessary oscillations during the EEG signal amplification, which lead to a precise measurement on EEG signals and provide the precise diagnosis for the patients.

However, this designed three-stage op-amp still remains challenges. Some paraments of the op-amp, such as slew rate (SR) and common-mode rejection rate (CMRR), have not been measured and simulated in the simulation. The power consumption of the circuit is not lower than 1 mW, which is needed to be improved in the future research. Meanwhile, the frequency compensation applied in the op-amp still has to be consummated in the future. Last but not least, in spite of the accurate data shown in the circuit design, the instrumentation amplifier based on this op-amp and the actual medical application of it still remains to be further discovered.

References

[1] Siuly S, Li Y, Zhang Y. EEG signal analysis and classification. IEEE Trans Neural Syst Rehabilit Eng, 2016, 11: 141-144.

[2] Li B, Cheng T, Guo Z. A review of EEG acquisition, processing and application. Journal of Physics: Conference Series. IOP Publishing, 2021, 1907(1): 012045.

[3] Babiloni C, Barry R J, Başar E, et al. International Federation of Clinical Neurophysiology (IFCN)–EEG research workgroup: Recommendations on frequency and topographic analysis of resting state EEG rhythms. Part 1: Applications in clinical research studies. Clinical Neurophysiology, 2020, 131(1): 285-307.

[4] Hung C C, Wang S H, Hung C C, et al. Introduction to Biomedical Signals and Their Applications. Ultra-Low-Voltage Frequency Synthesizer and Successive-Approximation Analog-to-Digital Converter for Biomedical Applications, 2022: 1-22.

[5] Hall J E. Brain Activities-Sleep, Brain Waves, Epilepsy, Psycosis. Textbook of Medical Physiology. United Kingdom. Elsevier, 2011, 12: 721-725.

[6] Jain A, Kandpal K. Design of a high gain, temperature Compensated biomedical instrumentation amplifier for EEG applications. 2017 11th International Conference on Intelligent Systems and Control (ISCO). IEEE, 2017: 292-296.

[7] Saurabh S, Saifi M, Karatangi S V, et al. Design of CMOS Instrumentation Amplifier Using Three-Stage Operational Amplifier for Low Power Signal Processing. International Conference on Artificial Intelligence: Advances and Applications 2019: Proceedings of ICAIAA 2019. Springer Singapore, 2020: 77-82.

[8] Seddighrad P, Tokunaga C, Eric C H S. Three-stage Nested Miller Low-Voltage Amplifier.

[9] Cheng Y. A Novel Feedforward Reversed Nested Miller Compensation Technique for Three-Stage Amplifiers. 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings. IEEE, 2006: 1788-1790.

[10] Leung K N, Mok P K T. Analysis of multistage amplifier-frequency compensation. IEEE transactions on circuits and systems I: fundamental theory and applications, 2001, 48(9): 1041-1056.

[11] Leung K N, Mok P K T. Nested Miller compensation in low-power CMOS design. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 2001, 48(4): 388-394.