Optimization Analysis of MOSFET Structure and Application

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Abstract. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a crucial power semiconductor device used in electronic equipment, playing a key role in various electronic systems and power electronics. As electronic technology advances, the demand for MOSFETs is increasing, requiring higher switching speeds, lower power consumption, enhanced reliability, and improved integration. Therefore, optimizing MOSFETs and exploring their applications is of significant research importance. This article presents an analysis conducted by both domestic and international scholars, focusing on topics such as the use of asymmetric inner surface oxide, layout optimization of bipolar MOSFETs, design enhancements of fully-encircled gate (GAA) MOSFETs, and studies on double-layer epitaxial structures. Additionally, it discusses the potential applications of MOSFETs in automotive electronic systems. Furthermore, the article delves into the future prospects of MOSFETs, highlighting the exploration of new materials, technological advancements, and heterogeneous integration to achieve higher performance, smaller size, and lower power consumption in devices. Furthermore, these findings from the research assist in guiding ongoing advancements in MOSFET technology and provide an outline of potential future developments.

Keywords: MOSFET, PN junction, Optimization.

1. Introduction

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a semiconductor device widely used in electronic circuits, which is known for its high input impedance, low driving power, fast switching speed and good integration performance. With the rapid development of electronic technology, MOSFETs, as one of the core components, play a crucial role in various electronic devices [1]. The optimization and application of MOSFETs have been a hot topic in the field of electronic engineering. The purpose of this paper is to discuss the latest optimization techniques of MOSFETs and their applications in modern electronic systems.

This paper first introduces the basic structure of MOSFETs and their principles, then discusses the study of MOSFETs through asymmetric inner surface oxides, followed by an overview of how MOSFETs can be optimized for energy-efficient circuit design. The effect of stress on the saturation current of MOS devices in 130 nm CMOS processes is also discussed. The structural aspects of MOSFETs are also discussed, exploring the design optimization of full-gate (GAA) MOSFETs and the optimization study of the performance of double-layer power trench MOSFETs. The design considerations for power MOSFETs in automotive electronic systems are analyzed in terms of applications. Finally, this paper provides an outlook on the future challenges of MOSFETs and the direction of research and development.

2. The basic structure and principle of MOSEFT

2.1. The structure of MOSEFT——PN junction

MOSFET consists of four main components: source (S), drain (D), gate (G), and substrate (B). Figure 1 shows a schematic diagram of the MOSFET [2].

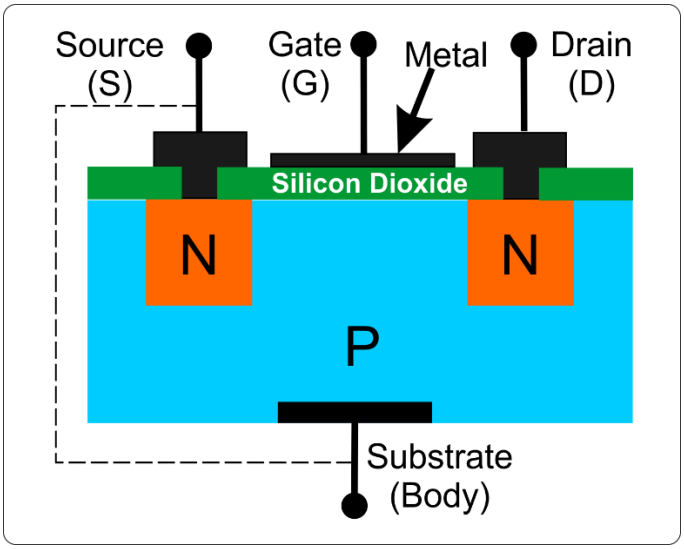

Figure 1. Schematic diagram of the MOS tube structure [2]

Source and drain are two main endpoints of MOSFET, respectively as the input and output of current. They are usually made of highly doped N-type or P-type semiconductor materials. The gate is isolated from the substrate by an insulating layer. Voltage changes in gate can control the flow of current between the source and drain. The insulating layer is usually composed of silicon dioxide (SiO2), The insulating layer is usually composed of silicon dioxide (SiO2), which allows the electric field to pass through but prevents the direct flow of charges. The substrate is the foundation of the entire transistor and can be made of P-type or N-type semiconductor materials, depending on the desired channel type.

2.2. Principles of MOSFET

MOSFET can be categorized into two types based on their operational principles: enhancement-type MOSFET and depletion-type MOSFET. For instance, in the case of an enhancement-type MOSFET, there exist two back-to-back PN junctions between the drain (D) and source (S). In the scenario where the voltage between the gate and source (VGS) is zero, despite a positive voltage (VDS) between the drain and source, the absence of conduction occurs due to one PN junction being in reverse bias, resulting in a drain current (IP) of zero.

Upon the application of a positive voltage between the gate and source, an electric field emerges from the gate towards the P-type silicon substrate within the SiO2 insulating layer situated between the gate and substrate. As SiO2 is an insulator, the VGS voltage does not generate a current, leading to the formation of an electric capacitor on either side of the oxide layer. VGS can be likened to the charging of this capacitor. With the gradual increase in VGS, the positive gate voltage attracts majority carriers towards the gate side, thereby establishing an N-type conductive channel from the drain to the source. Upon surpassing the MOSFET's turn-on threshold voltage, the N channel initiates conduction, resulting in the formation of the drain current (ID). The voltage between the gate and source at the onset of channel formation is referred to as the turn-on voltage [2].

3. Performance Optimization of MOSFET

3.1. Performance optimization of MOSFET using asymmetric internal surface oxides

The Pilot Center for Integrated Circuit Processes of the Institute of Microelectronics, Chinese Academy of Sciences (ICMS), China, has investigated the characteristics of asymmetric internal surface oxide devices using TCAD software. To control the short-channel effect of the devices, a thick inner surface oxide layer is applied to the source side of the devices to suppress the carrier mobility reduction, while a thin inner surface oxide layer is applied to the drain side. The performance of the device with asymmetric inner surface oxide is optimized, and the optimal performance is

obtained when about 15% of the thick inner surface oxide is applied to the source side of the device. After the optimization, not only the drive current of the device can be increased by 5%~15%, but also the short-channel effect is better [3].

3.2. MOSFET optimization toward power efficient circuit design

The ISDCS report examines optimization strategies for advanced MOSFET utilized in the development of energy-efficient circuits. The study employs a physically based compact model, HiSIM2, to investigate the correlation between device and circuit properties. Findings indicate that the short-channel effect, typically quantified by a threshold voltage deviation from long channel MOSFET, offers a consistent metric for assessing the impact of short channels on device performance decline. However, the degradation of circuit performance, such as power dissipation, cannot be accurately forecasted solely based on short-channel effects. The outcomes suggest that enhancing energy efficiency in circuit designs can be accomplished by minimizing the additional leakage current stemming from short-channel contributions [4].

3.3. Effect of Stress on the Saturation Current of MOS Devices in 130 nm CMOS Process

In the advanced submicron CMOS integrated circuit manufacturing process, the impact of stress on the operational efficiency of MOS devices has become a significant consideration. Stress has the ability to alter the mobility of semiconductor carriers, thereby influencing the saturation current of MOS devices. A study conducted by the National ASIC System Engineering Technology Research Center, Southeast University investigated the relationship between the operational performance of MOS devices and the layout configuration, utilizing variables such as the diffusion width of the active region, device channel width, and channel length. The study involved a quantitative analysis of the effects of stress induced by shallow trench isolation (STI) and source/drain metal silicide on the saturation current of MOS devices. It was found that x-direction STI compression stress can enhance the saturation current of PMOS devices by approximately 10% and decrease that of NMOS devices by 20%-30%. Similarly, y-direction STI compression stress was observed to reduce the saturation current of NMOS devices by 16%-20% and PMOS devices by 14%. Furthermore, y-direction STI compression stress was found to decrease the saturation current of NMOS devices by 16%-20% and PMOS devices by 14%. Additionally, the y-direction STI compression stress was noted to reduce the saturation current of NMOS devices by 16%-20% and PMOS devices by 14%. Moreover, the x-direction stress induced by source/drain metal silicide was found to have a more pronounced impact on the saturation current of NMOS devices compared to PMOS devices. The study suggests optimizing the layout design of MOS devices based on these findings. Specifically, for PMOS devices, it is recommended to employ a layout design with a wider channel width and minimized diffusion width. On the other hand, for NMOS devices, in addition to a wider channel width, a larger diffusion width is also advised for an optimized layout design [5].

3.4. Design optimization of gate-all-around (GAA) MOSFETs

Double-Gate (DG) MOSFETs are regarded as among the most promising candidates for operating in the sub-50 nm regime in CMOS scaling. This is primarily due to their excellent transconductance and robust resistance to the short channel effect (SCE). Enhancing the subthreshold swing (SS) and minimizing the drain-induced barrier lowering (DIBL) in DG MOSFETs can be significantly influenced by considering the ratio of fin width to gate length as a crucial design parameter. IEEE Transactions on Nanotechnology optimizes the design of a full-gate (GAA) MOSFET and compares it with that of a dual-gate MOSFETs are compared. The GAA MOSFETs is compared with DG MOSFETs by 3D device simulation. The GAA MOSFETs shows better suppression of the short-channel effect compared to DG MOSFETs. It has been verified that GAA MOSFETs offers advantages in CMOS scaling over DG MOSFETs. We conducted additional simulations for MOSFETs with cylindrical channels. The ideal cylindrical-channel MOSFET, designed to minimize corner effects, exhibits lower SS and DIBL in comparison to the cubic-channel GAA MOSFET. Thus,

it is evident that the optimized structure for GAA MOSFETs should feature cylindrical channels and effectively mitigate the short-channel effect, even if the fin width of this optimal cylindrical-channel MOSFET exceeds the gate length. In the case of the ideal cylindrical-channel MOSFET, the maximum ratio of fin width to gate length stands at 1.2 [6].

3.5. Optimization of power Trench MOSFETs With Double-Epilayer

Researchers from the Institute of Microelectronics at Southwest Jiaotong University in Chengdu, China, have conducted a study focusing on the optimization of n-type low-voltage power trench MOSFETs, specifically U-MOSFETs, utilizing a dual epitaxial layer structure. The research involved analyzing the impact on device performance by adjusting the thickness of the intrinsic epitaxial layer while maintaining a constant total epitaxial layer thickness of 4.0 microns. Through simulation experiments, the researchers thoroughly examined the effects of varying thicknesses of the intrinsic epitaxial layers on key parameters such as on-resistance ($R_{ds,on}$), gate-drain capacitance (C_{gd}), and blocking voltage (BV_{dss}) of the U-MOSFETs. The findings revealed that by optimizing the dual epitaxial layer structure, a notable reduction in on-resistance of the U-MOSFETs could be achieved without compromising the blocking voltage and threshold voltage. Specifically, the on-resistance ($R_{ds,on}$) decreased by 13% at a gate voltage of 4.5V and by 14.9% at 10V. Furthermore, the gate-drain capacitance (C_{gd}) exhibited a reduction of 31.3%, leading to enhanced switching characteristics, decreased switching time, and lower power consumption [7].

3.6. Design considerations for power MOSFETs in automotive electronic systems

In automotive electronic systems, power MOSFETs, as representatives of semiconductor power devices, are gradually replacing traditional mechanical relays. The Intelligent Network Development Institute of China First Automobile Group Corporation analyzes several key technical factors that need to be considered when power MOSFETs are applied in automotive electronic systems. The avalanche operation mode of MOSFETs when the drain-source voltage exceeds the breakdown voltage is investigated, parameters such as avalanche breakdown voltage and avalanche energy are analyzed, and how to protect the device in avalanche mode is discussed. The factors affecting the switching speed of MOSFETs, especially the effect of parasitic capacitance, are also discussed, and methods to improve the switching speed, such as selecting MOSFETs with small parasitic capacitance and optimizing the driving resistance, are proposed. And strategies to detect and protect MOSFETs from short-circuit damage are proposed, as well as how to reactivate MOSFETs through self-recovery after the short-circuit fault disappears. Finally, the importance of effective thermal management of power MOSFETs in automotive electronic systems is emphasized, and thermal characteristics such as thermal resistance and junction temperature are analyzed, and how to control the temperature of the device by design is discussed in order to ensure its high-temperature reliability in the environment [8].

4. Challenges and future development directions of MOSFET

4.1. The challenge faced by MOSFET

As the device feature size continues to shrink, a variety of effects gradually emerge, which seriously affect the performance and reliability of the device. First, the short channel effect (SCE) leads to device performance degradation, such as threshold voltage reduction and leakage current increase. Second, under strong electric fields, the hot carrier injection effect (HCI) increases the carrier energy, which may cross the potential barriers to form gate currents, thus affecting the reliability and lifetime of the device. Finally, as the gate oxide thickness decreases, quantum tunneling effects lead to an increase in gate leakage current, which affects power consumption and device performance. These effects pose significant challenges in the design and fabrication of modern microelectronic devices.

4.2. The future development direction of MOSFET

New high dielectric constant (High-k) dielectric materials and metal gate materials are being developed to replace conventional SiO2 and polysilicon gates to reduce gate leakage current and improve performance. For example, silicon carbide (SiC), gallium nitride (GaN), graphene (graphene) three types of materials have different advantages in different areas. Although the development of MOSFETs like graphene is limited by the difficulty of industrial synthesis, it still has great potential. The new material MOSFETs significantly improve the electron mobility and some aspects of the stability of the FETs by adding materials such as SiC, GaN and graphene, making them more promising for a wider range of applications in electronics and power [9].

MOSFET design and manufacturing processes are continuously optimized, such as the application of FinFET and FD-SOI technology, which can more effectively control the channel potential and suppress the short-channel effect.

The integration of electronic components of different materials, processes, functions or sizes into a single system or chip to achieve higher performance, smaller size, lower power consumption and higher functional integration. Heterogeneous integration technology is one of the key directions that will continue to drive the semiconductor industry, enabling electronic devices to deliver more performance and more functionality in a smaller size [10].

5. Conclusion

This paper provides an in-depth analysis of MOSFET structures, operating principles, performance optimization strategies, and challenges and future trends. The performance of MOSFETs is significantly enhanced by the application of asymmetric internal surface oxides, layout optimization of bipolar MOSFETs, design improvement of fully surrounded gate (GAA) MOSFETs, and optimization of double-layer epitaxial structures. Meanwhile, for the application of MOSFETs in automotive electronic systems, the article discusses key technical factors such as avalanche mode of operation, switching speed, short-circuit protection, and thermal management. Although MOSFETs face challenges such as short-channel effect, hot carrier injection and gate oxide leakage during size reduction, MOSFET technology is expected to achieve higher performance, smaller size and lower power consumption in the future through the development of new materials, technological innovations and heterogeneous integration, providing a strong support for the development of electronics and power electronics.

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