

Absolute value comparator structure optimization and application scenario analysis

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Abstract. In the era of rapid Internet and information technology advancements, individuals are now privy to a wider array of information channels, rendering access to information more extensive and convenient. Nevertheless, the concomitant information explosion has led to a significant surge in data volume, necessitating the employment of more efficient methodologies for processing and comprehension. A comparator serves as a valuable tool in assisting individuals to compare and contrast data, thereby enhancing their understanding of the intricate relationships among various datasets. This paper will commence with an exploration of the fundamental four-digit absolute value comparator, elucidating its operational principles. We have segmented the entire circuitry into two distinct components, namely, an absolute value calculator and a comparator. Subsequently, we have optimized and designed the resulting circuit, identified the critical path delay, and calculated pertinent parameters. Furthermore, we delve into the extended applications of the comparator, particularly its utilization in image sensor localization and signal processing. Finally, this paper presents the challenges confronting the development of the comparator and offers insights into its future prospects. Through the comprehensive study presented in this paper, readers will gain a profound understanding of the principles and applications of the comparator, thereby facilitating beginners in their learning and expansion endeavors.

Keywords: Absolute value comparator, critical path delay, image sensor localization, signal processing direction.

1. Introduction

As the Internet and information technology continue to advance rapidly, individuals now enjoy expanded and more convenient access to information channels. Nevertheless, the explosive growth of data occasioned by this information overload necessitates the employment of more efficient methods for processing and comprehension. The comparator serves as a valuable tool in this regard, facilitating the comparison of data and enhancing understanding of the underlying relationships [1]. The demand for comparators spans across diverse fields, encompassing business, science, medicine, society, and beyond, where they play pivotal roles. Furthermore, the continuous advancements in machine learning and artificial intelligence technology have spurred the development of comparators. Leveraging technologies like machine learning algorithms and deep neural networks, it is possible to construct more precise and efficient comparator models, enabling more intricate and comprehensive comparative analyses.

This paper shall commence with an exploration and elucidation of the fundamental working principles of the four-digit absolute value comparator [2]. The entire circuit has been divided into two distinct sections, namely, the absolute value calculator and the comparator, for the purposes of designing them individually. Subsequently, the obtained circuit has been optimized and redesigned, with the relevant parameters meticulously calculated. The optimized circuit exhibits an energy consumption of 19.26. Furthermore, this paper delves into the expanded applications of the comparator, with a focus on its utilization in image sensor positioning as well as its application in signal processing directions. Finally, the paper highlights the challenges facing the development of comparators and offers anticipations for their future advancements.

2. Design and optimization of the 4-bit absolute comparator

2.1. Absolute-value Detector

The absolute value detector is a specially designed magnitude comparator. It will have signed values as input and output 0 or 1 to indicate whether the absolute value of one input is greater than the other. There is Fig.1 showing the basic diagram of a 4-bit AVD.

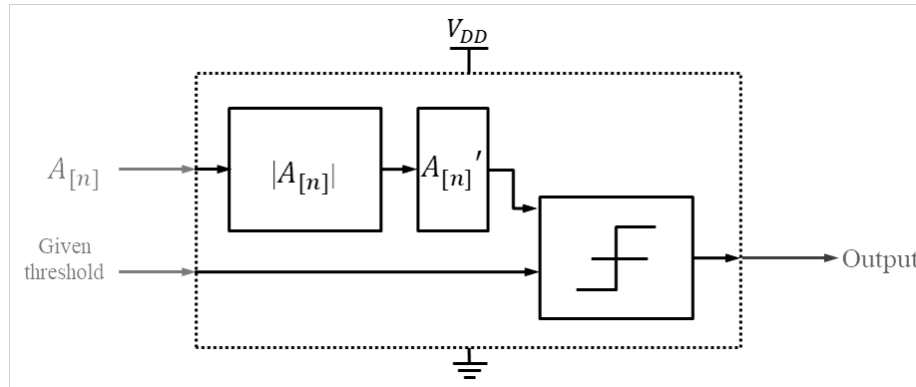


Figure 1. Basic diagram for an AVD

The inputs are presented on the left-hand side of the interface. The AVD circuits expounded in this study encompass an absolute value calculator and a comparator. The circuit's output is graphically represented on the right-hand side, clearly indicating whether the input signal $A[n]$ surpasses the designated threshold value T . If $A[n]$ exceeds the threshold T , the output will assume a high logic state; otherwise, it will maintain a low logic state [3].

In the present study, the absolute value of the input signal is not computed when the signal falls below zero [4]. Conversely, if the input signal exceeds zero, the approach outlined in this paper utilizes the method of 2's complement. Subsequently, this value is contrasted with a predetermined threshold. Depending on the sign of the computational outcome, the comparison result can be determined [5].

The proposed scheme utilizes logical operations to fulfill the role of the comparator, effectively enhancing the utilization efficiency of the circuit device and streamlining the complexity of the circuitry. Additionally, it offers ease of implementation in engineering practices. The principle of the absolute value detector is described as follows. The initial phase involves ascertaining the polarity of the input signal, whether it be positive or negative. Throughout this paper, the quartet of input signals shall be collectively designated as A . Subsequently, A' shall represent the outcome resulting from the execution of the 2's complement operation. The polarity of the input signal is discerned primarily based on the numerical value of the symbol bit A_3 . In the case of a negative input signal, no computation of the output is conducted. Conversely, for an input signal with a positive value, the 2's complement calculation is executed in order to derive the corresponding negative value [6].

$$A' = -|A| \quad (1)$$

The second crucial stage involves the detection and comparative analysis of A' against the established thresholds. Throughout this study, the derived outcomes are collectively designated as B . In scenarios where the input signal falls below zero, the full adder is employed to execute the addition operation on the prescribed value, leveraging its direct output capability. Conversely, when the input signal surpasses zero, the full adder executes the subtraction operation by implementing the 2's complement technique. Logic operations are utilized in this context to streamline the circuit's complexity [7]. The formula below shows the results.

$$B = T + A' = T - |A| \quad (2)$$

The input signal specified in this article is A . From high to low, the sign bit and the input signal bit are A_3, A_2, A_1, A_0 . The given threshold is collectively referred to as T . The given threshold bits

are A_3 , A_2 , A_1 and A_0 from high to low. A' is the result of 2's complement operation of the A . When A_3 is equal to 0, then A is larger than zero. This paper take 2's complement operation on it. The logical operation formulas are as follows.

$$A_0' = A_0 \quad (3)$$

$$A_1' = A_1 \oplus A_0 \quad (4)$$

$$A_2' = A_2 \oplus (A_1 + A_0) \quad (5)$$

$$A_3' = A_3 \oplus (A_2 + A_1 + A_0) \quad (6)$$

The calculation results of the above algorithm are shown in the table 1below.

Table 1. Truth table

$A_3A_2A_1A_0$	$A_3'A_2'A_1'A_0'$
1000	1000
1001	1001
1010	1010
1011	1011
1100	1100
1101	1101
1110	1110
1111	1111
0001	1111
0010	1110
0011	1101
0100	1100
0101	1011
0110	1010
0111	1001

This paper introduces the design of a chain adder, employing the 2's complement approach to perform subtraction. Regarding the design specifications, the chain adder incorporates an input buffer of one unit, powered by two inverter chains, each consisting of a single unit. The chain adder comprises three full adders connected in series to generate the final output. Each individual full adder within this configuration features an input signal labeled as A , a logical operation result labeled as B , an input C_{in} , and an output C_{out} . The operational outcomes of a single full adder are encapsulated in the following formula [8].

$$C_{out} = AB + (A \oplus B) C_{in} \quad (7)$$

Since the load outputs have been connected in series in this paper, the output of the chain load adder is B_3 .

$$B_3 = T_2A_2' + (T_2 \oplus A_2') (T_1A_1' + (T_1 \oplus A_1') (T_0A_0')) \quad (8)$$

The ultimate output result is designated as $A_3' + B_3$. A schematic diagram of the absolute value detector circuit is drawn here, as shown in the figure 2 below.

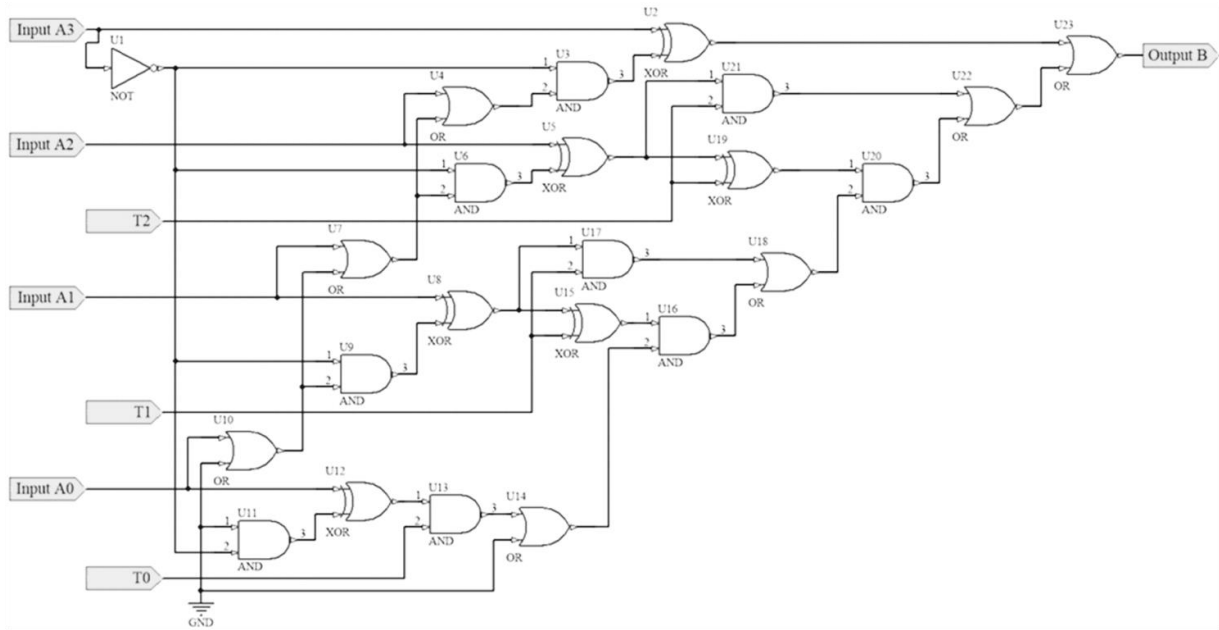


Figure 2. Absolute value detector circuit schematic diagram

2.2. Determination of the critical pathways

The critical path represents the logical sequence within the circuit diagram that exhibits the maximum delay from the point of input to the point of output. Referring to fig. 3, the designated path is identified as the critical path.

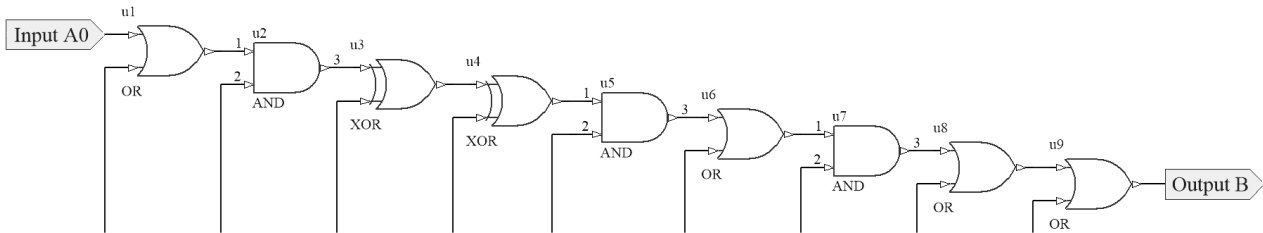


Figure 3. Absolute-value Detector critical path

As shown in table 2, several known parameters will be used in the calculations of the formulas [9].

Table 2. Logical effort of common gates

Gate Type	Number of Inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
Tristate, Multiplexer	2	2	2	2	2
XOR, XNOR		4,4	6,12,6	8,16,16,8	

When $V_{DD} = 1V$, the critical path delay is calculated here. Based on the path logic effort principle, this paper performs a calculation of the logic effort within the multi-level path [10].

$$G = \prod g_i = \frac{4^6 \times 5^3}{3^7} \quad (9)$$

H is the electrical effort along the path:

$$H = \frac{C_{out}(path)}{C_{in}(path)} = 32 \quad (10)$$

B is path branch effort:

$$B = 1 \quad (11)$$

Here is path effort:

$$F = GBH \quad (12)$$

$$\hat{f} = \sqrt[N]{F} = 2.69 \quad (13)$$

P represents the parasitic delay of the path:

$$P = 22 \text{ PS} \quad (14)$$

D represents the total path delay:

$$D = N\hat{f} + P = 46.25 \text{ PS} \quad (15)$$

The V_{DD}^{opt} is optimal voltage for the V_{DD} in the range of 0v -1v. The voltage also satisfies the requirement for a maximum delay of 1.5 minimum delays. As the following formula shown, it uses t_p to calculate the V_{DD}^{opt} :

$$t_p = \frac{CV_{DD}}{K'(V_{DD}-V_T)^2} \quad (16)$$

$$K' = \frac{W}{L}K \quad (17)$$

Based on the given scenario, which stipulates that the maximum delay is 1.5 times the minimum delay, we have predetermined a value of V_T equal to 0.2v.

$$D \propto \frac{V_{DD}}{(V_{DD}-V_T)^2} \quad (18)$$

$$V_{DD}^{opt} = 0.7758V \quad (19)$$

So D_1 as the critical path delay shows below:

$$D_1 = 1.5 D = 69.38 \text{ PS} \quad (20)$$

Energy consumption when $V_{DD} = 1v$

$$E = C_1 V_{DD}^2 = 32.00 \quad (21)$$

The overall energy consumption of the circuit remains unchanged.

$$E = C_1 V_{DD}^{opt^2} = 19.26 \quad (22)$$

3. Application scenario analysis and Challenges facing the Institute

3.1. Application in the image sensor orientation

The development of image sensor is more and more convenient for People's Daily life. Scholars at home and abroad are making efforts for the design of high-performance image sensor. At present, the mainstream image sensors on the market are divided into CMOS image sensor and CCD image sensor, while FGMOS-type pixel devices are gaining more and more attention because of their advantages of multi-signal control and variable and controllable threshold. Compared with the ordinary MOS tube, the FGMOS-type pixel device adds a layer of control gate, but the way of generating the pixel current is not much different from that of the ordinary MOS tube. Based on FGMOS-type pixel device, Jiangnan University designed a high-precision image sensor reading circuit system based on current readout. It is composed of clamp circuit, current mirror copy circuit, 1-V conversion circuit and comparator. The reference voltage of the comparator is generated by 10-bit ramp voltage. The key circuit module design of the overall readout circuit is conducted, and the improved reference current source circuit is verified. According to the temperature drift of the

temperature correction based on ADC and comparator is proposed. First, the two-pixel array is used as a reference column for temperature correction, so as to reduce and convert 1V to generate a reference voltage of the comparator or ADC, when the reference voltage is the same voltage as the input voltage. When the reading circuit uses the comparator as the analog-to-digital conversion IP, the input voltage and output voltage of the comparator are both temperature-related voltage signals, so that the temperature correction mode of the pixel device is realized. Secondly, when the reading circuit with ADC as the analog-to-digital conversion IP, with the ADC multiple digital output signal as a reference, ADC reference voltage also rely on two reference column, while the other basic readout as the normal pixel read out, the basic column and the normal read out, the output signal of two ADC, the value is a fixed value, so by the constant value to correct each normal pixel readout, realize the temperature correction with ADC analog conversion readout [11].

Wang Hao of University of Electronic Science and Technology proposed an improved LFSR to make it more suitable for RNS in random calculation forward conversion and obtain error-free random bit flow conversion circuit. The conversion circuit based on the addition counter is proposed, using the cycle counter that must exist in the random calculation system as the addition counter of the conversion circuit to reduce the resource consumption of the conversion circuit through logic. The intercorrelation between the random bit streams using SCC, respectively, both meets the scenarios where the random bit flow is irrelevant. In all random calculation scenarios using two or one multiplexers, according to the idea of uniform distribution, the selected end bit stream $P=\frac{1}{2}$ can use the binary frequency circuit instead of the original uniform distribution generation circuit, to achieve the purpose of saving resource consumption. It proves the feasibility of using a temporal circuit to construct a complex random computing unit Stancombined with the correlation insensitivity of the input end of the multiplexer, and proposes a way to realize the error-free random comparator without changing the model of the existing random comparator. The number of states of the Stanh in the proposed error-free random comparator is only $N=4$ with lower resource consumption compared with the existing random comparators. Through the cascading error-free random comparator, this paper obtains a random median filter system with high accuracy and low overhead, which is packaged as a universal and parameter-configurable random calculation median filter IP. Compared with the weighted binary median filter system, LUT resources are reduced by 41.23% and the power consumption is unchanged; Compared with the existing randomly calculated median filter system, LUT resources are reduced by 53.65% and power consumption by 0.88%. According to the correlation sensitivity of the input end, the implementation of the error-free random absolute value function is proposed according to the properties of the scaled random adder. Both are combined to obtain a high-precision random Roberts edge detection system. Because the simple optimization effect of the computational structure is not ideal, the Sobel edge detection system based on random calculation is proposed, packaged as a universal and parameter configurable random calculation edge detection IP. Compared with the weighted binary edge detection system, LUT resources are reduced by 46.66% and power consumption by 2.68%; compared with the existing random calculation system, LUT resources are reduced by 28.88% and power consumption is reduced by 1.80% [12].

3.2. Application in the direction of signal processing

Hao Chen who is a student of Xi'an Jiaotong University presents a 14 bit I-ADC with chopper steady zero and self-calibration techniques for ultra-low frequency signal measurement. The ADC in this paper adopts a first-order structure, which can achieve lower power consumption and smaller chip area. The ADC circuit is designed using the DongBu 0.5 μ m BCD process. Simulation results show that the absolute value of ADC conversion error is 21 μ V, DNL 0.12 bit, INL 0.21 bit, and the average current consumption of the modulator is only 20 μ A. The layout area of the modulator is only 150 μ m and 310 μ m [13].

Kangqiao Ren studies the error of the original grating signal, and uses the connection between the collected signal and the model parameters to analyze the amplitude deviation coefficient, DC component and phase deviation of the position of the signal, see whether the signal quality meets the

requirements, and compensate for the error to get the modified Moore stripe signal. The preprocessing circuit for the grating Moore stripe signal was designed and fabricated. This includes, the absolute value processing circuit, zero comparison circuit, comparator circuit, through the grating more stripe signal 8 times segmentation and absolute value processing, the hardware circuit of the complete performance test, after the preprocessing circuit signal has high signal quality, can be directly input to the ARM development platform for high multiple of software segmentation. The subdivision software based on ARM is designed to preliminarily realize the function of processing the input signal and uploading the data through the serial port. The amplitude segmentation method of grating signal can be preliminarily realized. However, due to the unknown interference of the ground end of the development platform used, the signal input to the ARM development platform is seriously polluted, and the next error correction process is not ideal. Left a regret for the actual realization of this paper [14].

3.3. Challenges facing the Institute

Absolute comparator studies face specific challenges that may differ compared to other types of comparator studies.

The first is the complexity of the definition. One of the first challenges that the absolute value comparator needs to address is how to accurately define and capture "absolute values". The definition of "absolute value" may vary in different fields and applications, and may even be ambiguity. Therefore, researchers need to devise a general and specific definition to be applied in different contexts. Next, the data acquisition and preprocessing. Obtaining and processing data related to absolute values may be more difficult. In some cases, data on absolute values may need to be collected from specific sensors or devices that can be expensive or unavailable [15]. In addition, outliers and missing values may be faced in the process of data preprocessing, so appropriate treatment methods should be adopted. Then is model building and evaluation. Designing and training models suitable for absolute value comparisons is a challenge. These models need to be able to accurately predict absolute values, and to maintain robustness across different contexts. Evaluating the performance of these models also requires taking into account the properties of absolute values, such as how prediction errors are defined and calculated [16]. Finally, the real-time performance and efficiency. In some applications, absolute value comparators may need to predict in real time and need to be highly efficient. Therefore, designing efficient algorithms and models and optimizing the utilization of computational resources is an important challenge.

To address these challenges requires interdisciplinary research and collaboration, involving expertise and technology in machine learning, data science, domain knowledge, and more.

4. Conclusion

This paper starts with the most basic four-digit absolute value comparator to explore and clarify its working principle. This paper divided the entire circuit into two parts, designing an absolute value calculator and comparator. Optimize and design the resulting circuit, and calculate the relevant parameters. The optimized circuit energy consumption is 19.26. Then the extended application of comparator is introduced, and the application of comparator in image sensor positioning, such as optimization study of random calculation and application in image enhancement, and research on high-precision readout system of FGMOS image sensor; the application in signal processing direction, such as high-precision low-power incremental analog-to-digital converter for ultra-low frequency signal measurement, and research on grating subdivision technology based on ARM. Finally, this paper introduces the challenges facing the comparator development and prospects the future development.

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