

Principal and performance analysis of three typical comparators

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Abstract. This paper discussed 3 innovative comparator topologies proposed in last several years. Depends on the target applications, each of the 3 designs achieved significant performance gains. Compared with conventional design, the comparator with self-calibrating technique has low offset voltage, small die area, low noise, and low power consumption. The comparator with regeneration operating midway realizes dramatically low operation delay with acceptable power consumption. The comparator with latch structure on amplifier stage implements circuit with high speed under low supplied voltage.

Keywords: Comparator topology, self-calibrating technique, comparator with regeneration operating midway

1. Introduction

Comparator is a widely used element in modern mixed signal systems. It is popular in applications like memory sensing circuits, data receivers and analogue to digital converters. The conventional comparator usually consists of an amplifier stage and a regenerative (evaluation) stage. For a comparator design, speed, power consumption, offset voltage, input referred noise, robustness, and area are six characteristics we usually considered to measure the performance of the comparator topology. Depends on the target application, a variety of structures are proposed to satisfy several of the performance above.

In the paper, 3 important designs of the last 10 years have been studied and discussed. In the process, some ideas about implementation have been proposed, and something can be improved in the 3 architectures have also been listed.

The first one is a comparator with self-calibrating technique, which is designed for low offset voltage, low noise with low power consumption and small die area. In some applications with high frequency and high resolution, it also has an advantage of speed. The main idea of the design is using digital circuit and charge pump to eliminate the offset voltage by testing the output when inputs are equal [1]. The second design is a comparator with regeneration operating midway. Its highest priority in design is speed. The main idea of the design is to reduce delay by starting the regeneration phase in midway. So, the structure changed the way connecting amplifier and latch, which has been confirmed that successfully achieve its goal [2]. The third design is the comparator with latch structure on amplifier stage. This structure is proposed to solve the problems in applications aiming for high speed with low supply voltage. The idea of the circuit is to apply the positive loop of the latch to amplifier stage and solve all design problems followed by it. After simulation and measurement, the result is good [3].

The paper is organised as follow. The analysis and discuss of the 3 designs in section II, the comparison of the structures in section III and section IV concludes all things in the paper.

2. Architecture of the 3 comparators

2.1 The comparator with self-calibrating technique

In conventional comparator design, the power consumption of the amplifier is too large due to the static current, and it is impossible to realize a wide bandwidth amplifier [1]. Besides, decrease in drain

[illegible]

The suggested design includes a charge pump, offset compensating current sources, and a comparator [1]. When it is in calibration mode, all input nodes are set to the common-mode voltage V_{cm} , the output totally depends on offset voltage. Then the output is digitally converted to determine whether to charge or discharge the charge pump by controlling current source I_{cp} . So, the control voltage V_c will keep changing until reaching offset voltage. When calibration mode is completed, all input nodes are switched to input signals, and evaluation is started with little offset voltage.

Timing diagram of the proposed 2-stage latch. The diagram shows three signals over time: 2nd stage CMP_{out} , 1st stage DI , and CLK . The 2nd stage CMP_{out} signal transitions from -1.0V to 1.0V at time t_L . The 1st stage DI signal transitions from -1.0V to 1.0V at time $t_L + 50-100ps$. The CLK signal has two triggers: the first stage latch trigger at t_L and the second stage latch trigger at $t_L + 2.4ns$. A note indicates that the proposed comparator uses the DI nodes voltage instead of the CLK for the 2nd stage latch timing.

Fig. 3 shows the signal behaviours of 2 comparators. Compared with conventional one, proposed comparator uses the voltage of Di nodes rather than $\sim\text{CLK}$ to timing second stage latch. It not only increases the sensitivity of proposed comparator, but also relaxes the clock driving requirement.

Higher sensitivity means lower noise, and relaxing clock requirement means that the circuit can be implement easily. More specifically, the delay of comparator T_d for the proposed structure is within 50~100 ps, so the delay between CLK and $\sim$ CLK for conventional comparator with same parameters must be less than 50ps. It is a very accurate condition that can hardly be satisfied.

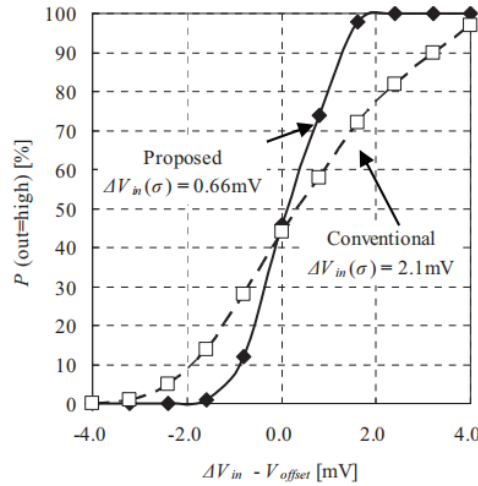


Fig. 4 Simulation-based noise distribution.

The results of the Spectre transient noise simulation for the comparator noise are shown in Fig. 4. The equivalent input noise of the suggested comparator is 0.66 mV, compared to 2.1 mV for the conventional one. The proposed comparator's input noise is around three times less than that of the conventional one. Besides, from the figure we can also learn that the possibility of output 1 is less than 50 percent when $\Delta V_{in} - \Delta V_{offset} = 0$, and $|\Delta V_{in} - \Delta V_{offset}|$ value for comparator output 0 with 100 percent possibility is less than output 1. Therefore, we need to consider the possibility asymmetry and set the threshold ΔV_{in} to fix it in our own design. Moreover, due to the 100 percent value for proposed comparator is 2 times lower than conventional one, we can use such high sensitivity characteristic to implement some circuits like flash ADC with higher resolution.

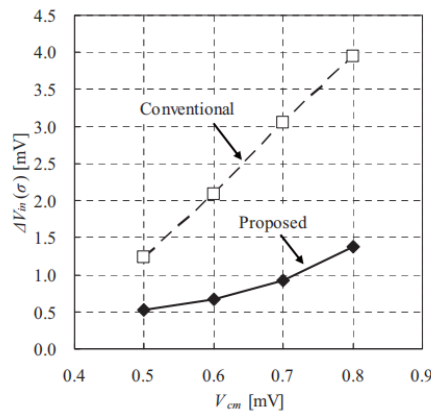


Fig. 5 Calculated from the cumulative noise distribution versus common mode input voltage, the simulated equivalent input noise is given as $\Delta V_{in}(\sigma)$.

Fig. 5 compares the common mode input voltage V_{cm} to the equivalent input noise $\Delta V_{in}(\sigma)$. As opposed to the conventional comparator's 2.8 mV increase, the proposed circuit's $\Delta V_{in}(\sigma)$ increases by just 1.0 mV when V_{cm} shifts from 0.5 V to 0.8 V. Therefore, the input noise of proposed structure is not only lower than conventional one but also more unsensitive to change of common mode voltage. It means that the proposed comparator can be applied to circuits with large V_{cm} variation range. Besides, the figure also shows that input noise would increase as the increase of common mode voltage. So, the choice of common mode voltage could largely influence the accuracy of evaluation. In the range 0.5mV ~ 0.8mV, 0.5~0.6mV would be the best choice. It is because the range of 0.5~0.6mV correspond to both the lowest input noise and the lowest increase rate of noise.

After simulation, the design successfully achieves goals of low offset voltage and low noise. Moreover, when applying such a self-calibrating technique to practical applications, we can win more advantages. For example, we can flexibly alter the complementation range by changing the current of charge pump I_{CP} . There is no need for reference voltage in calibration, thus we do not need calibration data word outside comparator anymore and die area could be reduced dramatically. Because lots of comparators can do self-calibration simultaneously, the delay caused by calibration time can be reduced largely in a system that lots of comparators are needed, like flash type ADC. Moreover, due to there is no need for adding a pre-amplifier to cancel offset voltage, the power consumption could be low.

However, there is still something noteworthy about the proposed design that the paper failed to mention. Firstly, we do not know the specific delay of one proposed structure. So, when it is used in low resolution ADC, the delay may be larger than conventional design. We need to spend time to figure out whether it is suitable to use proposed design in applications with low resolution. Secondly, because compensation range is related to I_{CP} , power consumption may be large when wide compensation range is required. Therefore, we need to reconsider the power consumption when wide compensation range is required and use simulation tools to get the correct result.

For these problems failed to be discussed in this paper, we can figure them later and try to pick up new ideas to improve them.

2.2 The comparator with regeneration operating midway

A clocked comparator includes two stages. One is to receive the input signals, the other one is a regenerative stage. When designed for low power goals, the regenerative stage begins to operate from supply or ground level [2]. Due to the latch calculates to its stable state beginning from the reverse one, the comparator speed is not offered the utmost priority in this scenario [5]. When comparator speed is prioritised above all else, the regenerative stage should operate halfway between the power supply and the ground [6]. However, the energy consumption of static current would be relatively high. In this study, a high-speed clocked comparator design is presented.

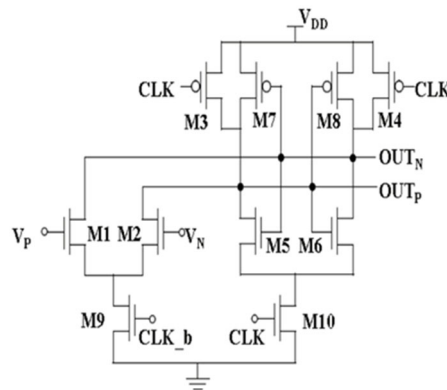


Fig. 6 Proposed comparator design.

In Fig. 6, the presented comparator is displayed. It composed of two stages. The M1–M4 and M9 transistors make up the first stage, which is the amplification stage. The M5–M8 and M10 transistors make up the second stage, which is the regeneration stage. The circuit works in the amplification phase when CLK is low. The phase amplifies the difference between V_p and V_n , and the outputs of differential part are then given to the regeneration stage's inputs. Meanwhile, the regeneration stage's functionality is prohibited. Whenever CLK enters its high state, the circuit operates in regeneration phase. The differential inputs that have been enhanced V_n and V_p are evaluated by the regenerative stage.

To test the speed and other performance of the presented comparator, the conventional circuit and the presented one are simulated and measured. The results are shown as follow.

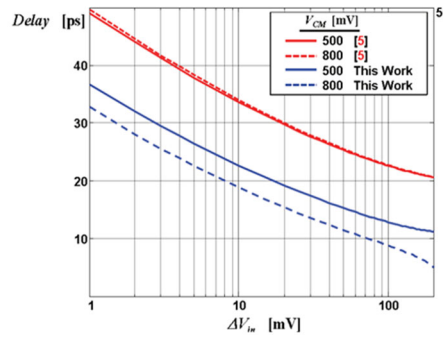


Fig. 7 Comparator delays vs the difference in input voltages in simulation. The reference circuit's delay is displayed by red curves. The proposed circuit's delay is represented by blue curves.

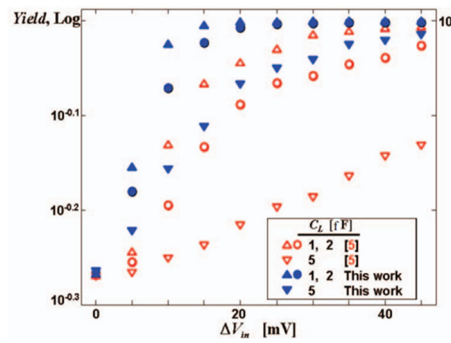


Fig. 8 Comparator yield simulation versus input voltage variation. The reference circuit's yields are represented by red symbols. The yields of the suggested circuit are displayed by blue symbols.

Fig. 7 displays the results of simulations of the proposed and reference systems' delays versus input voltage differences (ΔV_{in}) at two bias voltages. The outcome demonstrates that the suggested circuit not only has delay roughly 35% less compared to the reference design, but also has a delay reliance of 10% on the common mode voltage in the interval of interest. Moreover, the figure also shows that delay would be reduced linearly when input voltage difference increases. If the voltage difference of inputs is 100mV, the delay could be about 3 times lower than it is 1mV. It means that the delay could be lower when resolution of the applications is not high.

Because the delay of the regeneration phase limits the performance of the proposed circuit and supply transitions add to the input referred noise, we perform a Monte Carlo simulation for 1000 samples of each comparator at various load capacitors. The yield, which is defined as the quantity of accurate decisions per 1000 devices, is calculated relative ΔV_{in} as illustrated in Fig. 8. This figure depicts the robustness of both the proposed and reference designs. For proposed design, about 100 percent accuracy can be achieved if ΔV_{in} is larger than 20mV. While in reference design, it should be at least 30mV. The result indicates that the proposed design support applications with higher frequency and higher resolution compared with the reference design. Besides, by comparing the six curves we know that the capacitance C_L will influence the yield (robustness) of the circuit. The larger C_L is, the worse robustness of the circuit is. So, in our design we should make C_L small to increase the stability of the circuit. According to the figure, C_L less than 2 has little effect on yield, thus 2 would be a good choice for C_L . In the suggested design, the energy used during the amplification phase is mostly what determines the amount of energy used. Because of this, the proposed circuit is not suitable for low-power, low-frequency applications. Simulated results are used to determine the energy consumption for the highest frequencies that can be used on the two circuits in real-world applications. It is 461W at 7.2GHz for the suggested circuit, compared to 310W at 5.5GHz for the reference circuit. This indicates that the energy consumptions of the two designs at their highest frequency are comparable. So, power consumption is not a problem when we apply the proposed structure for high frequency applications.

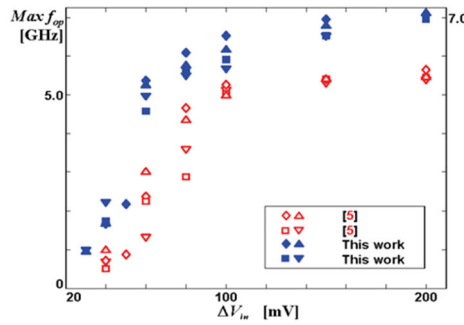


Fig. 9 Four devices were used to measure input voltage differences vs maximum operating frequency (f_{og}). The maximum f_{og} of the reference circuit is represented by red symbols. The planned circuit's maximum FOP is represented by blue symbols.

Fig. 9 depicts the test findings at the maximum working frequency of the 4 chips implemented with presented and reference topologies. The findings unequivocally demonstrate that the suggested circuit may run effectively at a higher frequency than the reference design when the input differences V_{in} are same. In addition, according to the figure we can also found that the maximum frequency will increase fast firstly and turn stable later along with the growth of ΔV_{in} . Therefore, we can use this characteristic to increase the frequency by reducing resolution in our design. However, because ΔV_{in} larger than 100mV have little influence on frequency, we should restrict ΔV_{in} under 100mV when changing it to increase frequency.

Simulation and measurement results verify that the design successfully realizes high speed, strong robustness, and acceptable power consumption. In addition, when applying the structure in practical world, there is extra profit. Due to larger gain means lower offset voltage, we can sacrifice power consumption to pursue higher accuracy and resolution in some situations, which is something we can adjust flexibly in our design.

However, there are still things that can be improved. At first, because the essence of the design is to win offset cancelling and speed performance by increasing power, the power consumption is a problem needed to be improved, especially in low frequency and high-resolution applications. Besides, in the design we just cancel the offset of regenerative stage, so how to eliminate the offset of the differential amplifier is another problem. Moreover, the input referred noise is also failed to discuss in the paper.

For these problems needed to be improved and have not been discussed, we can try to solve them later and pick up new ideas to ameliorate them.

2.3 The comparator with latch structure on amplifier stage

Low supply voltages are currently trapping the high-speed comparators in UDSM CMOS technologies, so we need to design high-speed comparators working with small supply voltage [7]. In the given technology, larger transistors are employed to make up for supply voltage loss and achieve high speed, but this requires more chip space and power [3]. Many approaches have been devised to address the low-voltage design issues, including supply boosting methods [8], [9] and methods using body-driven transistors [10]. However, they introduce reliability problems [3]. Therefore, a new comparator structure is proposed in the paper.

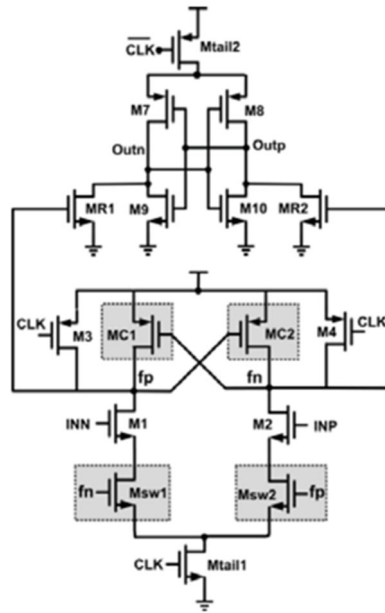


Fig. 10 structure of the comparator with latch amplifier stage.

The structure of the design presented in this paper is shown in Fig. 10. It is an improved circuit on the basis of the double-tail architecture. Principal concept of the design is that applying the positive looping feature of latch in amplifier stage to speed up the change of voltages at f_n and f_p . To implementing it, we add M_{c1} and M_{c2} in the stage to form a latch. Moreover, in order to prevent the supply to ground static current caused by M_{c1} and M_{c2} , we also add M_{sw1} and M_{sw2} which are controlled by V_{fn} and V_{fp} respectively to open the circuit.

To applying the principle above to implement the practical circuit, there are still some simulations must be made. The results are shown below.

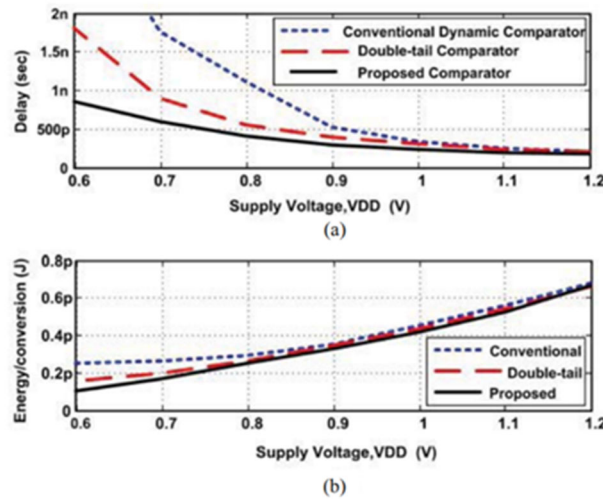


Fig. 11 (a) Simulated Post-Layout delay. (b) the energy required for each conversion in relation to the supply voltage ($\Delta V_{in} = 50$ mV, $V_{em} = V_{DD} - 0.1V$).

Fig. 11 displays the simulation results for the delay and energy per conversion of the dynamic comparators mentioned above displayed against supply voltage change. From Fig. 11(a) we found that the delay of the presented comparator is dramatically decreased at low-voltage supplies compared with the other two structures. When the supply voltage is high, all structures perform similarly. It is clear that the double-tail design operates more quickly and operates at lower supply voltages when using almost the same amount of energy as the traditional dynamic comparator. Comparing the suggested comparator to the traditional double-tail circuit, it is even superior.

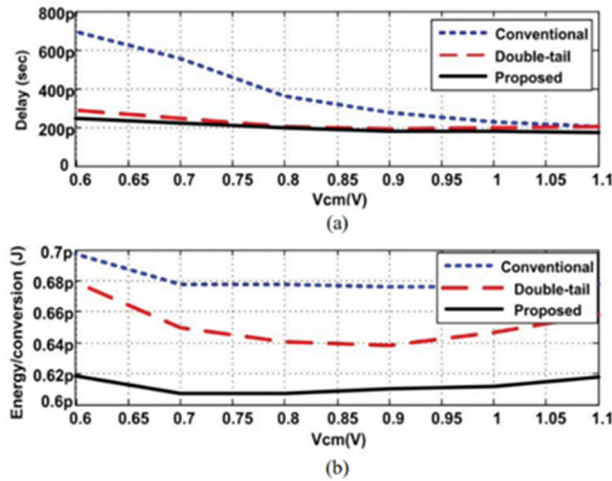


Fig. 12 (a) Simulated delays after layout (b) energy for each conversion in relation to the input common-mode voltage ($\Delta V_{in} = 50$ mV, $V_{DD} = 1.2$ V).

Fig. 12 shows the simulated performance of the circuits in relation to the common mode voltage (V_{cm}). From the figure we can conclude that the double-tail comparators' delay is insensitive to the change of the common-mode voltage compared with the conventional dynamic architecture. Therefore, we prefer to choose double tail designs in applications with wide common-mode range. Moreover, the power consumption of all 3 topologies is nearly same, so we do not need to consider power in our design to choose one structure of the 3 options.

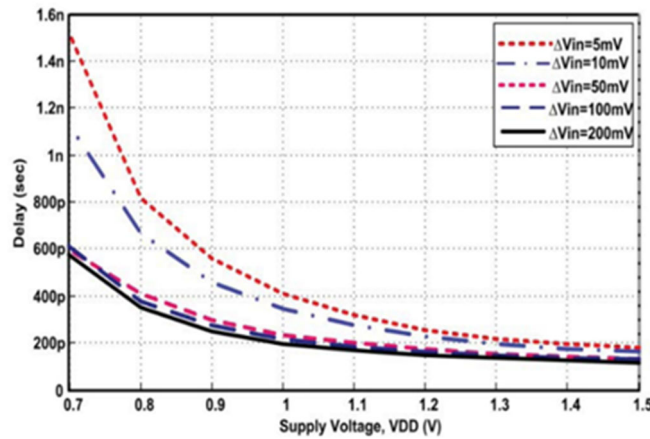


Fig.13 Comparison between supply voltage and the planned comparator's delay (V_{DD}).

Fig. 13 illustrates how the comparator delay depends on power supply level at various differential input voltages. It is clear that both large V_{DD} and large ΔV_{in} leading to low delay, and the influence of ΔV_{in} would be weakened by high V_{DD} , while the influence of V_{DD} also be weakened by large ΔV_{in} . This characteristic indicates that we can realize small delay applications with low V_{DD} by reducing resolution or realize small delay applications with high resolution by increasing V_{DD} . It all depends on the target we apply for. In addition, noting that both 2 influences above are not linear, so it would be reasonable to restrict V_{DD} within 0.7~0.9V and ΔV_{in} within 5~50mV.

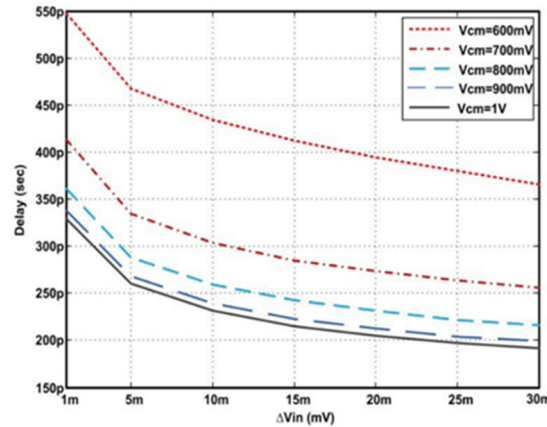


Fig. 14 The proposed comparator's delay in relation to input voltage difference (V_{in}).

Fig. 14 depicts the simulated comparator delay in relation to differential input voltages under different common-mode voltages (V_{cm}). Generally, in each V_{cm} , the delay tends to lower as input voltage difference increases. So, improve speed by reducing resolution is feasible. But ΔV_{in} should not exceed 10mV, because too large ΔV_{in} has little influence on delay. We can just change ΔV_{in} flexibly between 1mV~10mV. Moreover, the delay also depends on the value of common-mode voltage. Large common-mode voltage usually corresponds to small delay. Because such correspondence is not linear, in our design, the range of common-mode voltage between 700mV~1V is good.

However, although the circuit has excellent performance in delay and reasonable power consumption, there is still other characteristics the paper failed to discuss or have not improved. For example, the robustness of the circuit proposed is unclear, there is no measure to cancel the offset voltage. We can solve these problems in our later study.

3. Comparison

The 3 comparators are designed for different applications, and all of them achieve their goals successfully. So, it is unnecessary to compare the 3 structures for a same characteristic. The self-calibrating comparator is attractive for high resolution field like flash type ADC. The comparator with regeneration operating midway is suitable for application requiring high speed with limited common mode range, such as ADCs of moderate number of bits. The comparator with latch structure on amplifier stage is topology particular for low supply voltage, high speed applications.

4. Conclusion

The paper has studied 3 designs and discussed them in view of various characteristics including delay, power, area, noise, offset, and robustness. Every design has been verified achieving its design target. The comparator with self-calibrating technique dramatically improves its input offset voltage from 13.7 mV to 1.69 mV, while keeping the comparator noise level that is three times lower than the conventional topology. The comparator with regeneration operating midway achieves the speed improvement that operates averagely 31% faster than the reference one with acceptable power consumption in high frequencies. The comparator with latch structure on amplifier stage halving the delay with similar energy per conversion at the situation where voltage supply is low enough.

However, all the 3 design still have some problems could be improved. Those are things we would discuss next step.

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