Performance Analysis of Low-Power CMOS Dynamic Comparators

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Abstract. This paper studies four structures of CMOS dynamic comparators introduced in recent years. Based on conventional double-tail comparator, a comparator with a tail capacitor prevents output nodes of preamplifier from completely discharging to reduce energy consumption. Another comparator with a cross-coupled pairs achieves the same purpose of the first design. A comparator adds a floating inverter amplifier (FIA) to realize both dynamic bias and current reuse, achieve low energy consumption and be insensitive to the VCM. The triple-latch feed-forward (TLFF) comparator decreases delay conspicuously.

Keywords: CMOS dynamic comparators introduced, floating inverter amplifier (FIA), triple-latch feed-forward (TLFF)

1. Introduction

Dynamic comparators are the important part of analogue circuits. This paper studies four low-power and high-speed dynamic comparators owing to their importance.

Strong-Arm (SA) dynamic comparators have strong positive feedback to enable fast decisions and full swing outputs [1-2]. However, Strong-Arm latch-type dynamic comparator has some disadvantages such as: the large noise and voltage headroom. Double-tail comparator is used to replace it and can separate the pre-amplification from the latch operation, which is helpful to optimize noise, power, offset and speed independently. Nevertheless, this conventional design costs much energy and suffers from a large delay and noise, which does not meet design requirements and needs further improvement.

A comparator with a tail capacitor is proposed to optimize the energy efficiency by preventing output nodes of preamplifier from completely discharging. Besides, this design decreases the noise contribution and stabilizes the common-mode voltage level. [3-5]

A comparator with a cross-coupled pairs also achieves the same purpose of work one. This topology is a low area solution, which causes higher delay. [6]

It is an issue that the delay cannot be effectively decreased for decades. Therefore, a TLFF comparator is introduced to optimize the delay for high speed application by adding an extra bypassing feed-forward path. [7-8]

A comparator with a FIA realizes current reuse, boots g_m/I_d, insensitivity to the variation of V_{CM} and decreases energy consumption. A floating capacitor is used to power FIA and make the pre-amplifier insensitive to V_{CM}. [9-10]

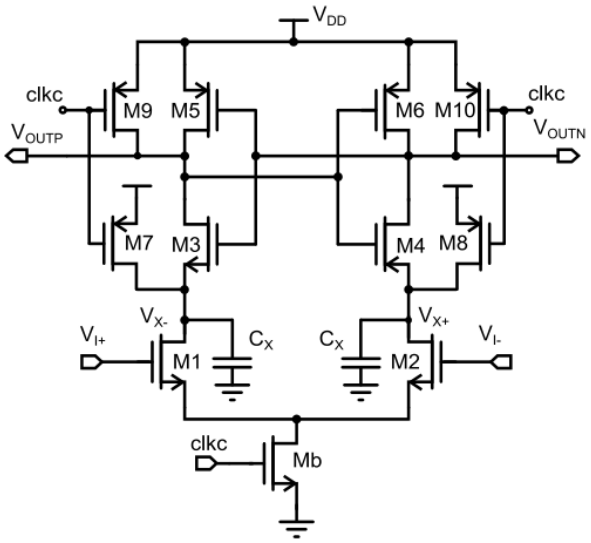

Figure 1. Conventional SA latch-type comparator.

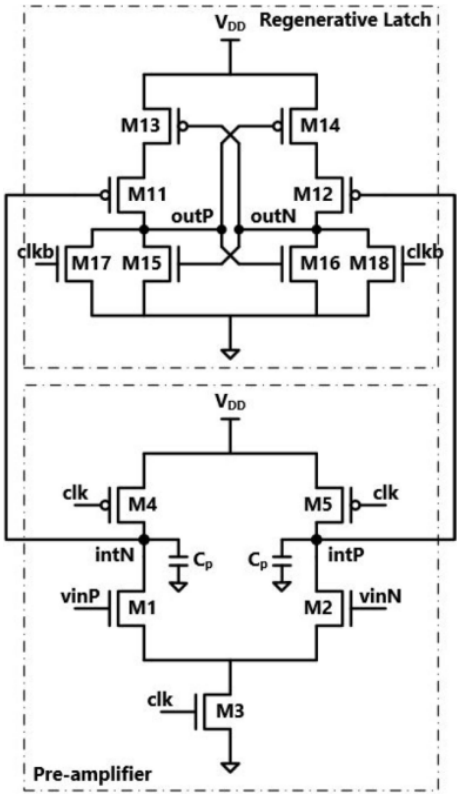

Figure 2. Classic double-tail latch-type comparator.

This letter is organized as follows. Four comparators are recommended in details in Section 2. Section 3 is a comparative table and analysis of the four designs. Section 4 makes a conclusion of the letter.

2. Architecture of Comparators

2.1 A Dynamic Bias Comparator

This circuit is an improvement of the Elzakker's comparator. Its schematic is shown in figure4. It uses a tail capacitor in order to stop output nodes of preamplifier from totally discharging based on the dynamic bias technique. The tail current will charge the tail capacitor and increase V_{GS} of M_1 and M_2, which achieves the dynamic bias.

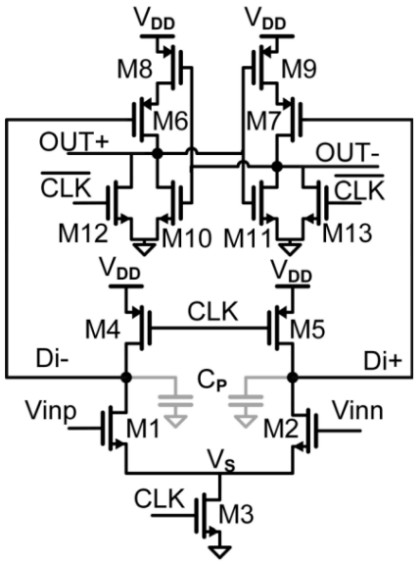

Figure 3.The Elzzaker's comparator.

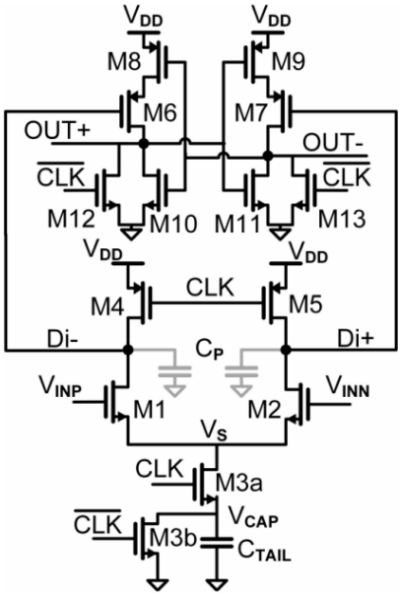

Figure 4. The introduced circuit.

For the Elzakker's comparator, the output of preamplifier completely discharges. Thus, it consumes $2 * C_p * V_{DD}^2$ for every comparison. However, in this architecture, the preamplifier consumes $C_p * V_{DD} * (V_{D1}+V_{D2})$.

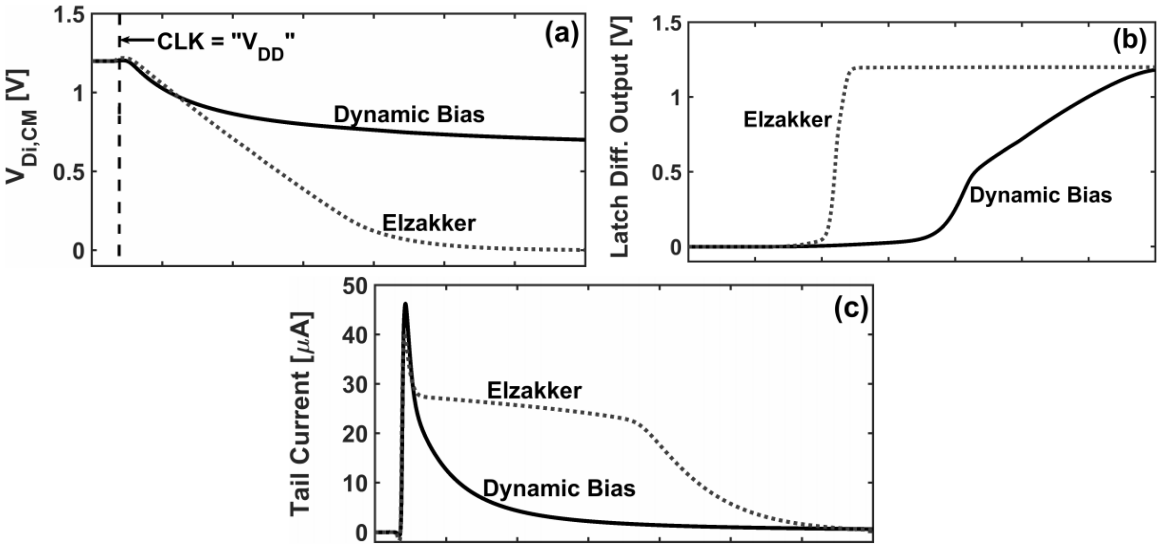

Figure5. (a)VCM, (b) Latch differential output, (c)Tail current.

Figure 5(a) shows that the V_{CM} of the introduced circuit drops to nearly 650 mV per comparison and the V_{CM} of the Elzakker's comparator totally drops to ground. This figure proves that the proposed circuit achieves its design objective. Figure 5(c) shows that the tail current of the introduced circuit is smaller than the traditional comparator.

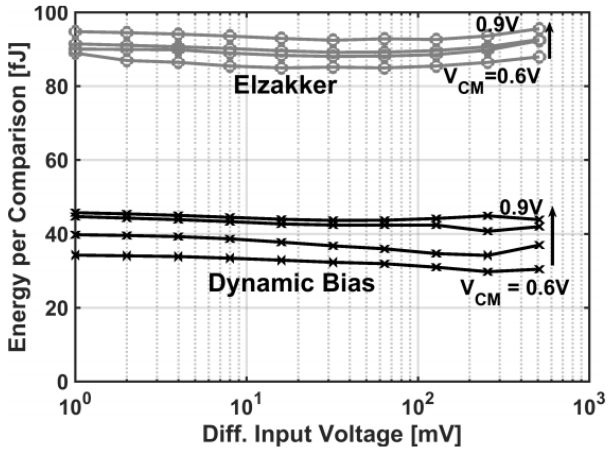

Figure 6.Energy consumption of different input voltage for various VCM.

Figure 6 shows the prototype comparator consumes more energy than the introduced circuit for different V_{CM}.

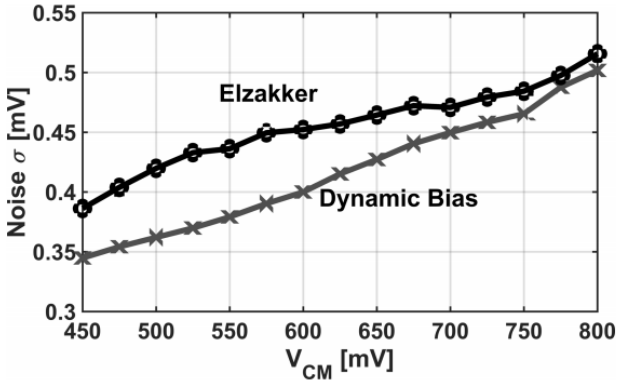

Figure 7.Input referred noise for different VCM.

Figure 7 expresses that this circuit also has a better noise performance than the Elzakker's comparator. The noise increases with V_{CM} increasing. The noise for weak inversion operation is

$$\mathrm{E}\left[v_{n,WI,in}^2(T_{INT})\right] = \frac{2nKT}{C_p * \Delta V_{Di,CM}(T_{INT}) * (\frac{gm}{I_{CM}})_{WI,T_{INT}}}. \quad (1)$$

Maximizing the g_m/I_d for M_1 and M_2 can get the smallest noise.

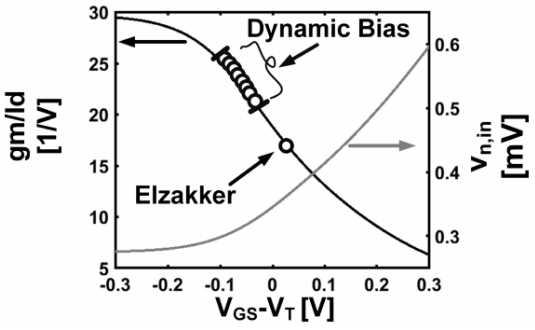

Figure 8. g_m/I_d and $V_{n,in}$ across V_{GS}–V_T.

Figure 8 indicates that the g_m/I_d increases with decreasing V_{GS}-V_T. The range of V_{GS}-V_T of work one is smaller than the prototype comparator. Thereby, dynamic comparator has a good noise performance than the Elzakker's comparator.

Figure 5(b) shows that the latch output of the introduced circuit consumes more regeneration time than the conventional comparator because M_6 and M_7 of the proposed circuit work at a low overdrive voltage.

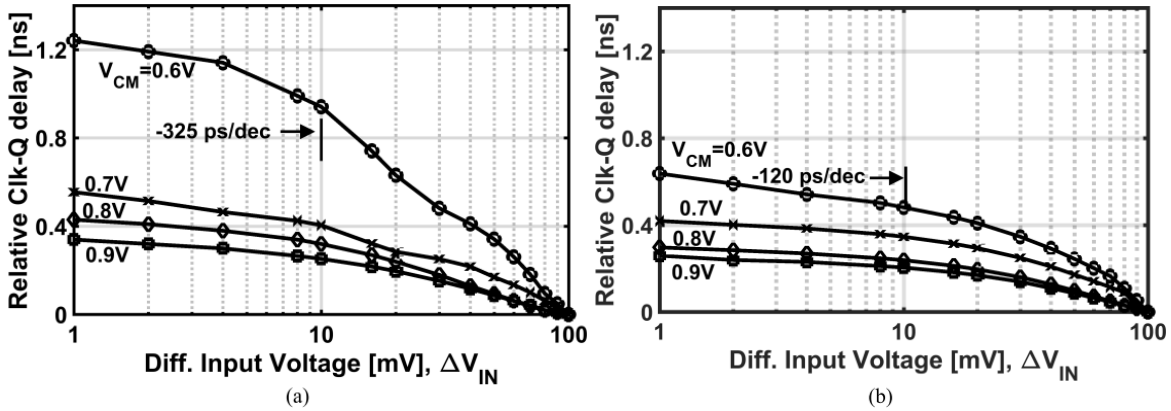

Figure 9.CLK-Q delay of (a) the introduced circuit and (b) the conventional circuit.

From figure 9, CLK-Q delay of the introduced circuit is nearly 2 times higher than the conventional circuit when V_{CM} is from 0.7 to 0.6V. It is the latch working in weak inversion region that causes higher delay for V_{CM}=0.6V. Overall, the CLK-Q delay of the introduced circuit is larger than conventional circuit.

2.2 A Low-Power Dynamic Comparator

This circuit is an improvement of conventional double-tail comparator. It uses a cross-coupled pairs to avoid output nodes of preamplifier from completely discharging, which can decrease energy consumption in each comparison and without complex logic or additional capacitors.

During the reset phase, intN and intP will be charged to V_{DD}. During the amplification phase, the voltages at intN and intP will decrease. Transistor M22 will turn off completely and intP will become static because the descending rate of intN is faster than intP. IntP and intN approach voltages V_{D1} and V_{D2} below V_{DD} respectively. Energy consumption reduces to $C_p * V_{DD} * (V_{D1}+V_{D2})$.

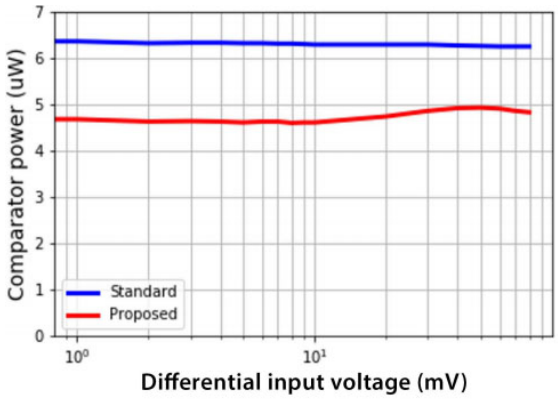

Figure 10.Comparator power across differential input voltage; V_{CM}=0.5V.

Figure 10 expresses that the proposed comparator has a 30% power reduction versus the conventional circuit in the similar noise levels.

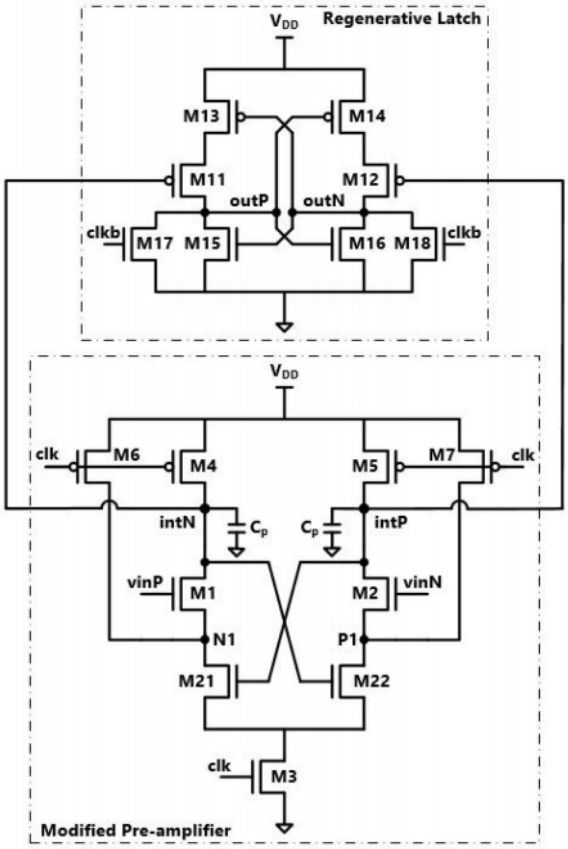

Figure 11.The latch-type comparator with the modified pre-amplifier.

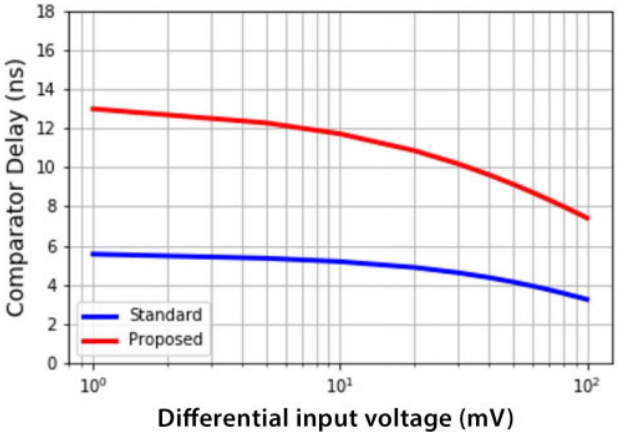

Figure12. Comparator delay across differential input voltage; V_{CM}=0.5V.

Figure 12 indicates that the proposed circuit has worse delay compared to the conventional circuit because it has higher conversion time. Adjusting g_m/I_d can improve this problem.

2.3 A Comparator with A FIA

This circuit is a dynamic comparator with a FIA. Its schematic is shown in figure 13.

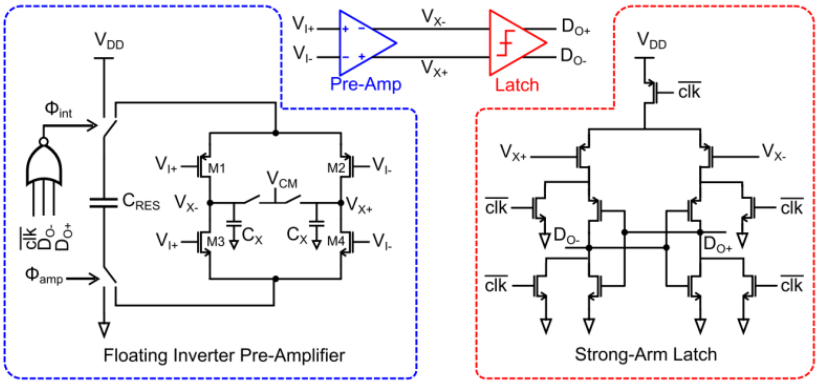

Figure 13.FIA+SA comparator.

The floating capacitor offers an isolated voltage domain for preamplifier. FIA operation is shown in figure 14. The current of input and output of C_{RES} is equal, which makes a constant V_{CM} and ensures the insensitivity of $V_{I,CM}$.

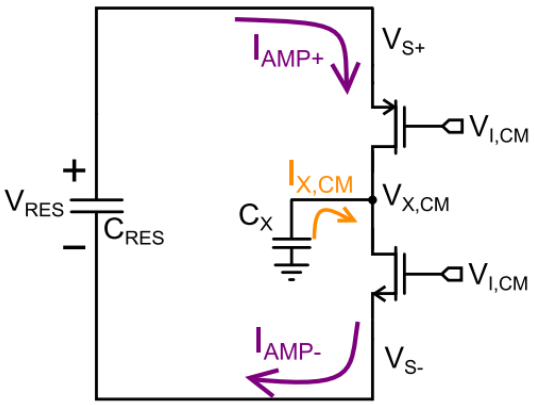

Figure 14.FIA operation.

The figure of merit (FoM) is

$$\mathrm{FoM}_{FIA} = 4nkT \cdot V_{DD} \cdot \frac{I_d}{g_m}. \quad (2)$$

The FoM_{FIA} can be improved by adjusting the g_m/I_d, which represents energy efficiency of a comparator [10].

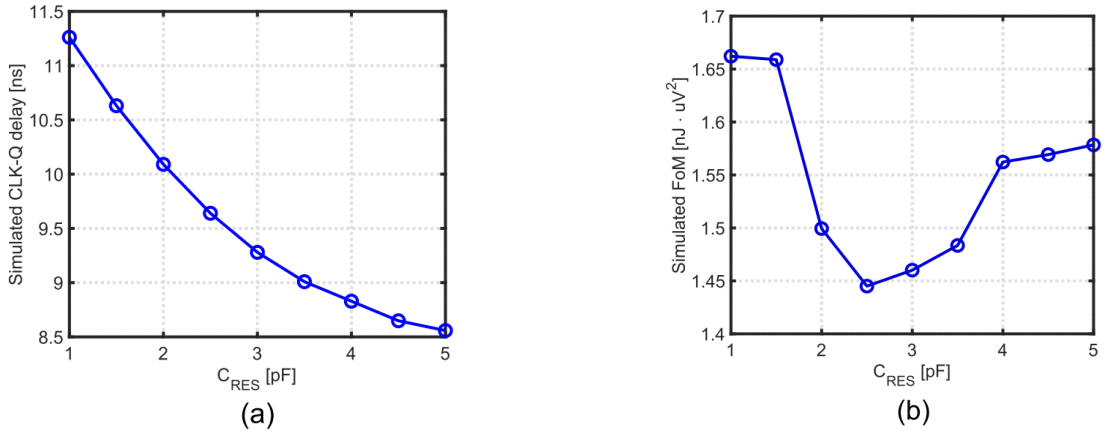

Figure 15. (a) CLK-Q delay and (b) FoM across CRES value.

Figure 15(a) indicates that CLK-Q delay diminishes while the C_{RES} increases. Fig. 14(b) shows the relationship between the FoM and the C_{RES}. The pre-amplification gain cannot repress the noise with a small C_{RES}. However, the large C_{RES} will decrease g_m/I_d. Therefore, this circuit chooses 2pF C_{RES} to balance the demand between the delay and energy efficiency.

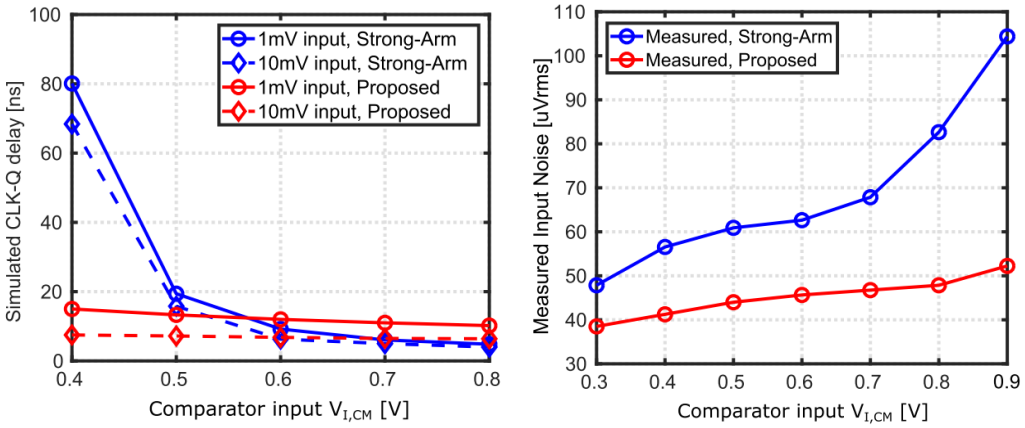

Figure 16. Simulated CLK-Q delay and Figure17.input noise versus $V_{I, CM}$.

Figure 16 shows that FIA+SA is insensitive to the variation of $V_{I, CM}$. Figure 17 indicates that the noise increases while $V_{I, CM}$ increases. Compared to SA, FIA+SA decreases four times noise variation.

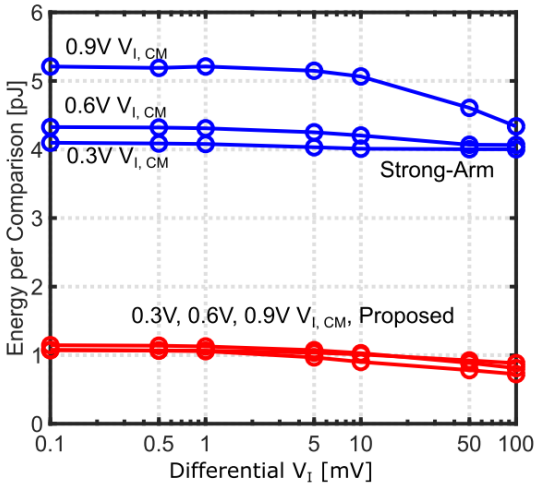

Figure 18. Energy consumption versus V_I.

Figure 18 highlights that the overall energy consumption of FIA+SA diminishes for different $V_{I, CM}$. The current in the SA latch increases and consumes more energy with $V_{I, CM}$ increasing. This circuit achieves over four times reduction of energy consumption than SA.

2.4 A TLFF Dynamic Comparator

A TLFF comparator is introduced to optimize the delay. The detailed circuit schematic is shown in figure 19.

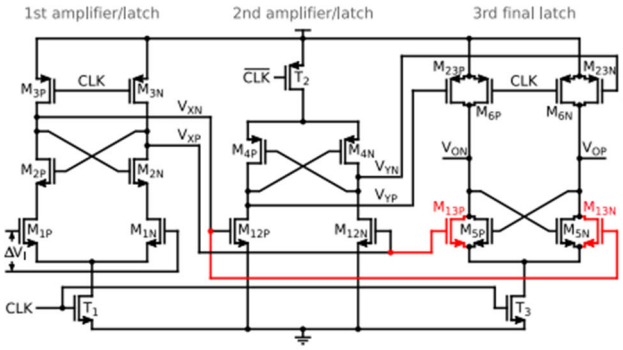

Figure 19. The TLFF comparator schematic.

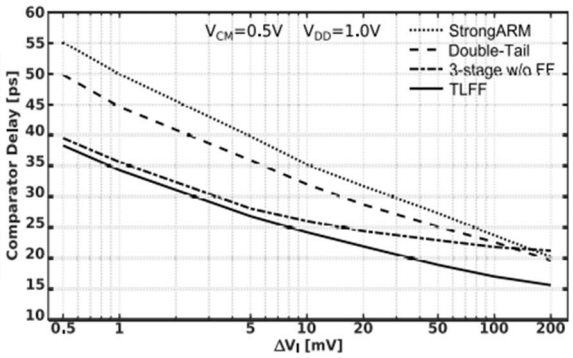

Figure 20. Comparator delay versus ΔV_I.

Transistors M12P/M12N and M23P/M23N reduce the load on their critical nodes as gain and reset stages. The low delay, noise level, high total gain and sensitivity to V_{CM} are achieved by cascaded latches and feed-forward.

Figure 20 shows that TLFF achieves 40% and 30% delay reduction compared to SA and the double tail comparator for ΔV_I=5mV. Overall, TLFF achieves the lowest delay among these circuits

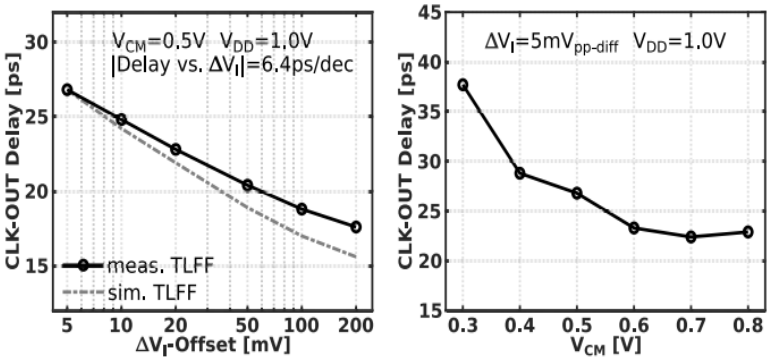

Figure 21. TLFF comparator delay versus ΔV_I and V_{CM}.

Figure 21 indicates that the CLK-OUT delay get lower when ΔVI increases. Besides, the CLK-OUT delay reduces at the range of 0.3-0.6V of VCM and is steady at the range of 0.6-0.8V of VCM. This circuit achieves a low CLK–OUT delay.

3. Performance Summary

Table 1. Performance Summary.

	Standard SA,[4]	FIA+SA,[4]	Cross-Coupled Mechanism,[6]	TLFF, [5]	Dynamic Bias,[3]	Double Tail,[3]
Process[nm]	180	180	65	28	65	65
Supply[V]	1.2	1.2	1.0	1.0	1.2	1.2
Noise [mV]	0.062	0.046	0.220	NA	400	375
Energy[pJ]	4.1	0.98	0.192	0.163	0.034	0.088
Area [μm²]	7700	9800	NA	NA	125	90

Table 1 concludes the specification of comparators studied in this paper. FIA+SA, dynamic bias and cross-coupled mechanism comparator are designed to optimize energy consumption. Dynamic bias comparator attains best energy consumption and reduces the area. Cross-coupled mechanism comparator is a low-area and low-power solution. However, the dynamic comparator and cross-coupled mechanism comparator have higher noise than the FIA+SA comparator. The FIA+SA comparator achieves great noise level and energy consumption while it costs huge area compared to other circuits. TLFF comparator is designed to solve delay problem and it achieves the best delay.

4. Conclusion

The dynamic bias comparator prevents output nodes of preamplifier from completely discharging by using a tail capacitor and achieves a two times energy reduction than the conventional circuit. Overall, the delay of the introduced circuit is larger than the traditional circuit.

The cross-coupled mechanism comparator has a 30% power reduction and worse delay compared to the conventional circuit.

FIA+SA comparator uses a dynamic floating inverter amplifier to realize both current reuse and dynamic bias and achieves over four times reduction of energy consumption than SA while is insensitive to V_{CM}. Besides, compared to SA, FIA+SA decreases four times noise variation.

TLFF comparator optimizes the delay by adding feed-forward path into conventional comparator. It achieves a low delay and reduces the energy consumption and the noise level.

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