The Performance analysis of Low-Power High-Speed comparators

Yichen Li

Faculty of Information Technology, Beijing University of Technology, Beijing, China

Yichen.li@emails.bjut.edu.cn

Abstract. Comparators are the essential block for planning high-speed analog and. This paper presents three inventive designs of the comparators in recent years. First, innovated by classic two-stage comparator, the comparator with a transconductance-enhanced latching stage is suitable for low-power, high-speed operation. Second, triple-latch feed-forward(TLFF) fully dynamic comparator guarantees the maximum possible gain and speed for a specific power across the entire input range. Finally, the comparator with a dynamic floating inverter maximizes efficiency by reusing the current.

Keywords: high-speed analog, triple-latch feed-forward (TLFF).

1. Introduction

The comparator is crucial in many digital and complex systems, for example analog-to-digital converters (ADCs) and microprocessors. These applications push toward higher speed and power effectiveness of comparators. It compares two current or voltage and give related output. A considerable number of boundaries impact the result of a comparator, like energy, delay, and noise level. In recent years, power and delay have been vital specifications. This article mainly discusses three comparators that have different parameters and characteristics.

Modified from the classic two-stage dynamic comparator, the comparator with a new latching stage adds cross-coupled transistors in the structure and a new clock signal to control it. This design presented by Yao Wang in 2019 and his team build up the total effective transconductance of the latch at the threshold of the comparison region and significantly diminishes the delay and power.
The TLFF comparator, improved by Athanasios T. Ramkaj, adds a feed-forward path to the triple-latched comparator, which helps achieve lower delay in a large area and power supply region. As a result, the maximum clock-out delay is around 27 ps, and the delay slop is about 6 ps/decade.

Improved from the classic Strong-Arm design, Xiyuan Tang with his team presented a unique structure of a pre-amplifier adds capacitors. The added capacitors lower the energy consumption and input noise. In addition, capacitors provided isolated voltage domains for dynamic integration.

The article is organized as follows. Section II presents three comparators with their crucial parameter, like delay and power. Section III is a relative analysis of the three comparators, and Section IV concludes the paper.

2. Proposed comparator.

2.1 A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage

Yao Wang with his team devise a two-stage, ultrahigh-speed, low energy cost, dynamic comparator. This circuit was designed in July 29, 2019. The proposed design is to optimize delay and power compare to the conventional two-stage comparator. The schematic of aforementioned design are as follow.

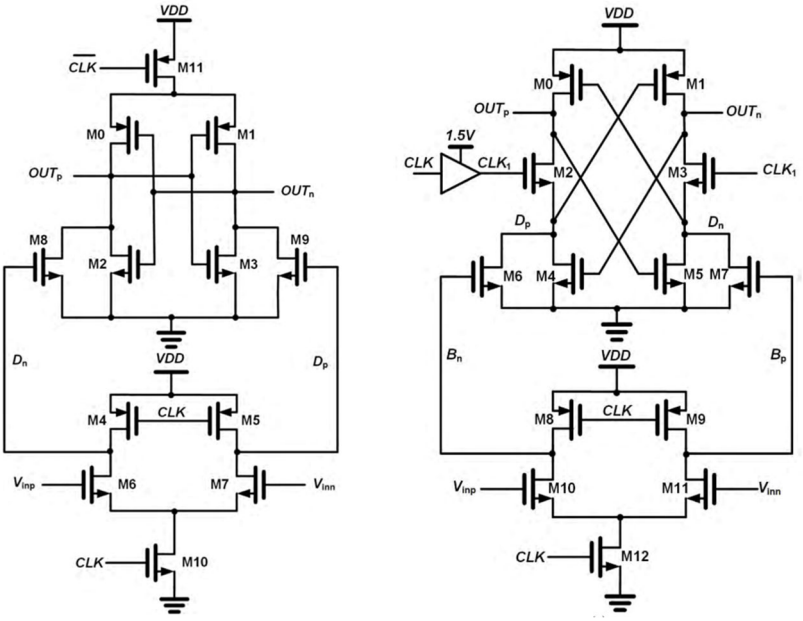

Figure 1. traditional two-stage comparator and proposed comparator.

The new architecture's input stage or pre-amplifier stage is identical to the conventional one. However, the inventive structure is at the latching stage. Compared to the traditional design, the author added a new latching stage at the top side of the comparator. In addition to that, the clock waveform is also added to the system. CLK1 is a signal controlled by CLK signal with a level-shift of about 95 ps delay after calculation. When CLK1=V_{dd}, the proposed comparator's behavior is identical to the classic 2-stage comparator. When CLK1=0, the output voltage is latched. Therefore, the output potential causes the cross couple of both NMOS and PMOS to maintain the overdrive voltage. This feature means when latching at the beginning, the initial voltage is not connected to the ground. When M2 and M3 are off, creating voltage isolation prevents voltage turn back to ground voltage and refers to an initial voltage condition. Add an initial voltage as a precondition, like overdrive voltage, and it can drive the output. This design also lowers the power consumption because of a shorter metastable duration.

When it comes to the formula and study, delay is primarily from two parts, t0 and t_{latch}.

T0 can be estimate from the equation.

$$t_0 = \frac{V_{THN} C_{OUT}}{I_p} = \frac{V_{THN} C_{OUT} \cdot 2\mu_p C_{OX} \frac{W_P}{L_P}}{g_{mp}^2} \approx \frac{V_{THN} C_{OUT} \cdot 2\mu_p C_{OX} \frac{W_P}{L_P}}{g_{m,eff}^2} \quad (1)$$

T_{latch} can be calculate from another equation.

$$t_{latch} = \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{\Delta V_{out}}{\Delta V_0} = \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{V_{DD}/2}{\Delta V_0} \quad (2)$$

When combining these two equations, the total delay mainly depends on gm, V_{dd}, C_{out}, and the following equation can provide their relationship.

$$t_{delay} = \frac{V_{THN} C_{OUT} \cdot 2\mu_p C_{OX} \frac{W_1}{L_1}}{g_{m,eff}^2} + \frac{C_{OUT}}{g_{mp}^2} \cdot \ln \frac{V_{DD}/2}{\Delta V_0} \tag{3}$$

According to the equation provided, $g_{m,eff}$ is a parameter can be the crucial factor. Because unlike other parameters, $g_{m,eff}$ is inverse square to t0, it significantly impacts delay. Therefore, the most effective way to lower the delay is to increase $g_{m,eff}$. However, the following formula indicates that $g_{m,eff}$ is related to the width of M2 and M3.

$$g_{m,eff} = g_{mm} + g_{mp} = \mu_n C_{OX} \left(\frac{W}{L}\right)_n V_{dsn} + \mu_p C_{OX} \left(\frac{W}{L}\right)_p |V_{dsn}| \tag{4}$$

Because of the complex relationship between the width (M2 and M3)and power or delay, so figure 3. reveal the actual relationship and corresponding curve of delay and power vs. the width of M2 and M3. When the width is larger than 1 um, there is no momentous reduction in the delay. As for power, when the width is more extensive than 1um, power is approximately proportioned to width. So, the suitable width is roughly in the range of 1.0um to 1.5um. Therefore, the author and his team set it to 1 um is entirely reasonable.

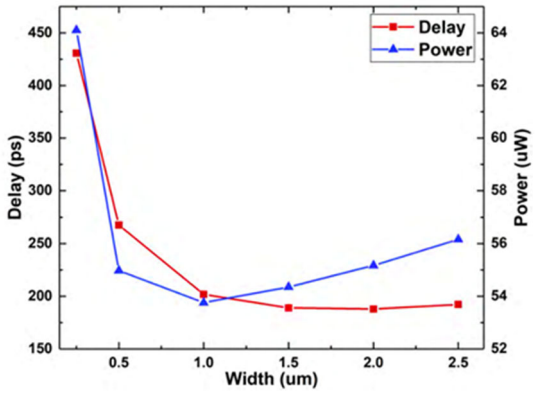

Figure 2. The correlation of width with delay & power.

The newly generated clock CLK1 is a modified and shifted signal from the original CLK; the time difference of these two signals is called t_{opm}. A more limited t_{opm} may prompt a larger short current through M6 and M7, while a more drawn-out t_{opm} may prompt a critical debasement of speed. From range 0-120, energy is approximately linear inverse to t_{opm}. But, the minimum delay can be find at around t_{opm} equal to 80ps. And the curve intersection is at 95 ps. Therefore, the writer selects the intersection point as the final value. It is acceptable, but if the requirement needs minimal delay and is less sensitive to energy consumption, t_{opm} 80ps is also a proper choice.

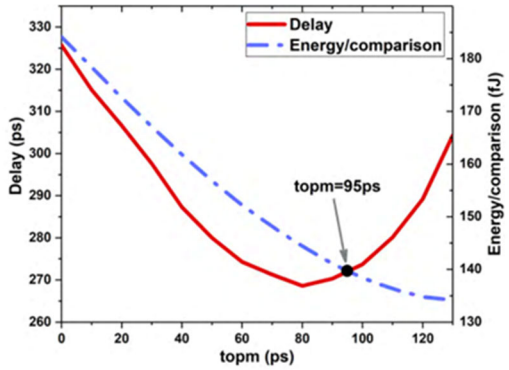

Figure 3. Simulation result of delay & energy vs. topm

The two graphs in figure 4 show the simulation delay and the energy/comparison when V_{id} = 50mV, V_{dd} = 1.2V. It indicates that the new structure comparator's delay performance is significantly better than competitive comparators. Furthermore, in most cases, energy consumption is also lower than the competitor, except V_{cm} equal to 0.6 volts ,which one comparator is lower than the proposed design.

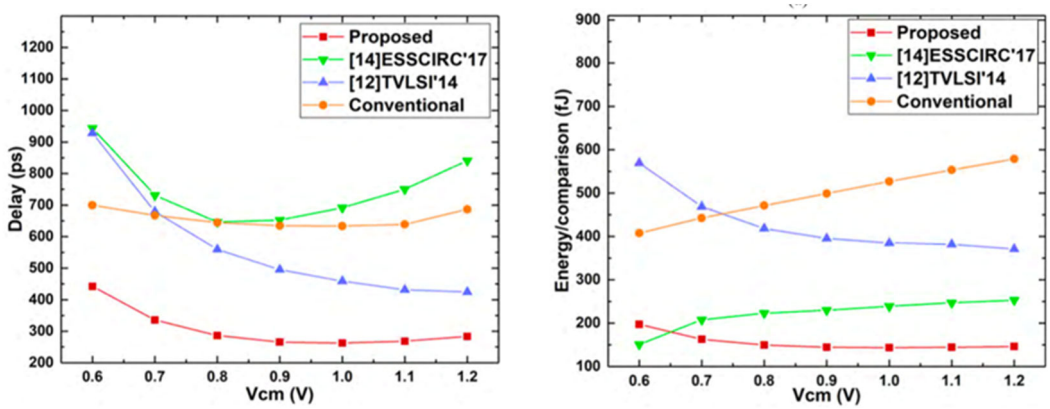

Figure 4. Simulation result of different comparatos' Vcm vs. delay & power.

Figure 5 shows that when tune the V_{id} = 50mV, V_{cm} = V_{dd}-0.1V, whether delay or power, the proposed comparator have better performance than other competitor.

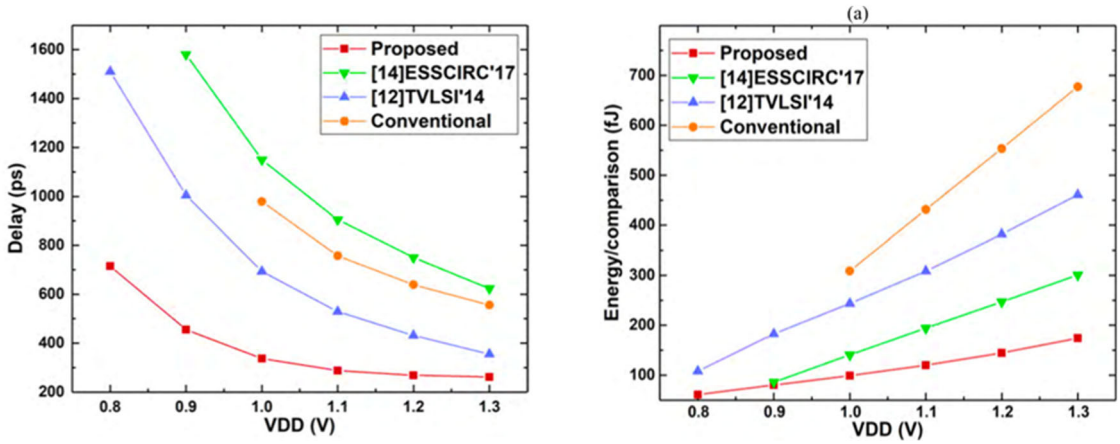

Figure 5. Simulation result of different comparatos' Vdd vs. delay & power.

The figure 6 below shows that simulated delay will decrease when V_{cm} increase from 0.6V-0.7V. The range from 0.7V to 1.1V, the delay shifts slightly. However, the delay remains moderate compared to rivals. As a result, the input voltage can be selected in the area from 0.8 to 1.2V.

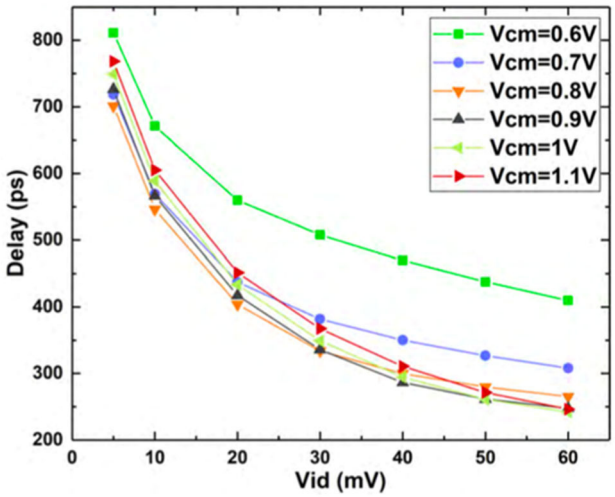

Figure 6. Vid vs. delay at different Vcm.

Figure 7 implies that the simulation result and actual measurement are approximately equally shifted. Both trends of measurement are similar to simulation. The delay's time shift may affect the oscilloscope or the measurement device's internal delay.

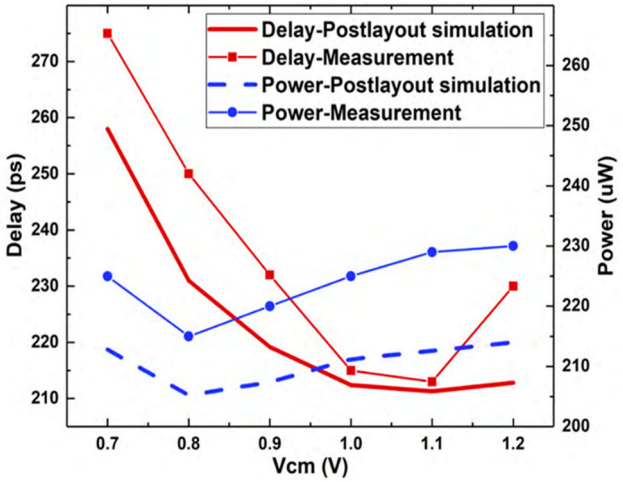

Figure 7. Vcm vs. delay & power.

2.2 Comparator With Dynamic Floating Inverter Amplifier.

The comparator with the new pre-amplifier stage and SA-latch was presented by Xiyuan Tang and his team in 2020. The proposed innovational structure is called a Floating Inverter Pre-amplifier.

$$\sigma_{n,\text{int}}^2 \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{TNH} C_X} \tag{5}$$

The equation, as mentioned earlier, can estimate thermal noise. In order to reduce the thermal noise, higher gm/Id and larger Cx are needed. The NMOS DB integration satisfied the two conditions above. DB integration adds a capacitor C_{tail} between Mb and ground in figure 8. The capacitor will isolate the ground and the NMOS connected to the CKLC. The capacitor can prevent leakage current, which can reduce extra energy consumption. This design improved the efficiency of the comparator.

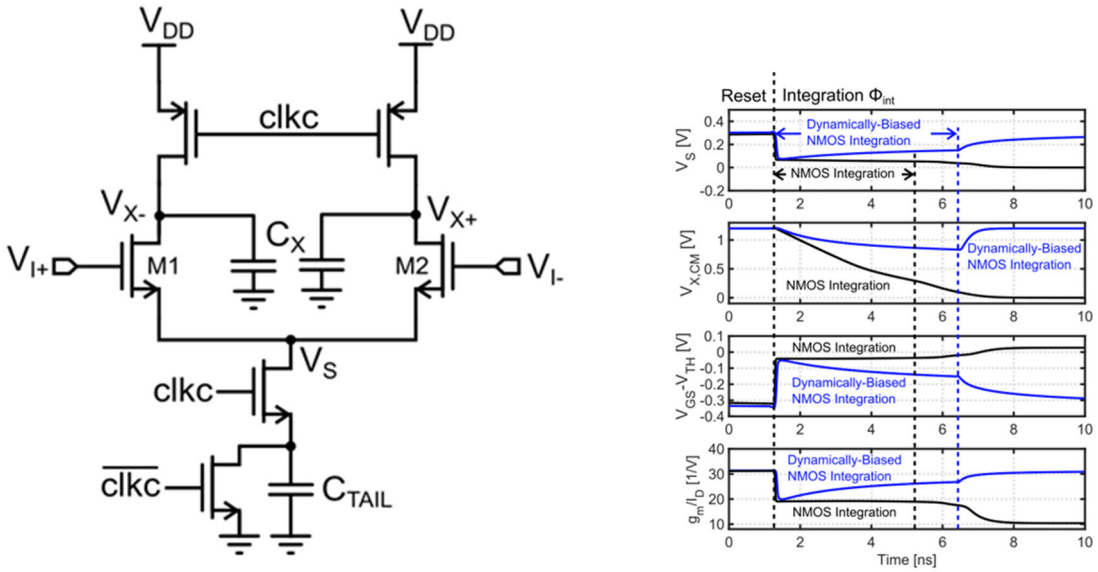

Figure 8. Comparator with Ctail and its behavior.

Because of the decent result, a new structure takes a step further. Adding more capacitors to save energy is reasonable. The CMOS DB integration is provided in figure 9. When the pre-amplifier is in the integration phase, the bottom node VS- value will increase, and Vs+ will decrease. However, the overdrive voltage got reduced. Thus, the capacitor hugely influences the stabilization of the output.

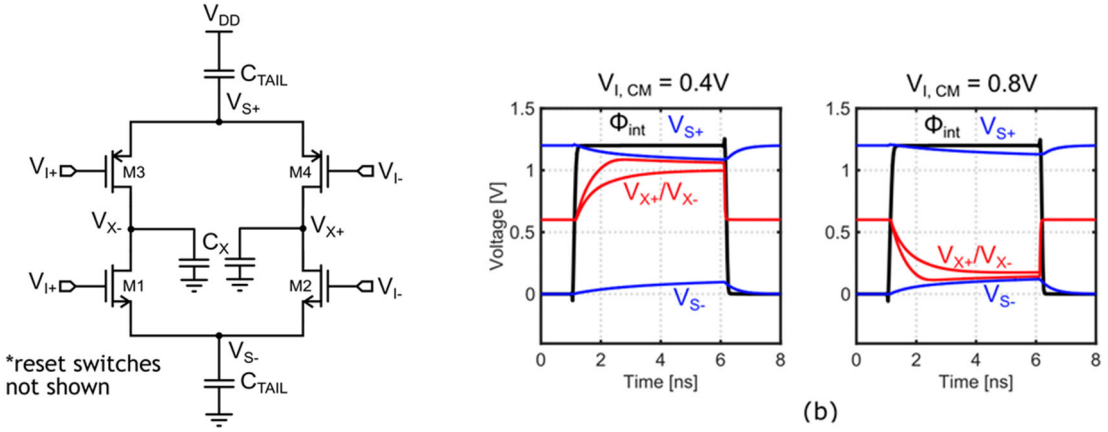

Figure 9. CMOS DB model and its input curve.

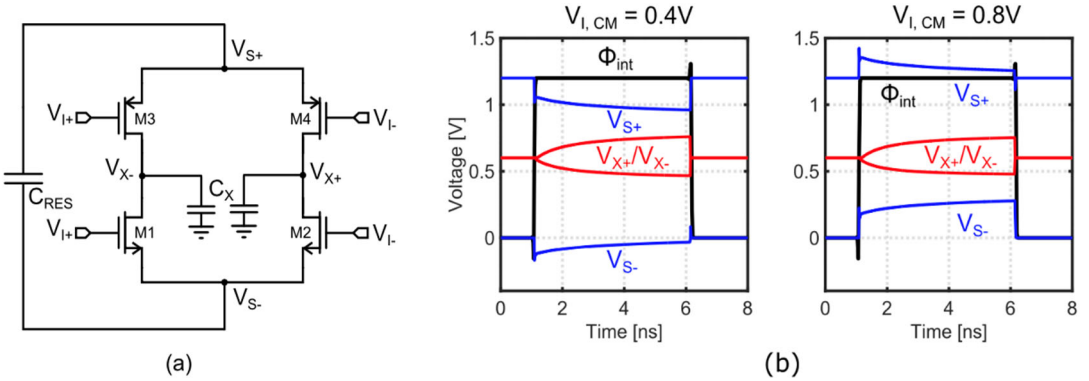

Figure 10. **FIA model and its input curve.**

The author reformed the structure. The proposed design is in figure 10 (a). Switching the two C_{tail} to one C_{res} capacitor provides an isolated voltage area. Furthermore, because the conservation of current flow through C_{res}, the common-mode current flowing into capacitor is down to 0. Therefore, the additional circuit is needless. Besides, the isolated area also provides, give flexibility for expansion.

$$\sigma_o^2(t) = \frac{1}{2}\int_0^t S_i(t-\tau)\cdot\left|h_n(\tau)\right|^2 d\tau \tag{6}$$

This formula can represent the noise of the pre-amplifier, including classic NMOS integration pre-amp-amplifier, DB integration pre-amplifier, and floating inverter pre-amplifier. The noise level is corresponded to the power spectral density(PSD) and magnitude of squared impulse response (h_{ntao}). The eventual formulas can be expressed as follow.

$$\sigma_{in,SA}^2(T_{INT}) = \frac{2nkT}{V_{TNK}\cdot C_X}\cdot\frac{I_D}{g_m} \tag{7}$$

$$\sigma_{in,DB}^2(T_{INT}) = \frac{2nkT}{C_P\Delta V_{X,CM}\cdot(T_{INT})}\cdot\frac{I_D}{g_m} \tag{8}$$

$$\sigma_{in,FIA}^2(T_{INT}) = \frac{2nkT}{C_{RES}\Delta V_S(T_{INT})}\cdot\frac{I_D}{G_m} \tag{9}$$

Due to the higher gm/Id and C_{res}, the FIA structure has taken the lead and has the relevant lower noise.

As for energy efficiency, the parameter can be approximately defined as figure of merit(FoM). FoM is shown by the equation 10.

$$FoM = Energy\cdot(Noise\ Power) \tag{10}$$

The corresponding FoMs are shown:

$$FoM_{SA} = \frac{4nkT\cdot V_{DD}^2}{V_{TNK}}\cdot\frac{I_D}{g_m} \tag{11}$$

$$FoM_{DB} = 4nkT\cdot V_{DD}\cdot\frac{I_D}{g_m} \tag{12}$$

$$FoM_{FIA} = 4nkT\cdot V_{DD}\cdot\frac{I_D}{g_m} \tag{13}$$

FoM for FIA compared to FoM for DB, as Gm is always larger than gm; what's more, Vdd is always larger than Vthn. Based on the theory analysis, FIA's FoM tends to be the smallest. The impact of C_{res} can be disregarded, which is indicated in figure 11.

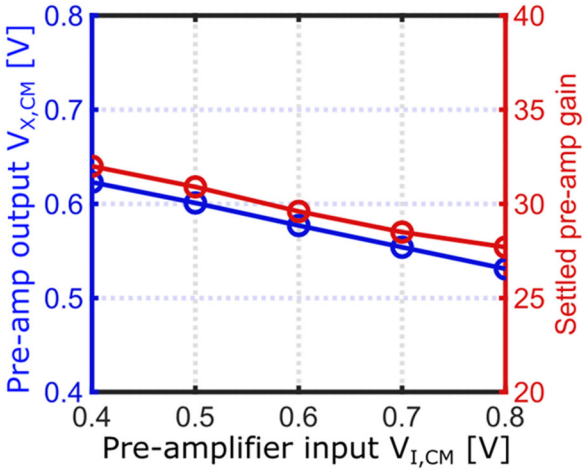

Figure 11. Simulation result of pre-amplifier voltage.

As for the vital specification delay, it is approximately inverse proportional to the C_{res}. The relationship between C_{res} and FoM is similar to the quadratic function. Thus, the balanced point for C_{res} is around 2.5 to 3 pF.

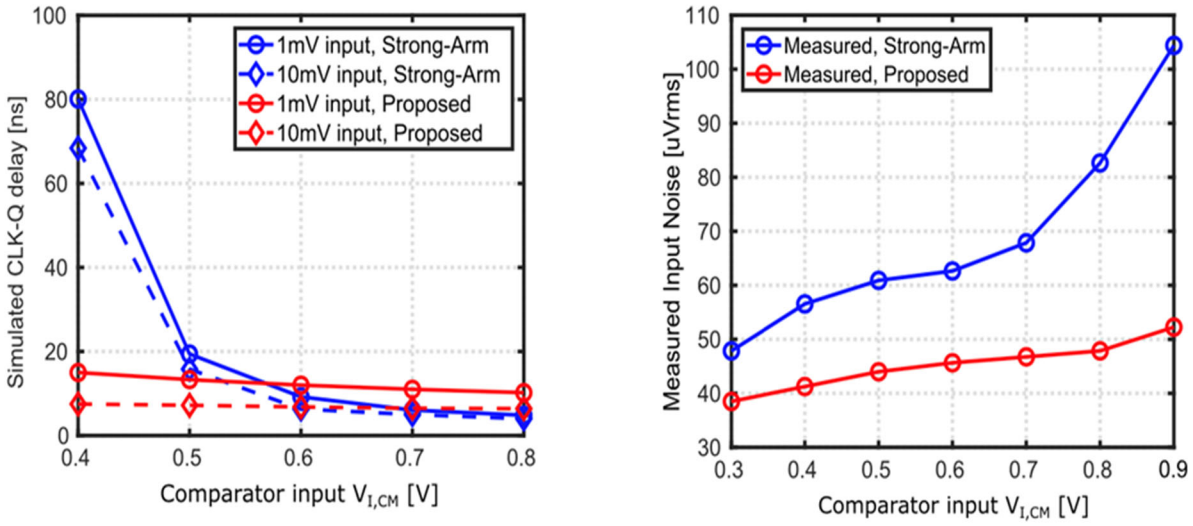

Figure 12. Noise & delay vs. Vi,cm.

The proposed comparator with FIA pre-amplifier has a vast delay advantage when Vicm is lower than 0.5V whether the input is 1mV or 10mV. However, when the comparator input voltage is higher than 0.6V, it is nearly the same compared to the SA structure. And the noise input is shown in figure 12. The new structure diminishes at least 10% and up to 60% input noise, which dramatically improves.

2.3 Triple-Latch Feedforward Dynamic Comparator.

Athanasios T. Ramkaj and his team present a three-stage dynamic comparator with an additional feed-forward path in 2019. The classic double-tail latch comparator and its improvement structure have some advantages in contrast with the classic SA structure. For example, it can sustain a larger current and maintain a low noise level. However, despite these advantages, it can not avoid a significant delay. So the author introduces the three-stage comparator with an extra feed-forward path.

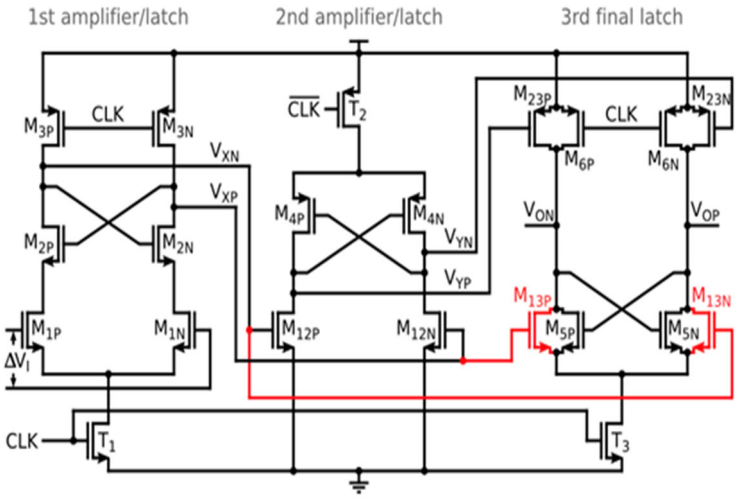

Figure 13. double-stage and triple stage comparators.

As mentioned above, the schematic of the comparator is demonstrate in figure 13. The first two latch serves as an amplifier and latch. The first pre-amplifier is to lower the noise and offset and attain high gain for the following two latches. The second pre-amplifier also reduces input noise like the first one but also works as isolation gain stage between input and output. The third stage works as a latch to reduce regeneration time. When CLK=0V, M3p, M23p, and M6p turn on, T1 and T3 turn off simultaneously. M12P/N and M23P/N play two roles, both gain and reset stages. When CLK = Vdd,

T1 to T3 turn on simultaneously, the direct path amplifies through M12P/N -M4P/N M23P/N chain, and the feed-forward path amplifies M13P/N. These two paths boost the voltage difference generated at the drains of the input pair.

$$\tau_{FF} \approx \begin{cases} \dfrac{\tau_2}{(1+g_{m12}/g_{m2})} + \dfrac{\tau_3}{(1+g_{m23}/g_{m5})} & small V_I \\ \dfrac{\tau_3}{(1+g_{m13}/g_{m5})} & large V_I \end{cases} \tag{14}$$

In the equation, gm parameters are the transconductances of the corresponding transistor. (For example, gm12 is the transconductance of M12P/N). T2 and t3 are the constants of stage 2 and 3. Therefore, tff is inverse proportional to the transconductance of the transistors, as mentioned earlier. Furthermore, when V1 is large up to a point, the delay can be estimated differently and simpler.

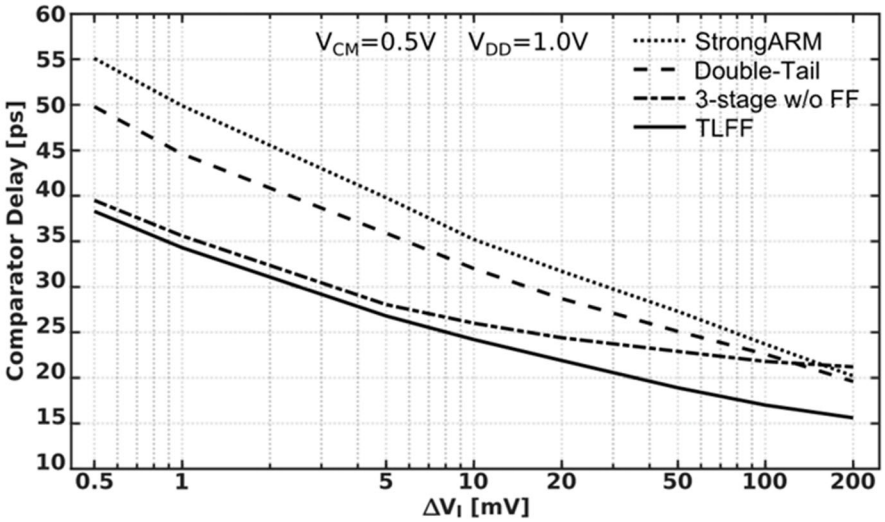

Figure 14. Delay vs. V1.

Figure 14 Shows the TLFF and other comparators with fixed V_{cm} = 0.5V and V_{dd} = 1V. TLFF is about 50% less delay than a competitor when V1 is 200mv. Furthermore, when V1 ranges from 0.5 to 100, the wait is 36% lower than StrongARM and 30% lower than 3-stage w/o FF.

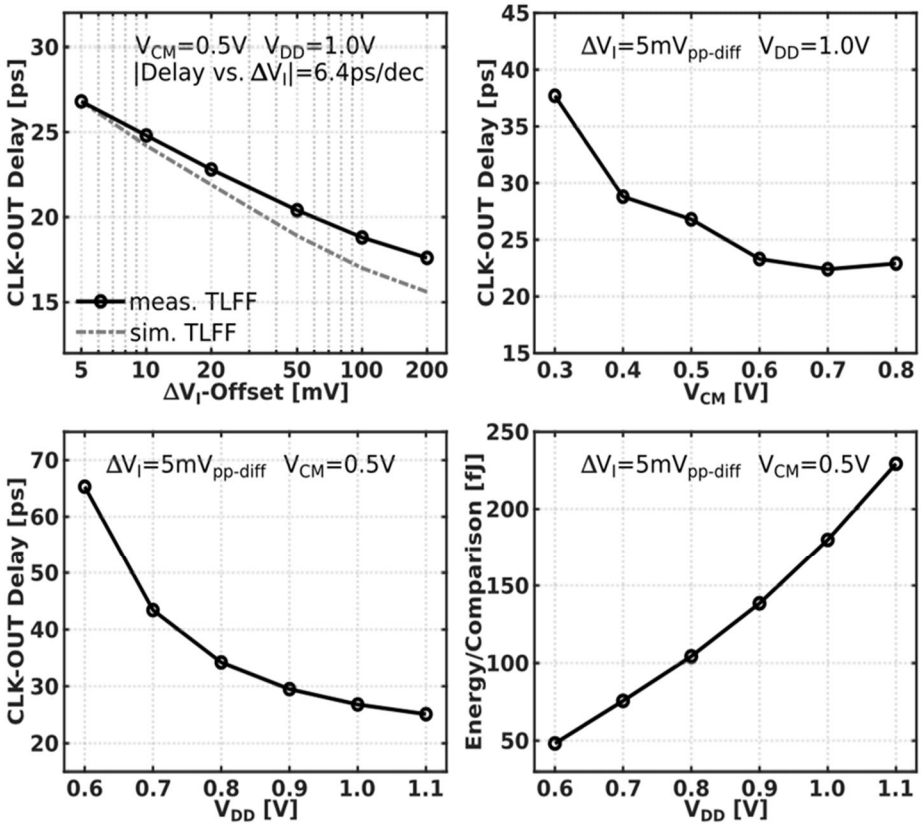

Figure 15. Delay & power vs. Vdd and Vcm

According to the measurements in figure 15 The measured CLK-OUT delay(top-left) is almost the same as the simulated result. The delay when V1=5mV is 26.8ps, and the slope of delay vs. V1 is 6.4ps/decade. V_{cm}'s delay drops about 40% when V_{cm} increase from 0.3 to 0.6. However, after 0.6, the variation is less significant, and the delay remains in a small range.

The two graphs about Vdd show that delay is inverse proportional to Vdd, and the power consumption is proportional to Vdd. The sweat point of Vdd is approximately 0.9V. Therefore, the author selected 1V as a trade-off for better delay performance is acceptable.

3. Conclusion

This paper mainly focuses on the design and advancement techniques for comparators, addressing the tight objective of speed, power, and responsiveness. These three design plans are robust and show extraordinary enhancements over earlier expressions. The first design introduced a comparator with an original transconductance-improved latching stage, which is reasonable for low-energy, high-speed activity. In addition, the cross-coupled transistors in the proposed latch structure are one-sided in the major area of strength for the district during the reset stage, which helps the total effective transconductance of the latch at the beginning of the comparison phase and diminishes the delay and power consumption. For the second design innovatively combined two capacitors into one, which helps maintain low power as CMOS DB, but is much more stable and makes less noise.

In most cases, delay is at least 25% lower than the competitor in all ranges. The third design presented An super-high speed, reasonable power, and fully dynamic multistage comparator. Adding a feed-forward route to the triple-tail comparator reduces the delay up to 50% depending on voltage. Eventually, the trade-off between energy consumption, delay, compensation, etc., remains the basic issue of comparators. Consequently, it is concluded that the trend in further research will systematically focus on improving performance and integration.

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