Analysis and comparison of several types of low-power, low offset comparators

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Abstract: This paper studies several excellent works of comparator constructions of comparators and compares them with the Double-tail latch-type comparator. Based on the Elzakker comparator, the comparator with a dynamic bias reduced the use of energy by partly discharging the preamplifier's output nodes. Edge-Pursuit Comparator(EPC) demonstrates a new approach to reducing energy consumption by automatic energy optimization. Apart from the designs that optimize energy consumption. Low-Noise Self-Calibrating Dynamic Comparator provides the low-offset feature while in relatively low power consumption.

Keywords: Dynamic bias comparator, Low-Noise Self-Calibrating Dynamic comparator, Edge-Pursuit Comparator, Energy optimization, Low-offset feature.

1. Introduction

Increasingly stringent demands on ADCs continue pushing the ADCs to break their limits. For most of the ADCs. Comparators consume nearly half of their energy consumption. Thus, low power consumption and low offset features are desirable. This paper studies three architectures of comparators focusing on low offset and low power consumption.

Dynamic bias comparators are proposed based on the Elzakker comparator. An Elzakker comparator can be get by slightly changing the topology of the conventional two-staged comparator [1]. Elzakker comparator separate pre-amplifier and regenerative latch to work asynchronously. This means delaying the conduction of the regenerative latch to get a more optimum energy solution. Based on this improvement. The dynamic bias comparator further optimizes the power consumption and input-referred noise.

Low-Noise Self-Calibrating Dynamic comparator minimizes the offset voltage through its unique self-calibrating technique. According to the value of the output and the fit of the two logic gates. The offset can be fed back to the comparator for adjustment [6].

Edge-Pursuit Comparator(EPC) has a new perspective to optimize energy consumption. Two oscillations with different propagation speeds were obtained through current-limiting transistors [8]. The output varies according to the voltage input to the limiting transistors. Energy consumption depends on the speed of the oscillation collapse. The larger the differential signal is, the faster the collapse occurs. Thus less energy is consumed. Thereby the automatic optimization of energy is achieved by this method.

The structure of the paper is as follows: The concepts of dynamic bias comparator, Low-Noise Self-Calibrating Dynamic comparator, and Edge-Pursuit Comparator(EPC) are revisited in Sections 2.1, 2.2, and 2.3, respectively. Section 3 carries out a parallel analysis and comparison of three comparators.

2. The basic fundamental of 3 comparators

2.1 Dynamic bias comparator

The strongARM latch was the initial batch of dynamic comparators to be extensively implemented throughout time. The comparator's robust feedback facilitates quick judgments. In addition, it offers full swing outputs and no static power usage. However, the strongARM latch comparator has a single-

stage design, which means the pre-amplifier and latch are not isolated. Therefore, this kind of comparator has severe kickback and needs a huge voltage headroom [1].

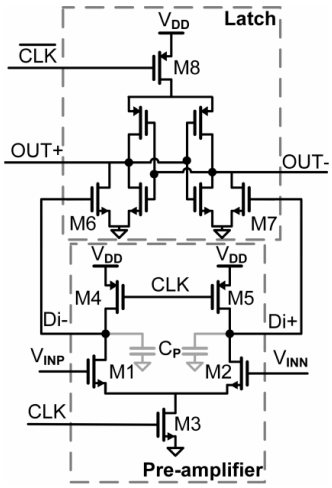
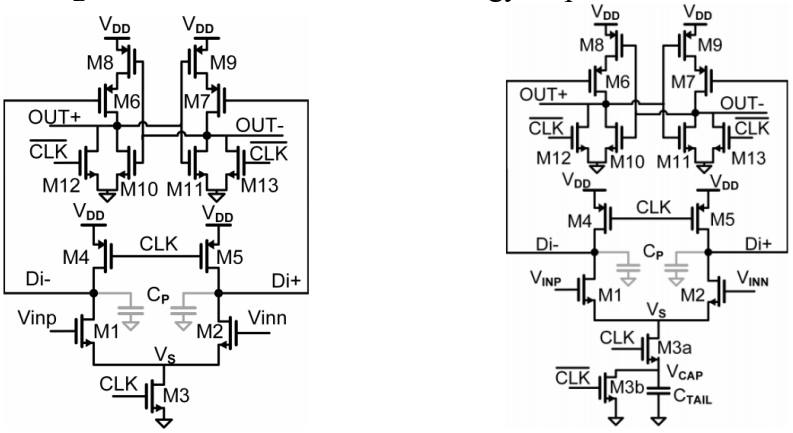


Figure 1. Double-tail latch-type comparator(Conventional 2-stage comparator)

As shown in Fig.1. By isolating the preamplifier from the regeneration latch, a double-tail latch comparator may alleviate the issues. It permits a larger input common mode range, resulting in functioning close to V_{DD}. In addition, it enables an independent tail transistor by offering an extra degree of freedom via the provision of distinct tail transistors [3]. This structure is well established and more widely used. Thus it is the conventional structure in this paper. However, its energy is not optimized to the best of its ability. At the end of the process, the preamplifier's output nodes are directly connected to the ground., which means fixed energy 2Cp.VDD is consumed per comparison.



(a) (b)

Figure 2. (a) Elzakker's comparator (b)Dynamic bias comparator

Elzakker's comparator is shown in Fig.2 (a). By delaying the latch stage's conduction until a significant voltage gain is built. Elzakker's comparator can be more energy efficient. The output of the pre-amplifier is fed to PMOS transistors–M6/M7, which are embedded in the latch stage instead of M8 in the Elzakker's comparator. And there is not a tail transistor in the latch stage of Elzakker's comparator. In Elazakker's comparator, M6/M7 are initially off. Only if the preamplifier's common-mode output voltage drops under the threshold voltage of these PMOS. The latch will start conducting [2].With this mechanism, when the latch starts to operate, sufficient differential voltage (gain) is built for regeneration operation. However, the pre-amplifier still accounts for around 80% of the comparator's overall energy consumption [2].

To optimize energy consumption even further. The comparator with Dynamic bias is created by applying the dynamic bias technique [4] to Elzakker's comparator. As it shown in Fig.2(b). Instead of M3 used in Figure 2(a), a tail capacitor and a (switch) tail transistor M3a are used. The reset

operation is achieved by M3b. The capacitor is used to regulate the discharge rate of Di+/Di- nodes. to provide a dynamic bias. When CLK equals zero, the transistors M4 and M5 pre-charge the Di+ and Di- to V_{DD}. The latch is reset by M12 and M13 and C_{TAIL} is connected to the ground. When $\mathrm{CLK} = V_{DD}$, every reset transistor is closed. M3a turns active, therefor, connecting the capacitances. Di+ and Di- initiate discharging. The tail current will flow to the tail capacitor to build a voltage resulting a reduced V_{GS} on differential pair(M1/M2). Consequently, the differential pair is provided with a dynamic bias during the comparison phase. Based on the magnitude of V_{INP} and V_{INN}. V_{GS} of M1 and M2 will reduce until it reaches the initial stage of quenching. V_s=min (V_{INP}-V_T,V_{INN}-V_T). Then one of differential pair turns off. Then the drain VDi+ and VDi- stop decreasing. The other transistor keeps discharging until it reaches the second quenching threshold, V_s=max (V_{INP}-V_T,V_{INN}-V_T) [4]. This is different from Elzakker's comparator which discharges the Di+ and Di- nodes completely to the ground. Thus, some energy is saved per comparison.

For the analysis of the performance of the comparators. The following relationships are given:

(1) The input-referred noise level of Elzakker comparator for the operation of strong inversion

(2) The input-referred noise level of suggested comparator for the operation of strong inversion

$$\mathrm{E}[\mathrm{v}^2{}_{\mathrm{n,SI,in}}(\mathrm{T_{INT}})] = \frac{4\mathrm{kT}\gamma}{\mathrm{C_P}.\Delta\mathrm{V_{Di,CM}}(\mathrm{T_{INT}}).(\frac{\mathrm{gm}}{\mathrm{I_{CM}}})_{\mathrm{SI,T_{INT}}}} \quad (1)$$

$$\mathrm{E}[\mathrm{v}^2{}_{\mathrm{n,WI,in}}(\mathrm{T_{INT}})] = \frac{2\mathrm{nkT}}{\mathrm{C_P}.\Delta\mathrm{V_{Di,CM}}(\mathrm{T_{INT}}).(\frac{\mathrm{gm}}{\mathrm{I_{CM}}})_{\mathrm{WI,T_{INT}}}} \quad (2)$$

As the $^{\mathrm{g_m}}/_{\mathrm{I_d}}$ ratio shown in Fig.3. The $^{\mathrm{g_m}}/_{\mathrm{I_d}}$ ratio of suggested comparator is obviously greater than Elzakker. Therefore, based on (1), the input-referred noise of the proposed comparator is smaller than Elzakker's comparator.

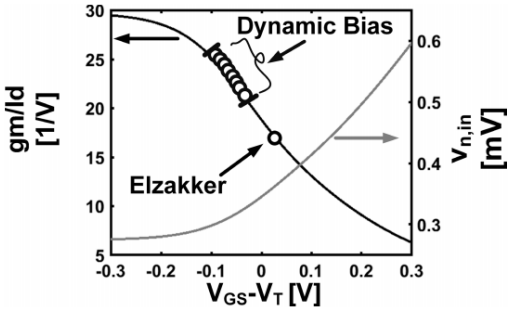
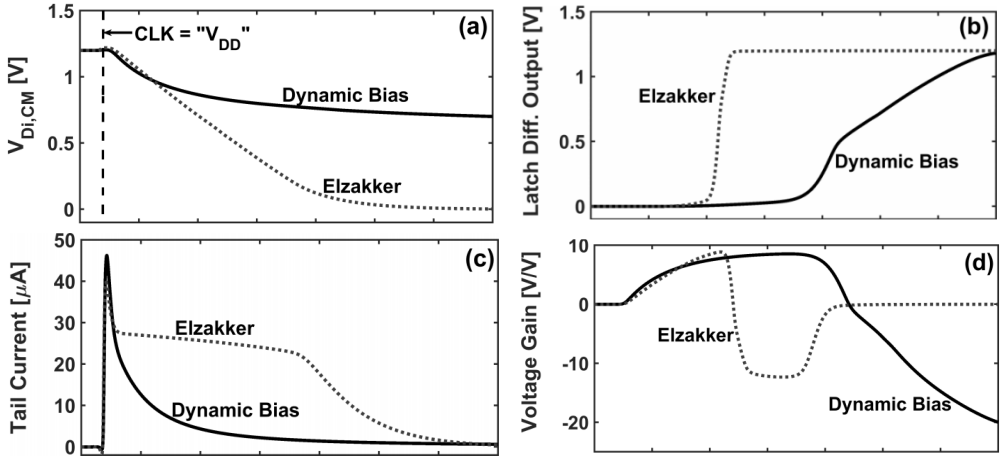


Figure 3. Estimated input-referred noise and $^{\mathrm{g_m}}/_{\mathrm{I_d}}$ ratio vs VGS–VT



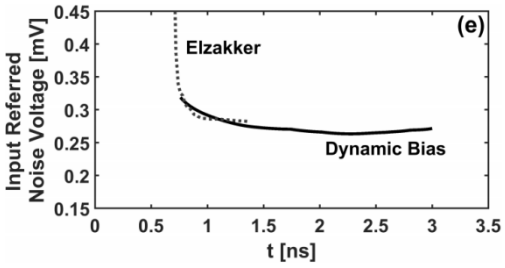


Figure 4. Some important parameters

Fig.4 (a) depicts the decrease in common mode voltage of both kinds of comparators. The Dynamic bias comparator will only discharge partially. Thus, the voltage will stop at a relatively high voltage.

The differential latch output of comparators mentioned above is seen in Fig.4(b). It is obvious that the comparator with dynamic bias suffers a time delay since PMOS transistors M6 and M7 perform at a low overdrive voltage.

Fig.4 (c) shows the tail current of the comparators. This indicates the power is mainly consumed in the first half stage of the operation, while the Elzakker consumes energy through the whole process.

Fig.4 (d) illustrate the voltage gain of the comparators. Due to the continually diminishing VGS, dynamic bias comparator goes deep in weak inversion and achieves maximum gm/Id ratio for most of comparison. Thus, the proposed structure's voltage gain decreased in the comparator's last half stage.

Fig.4 (e) demonstrates the input-referred noise of the comparators. Suggested comparator has better input referred noise condition.

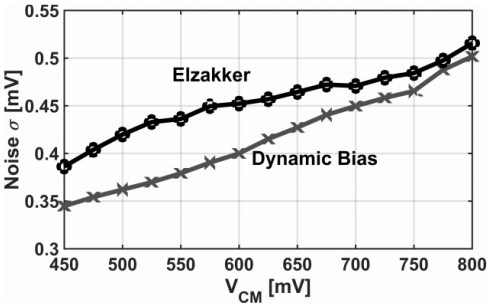
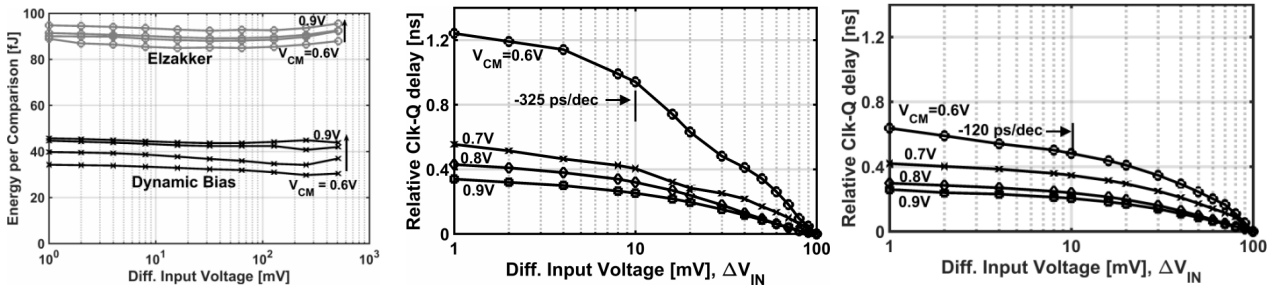


Figure 5. Measured input-referred noise versus V_{CM} for both comparators.

Fig.5 shows the input-referred noise for both comparators. It again demonstrates the superiority of the proposed comparator.



(a) (b) (c)

Figure 6. (a)Overall energy consumption (b)Relative Clk-Q delay of suggested comparator (c)Relative Clk-Q delay of Elzakker's comparator

Fig.6 (a), (b), and (c) depict the total energy consumption and relative Clk-Q delay of both comparators. It highlights the energy benefits of the suggested comparator. Under the condition of V_{CM}= 0.6V, the suggested comparator consumes 34 fJ/comparison while the Elzakker comparator consumes 88 fJ/comparison. This means about a 61% improvement in energy consumption. Energy optimization is similar to a common mode input of 0.6V-0.9V [4]. However, the Dynamic comparator has a disadvantage in terms of the relative Clk-Q delay, which is particularly noticeable when V_{CM}=

0.6V. However, by controlling the magnitude, the deterioration of the relative Clk-Q delay can be kept within an acceptable range.

2.2 Low-Noise Self-Calibrating Dynamic comparator

In addition to the high demands on power consumption, the low offset feature is also significant. However, most of today's comparators do not guarantee low offset with low power consumption and high speed. As shown in Fig.7. A self-calibrating technique is applied to the comparator to reduce the offset voltage.

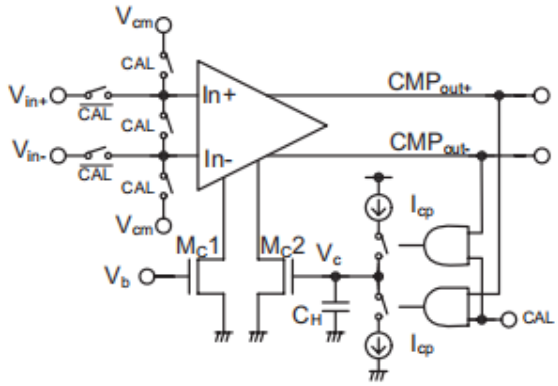


Figure 7. Basic structure of Low-Noise Self-Calibrating Dynamic comparator

Mc1 and Mc2 are linked to the comparator's internal output node create the compensating current. If there is an offset voltage on the output. Assume the offset to be positive, which means CMPout+>CMPout-. When CAL is high, the logic circuit drives the switch to control which current source is connected to the capacitor, thus controlling the potential of V_C. In the condition of offset voltage to be positive. The lower current source will be connected to the Ch, which means the potential of V_C will drop. In this way, C_H can keeps the offset value to eliminate the offset effect [4]. The circuit's behavior is shown in Fig.8. When there is no input. With the calibration of the surrounding circuit, V_C will continue to be close to V_{offset} and eventually fluctuate around V_{offset}.

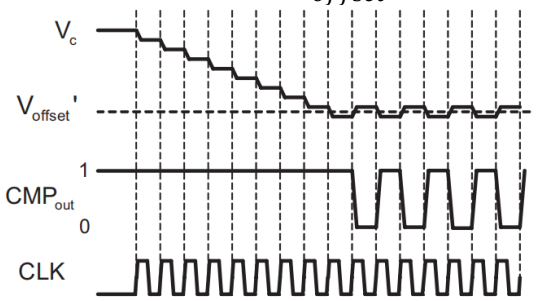


Figure 8. Behavior of the circuit

In order to apply the self-calibrating technique to the conventional comparator. The structure depicted in Fig.9 is suggested. It is comprised of a comparator based on a conventional two-stage structure [1] (shown in Fig.1), a current source used for compensation (MC1-2), and a charges pump. As seen by the signal behavior of the comparators in Fig.10. M3 and M4 pre-charge the Di to V_{DD} when CLK=0. Which allows the M8 and M9 output nodes to be discharged to GND. After the reset phase, the CLK signal becomes high. M3&M4 close and M5 activates. The potential of Di nodes will thereafter gradually decline.[5]

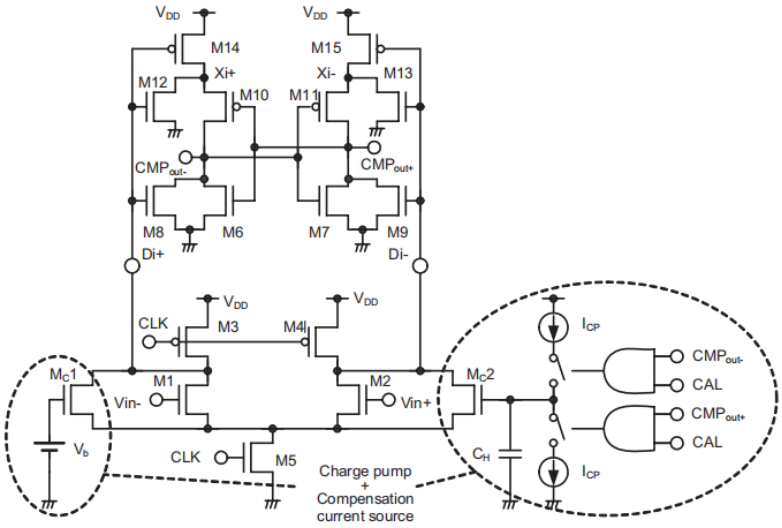


Figure 9. Proposed self-calibrating comparator

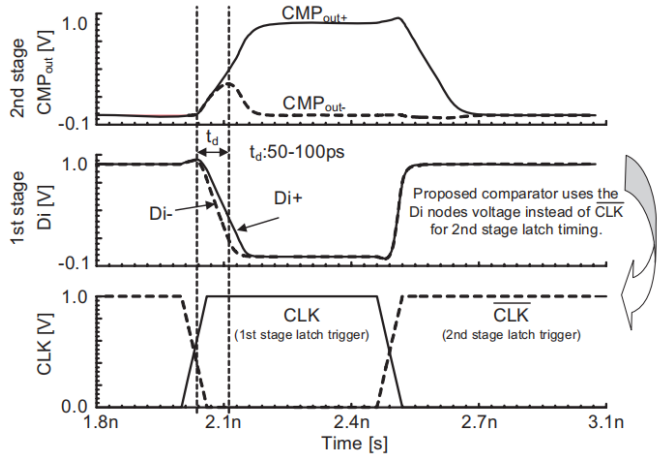
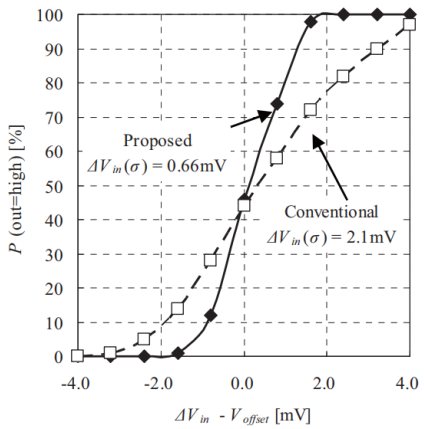
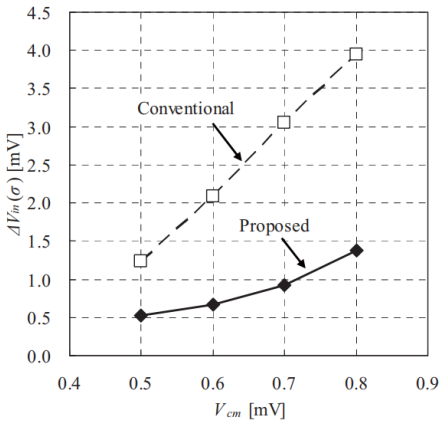


Figure 10. Signal characteristics of the conventional and suggested comparators.

As seen in Fig.10. A benefit of the suggested comparator is that the latch timing for the second stage is determined by the negative edge at Di nodes. Since the suggested comparator only requires a single-phase clock, the clock driving requirements are reduced. At the second latch stage, M14 and M15 serve as both input transistors and pre-charge switches. Thus, the gain of the second stage can be raised to improve the comparator's sensitivity.

To demonstrate the superiority of the given circuit. The same size transistors are used both in the proposed circuit and the conventional one. And the conditions of operation are the input common-mode voltage V_{CM} = 0.6 V, clock frequency f_{CLK} = 4 GHz and V_{DD} = 1.0 V.





(a) (b)

Figure 11. (a)Comparator noise acquired with Spectre transient noise simulation (b)Simulated equivalent input noise ΔVin(σ) vs V_{CM}

Fig.11(a) shows the results of the Spectre transient noise simulation on the comparator noise. The findings reveal that the proposed comparator has about three times less noise than the conventional two-stage comparator.

The simulated equivalent input noise ΔVin(σ) is seen in Fig. 11(b), and it was derived by plotting the cumulative noise distribution against the V_{CM}. In contrast to the conventional comparator, the suggested circuit's ΔVin(σ) only rises by 1.0 mV when V_{CM} is increased in given range (0.5V-0.8V). This is a better situation compared to the 2.8 mV rise that occurs in the conventional comparator [6].

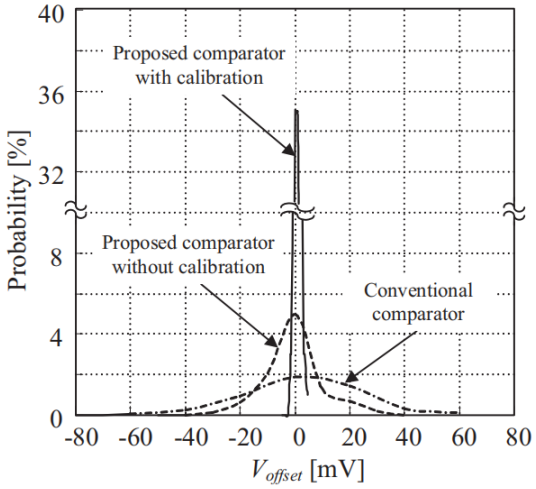


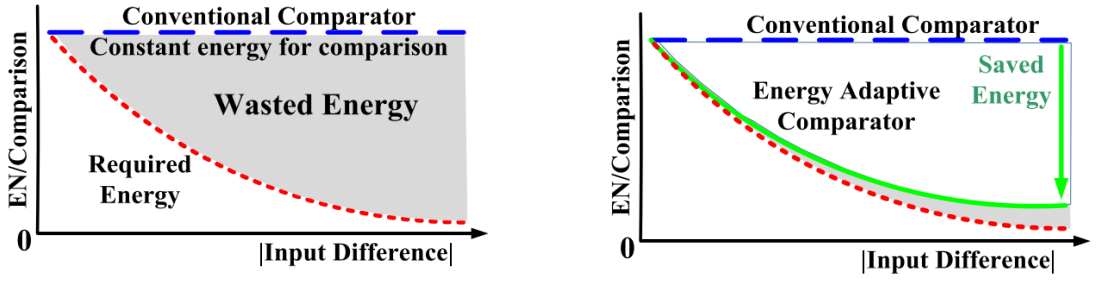
Figure 12. Simulated distribution of input offset voltage

As shown in Fig12. A simulation using 100 samples showed that the suggested comparator's offset distribution was 13.5 mV, while it was 21.5 mV for the conventional two-stage comparator when the self-calibrating technique was disabled. The method allows for an offset distribution optimization down to 1.3mV when the calibration technique is applied.

The technique is validated on a 0.0348 mm^2 chip area 90 nm 10M1P CMOS technology, which uses 64 comparators with SR latches to provide a steady output. The measurement results show a significantly improved offset voltage from 13.7mV to 1.69mV. This means 87% offset voltage optimization is achieved.

2.3 Edge-Pursuit Comparator(EPC)

As seen in Fig.13(a). For 2 stage-conventional comparators used nowadays can only consume constant energy. But actually, different amounts of energy are required depending on the differential inputs. For low differential inputs, more energy is needed. In contrast, less energy is needed. The wasted energy, in this case is significant. However, EPC can automatically optimize the power consumption according to the input difference. The saved energy is shown in Fig.13(b).



(a) (b)

Figure 13. Energy required for comparison against input difference

The basic structure of the EPC is demonstrated in Fig.14. The design consists of two NAND gates to initiate the oscillation and inverter delay cells. When the signal START goes high simultaneously. The comparator will initiate two propagating edges chasing each other. Until one overtakes the other, the oscillation will stop[7]. Then stage output COMP will settle to VDD or GND, which indicates the relationship between the magnitude of the two input signals.

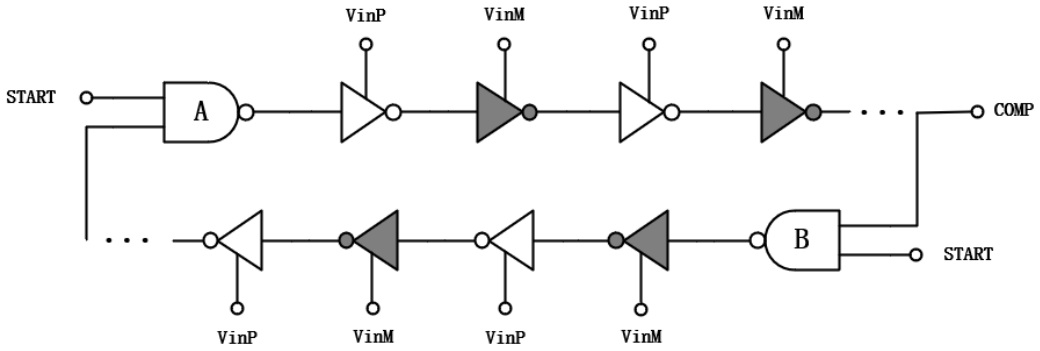


Figure 14. Gate level circuits of Edge-Pursuit comparator

In order to obtain different speeds of two propagating edges. Inverter delay cells are used. The CMOS static of a unite delay cell is illustrated in Fig.15. By applying different Vin to the current limiting transistors. Different pull-down/up times can be achieved. For example, if VinP>VinM. This means VinP is closer to logic 1 compared with VinM. At the same time, VinM is closer to logic 0 compared with VinP. Thus, as a result. The inverter connected to the VinP will have a shorter pull-down time than the pull-up time. The inverter connected to the VinM will have a shorter pull-up time than the pull-down time. By this, we can generate different propagation speeds for two propagating edges.

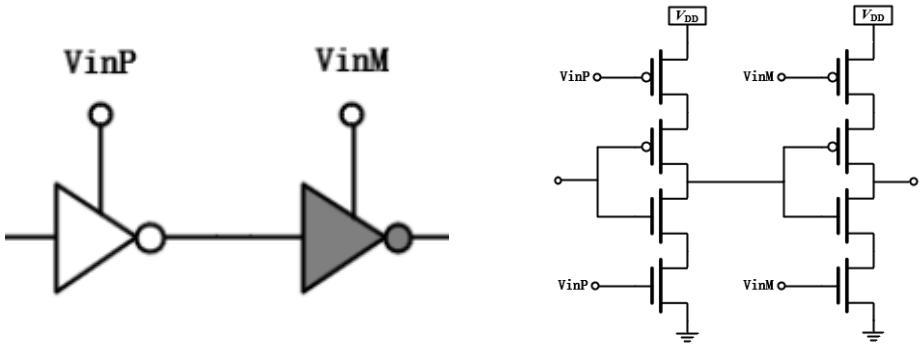
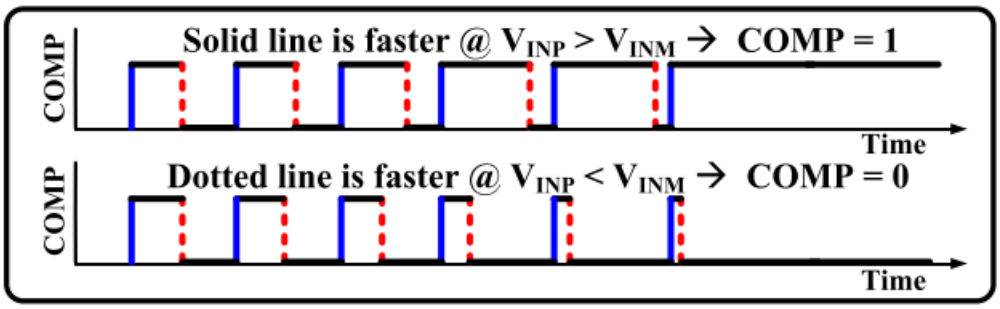
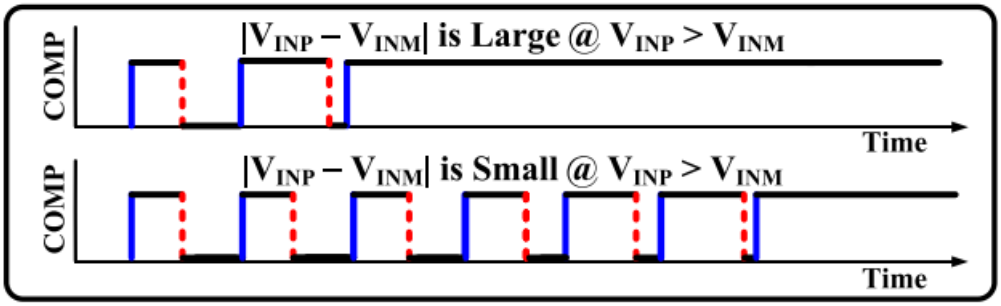


Figure 15. The CMOS static of an unite delay cell

Two simulation examples are shown in Fig.16 (a)&(b). COMP will be set to VDD if VinP>VinM. In contrast, the COMP will be set to 0. And as seen in Fig.16 (b). When the input difference is significant, the two edges collapse rapidly. While if the gap is small, the collapse will come slower, thus controlling energy consumption. That is because larger differences in input also produce more significant speed differences on propagating edges. Thus the oscillation will collapse faster.



(a)



(b)

Figure 16. The output of the EPC versus time during operation

In order to simplified the analysis, the following parameters and equations are given：

(3) Drift coefficient of the random process-M.
(4) Diffusion coefficient of the random process-Σ
(5) M/Σ ratio
(6) Scaling factor-S(k)
(7) The input-referred noise
(8) The average energy consumption per comparator

$$M \equiv \frac{\mu\Delta\varphi}{\tau} = 4\pi f_0 \frac{V_{in}}{V_{OV}} \tag{3}$$

$$\Sigma \equiv \frac{\sigma^2\Delta\varphi}{\tau} = 8\pi^2 {f_0}^2 \frac{kT}{I}\left(\frac{2}{V_{OV}}(\gamma_N + \gamma_P) + \frac{2}{V_{DD}}\right) \tag{4}$$

$$\frac{M}{\Sigma} = \frac{1}{\sqrt{12}} \frac{v_{in}}{\sigma_{v_n}} \tag{5}$$

$$S(k) \equiv \frac{\tanh(k\pi)}{k\pi} \tag{6}$$

$${\sigma_{v_n}}^2 = \int_{-\infty}^{\infty} {v_n}^2 f_{v_n}(v_n) dv_n = \int_{-\infty}^{\infty} {v_n}^2 h'(v_n) dv_n = \frac{\pi^2}{3} {f_0}^2 \left(\frac{kT}{I}\right)^2 \left(\frac{2}{V_{OV}}(\gamma_N + \gamma_P) + \frac{2}{V_{DD}}\right)^2 {V_{OV}}^2 \tag{7}$$

$$E = P \times E[T] = 2I.V_{DD}.\frac{\pi^2}{\Sigma}.S\left(\frac{M}{\Sigma}\right) \tag{8}$$

According to (7), the input-referred noise level increases as f_0/I increases and decreases as x squared, inversely proportional to the capacitance. Consequently, the input-referred noise may be modified by adjusting the size of each inverter cell or the number of delay cells in the comparator. Fig.17 depicts the simulation results of the two approaches.

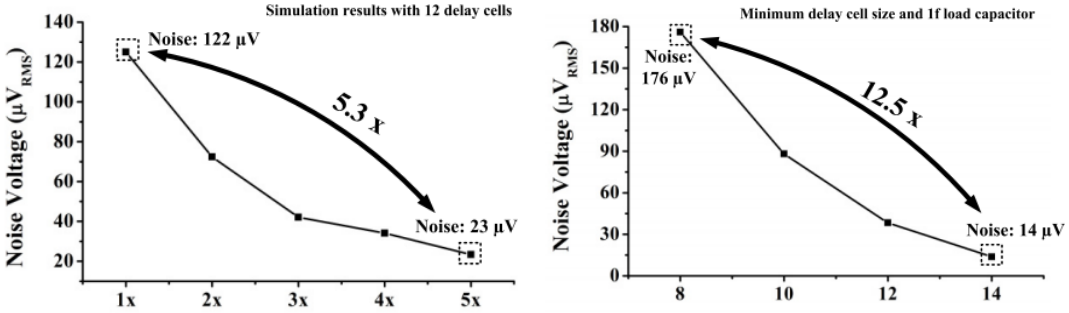


Figure 16. Two methods for noise voltage adjustment

The noise changes more sensitively when the amount of delay cells increased. It is due to the phase difference shift's positive feedback. By increasing the number of stages from 8 to 14, this positive feedback mechanism increases the level of noise that may be optimized by a factor of 12.5 [8].

As shown in Fig.18, The scaling factor S(k) will keep around 1 when the differential input is inside the noisy region. Still, if the difference input travels outside the noisy zone, it rapidly goes toward zero. By which automatic energy scaling can be achieved. According to (5) and (6), Energy scaling factor S (M/Σ) can be derived. According to (5), M/Σ ratio is inversely proportional to s_{vn}. And s_{vn} is inversely proportional to overall capacitance, then M/Σ ratio is positively correlated to overall capacitance. Thus, overall capacitance can be used to modulate the EPC's energy scaling factor.

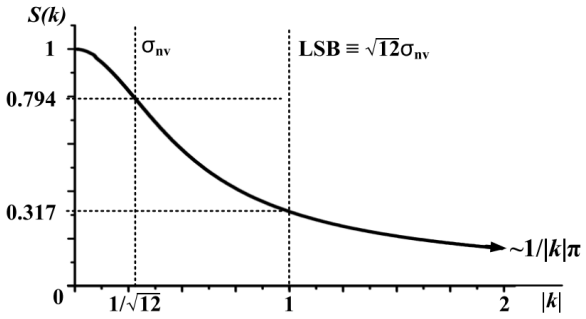


Figure 18. EPC's scaling factor

The number of delay cells affects not only the value of input-referred noise but also the size of the input-referred offset, according to the simulation in [9]. The input-referred offset versus is given in Fig.19.And the equation is given as $V_{OS\_N} = \frac{1}{\sqrt{N}} . V_{OS}$.

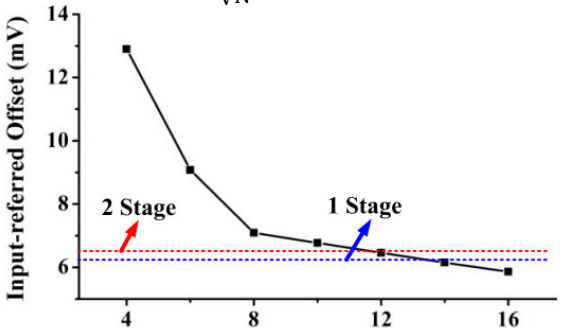


Figure 19. Input-referred offset voltage against the number of delay cells

For the purposes of indicating the energy efficiency of comparators. $N \equiv E \times \frac{{\sigma_{vn}}^2}{{V_{DD}}^2}$ is defined.

Thus, for different comparators, the value of N can be deduced:

(9) N value for conventional two-stage comparator (Shown in Fig.1)

(10) N value for EPC (Shown in Fig.14)

(11) The ratio of the norms

$$N_{TS} = E_{Ts} \times \frac{\sigma_{vn}{}^2}{\mathrm{V_{DD}}^2} = 4\mathrm{kT}\gamma\frac{\mathrm{V_{OV}}}{\mathrm{V_{th}}} \tag{9}$$

$$N_{EPC} \cong \frac{\pi^2}{3} S(\frac{M}{\Sigma}) kT\gamma \frac{\mathrm{V_{OV}}}{\mathrm{V_{DD}}} \tag{10}$$

$$\mathrm{N_{EPC}}: \mathrm{N_{TS}} = \mathrm{S}(\frac{\mathrm{A}}{\mathrm{B}}) \frac{\pi^2/_3}{\mathrm{V_{DD}}} : \frac{7}{\mathrm{V_{th}}} \tag{11}$$

Since N represents Energy efficiency, according to equation (11), the EPC has norms that are lower than those of the conventional two-stage comparator. In other words. EPC has superior energy efficiency.

EPC is finally verified on a 15 bits high-resolution synchronous SAR ADC [8], [10]. The transient noise simulation result is given in Fig.20 under the condition of 0, 0.5, and 1 LSB input voltage difference. When the difference of input voltage reaches 1 LSB, the comparison time required is minimal. When the difference is 0LSB, the comparison time is the longest. That corresponds exactly to what is shown in Fig.16(b). Thus, the automatic energy scaling function is verified. EPC can save an amount of energy when significant input voltage differences occur.

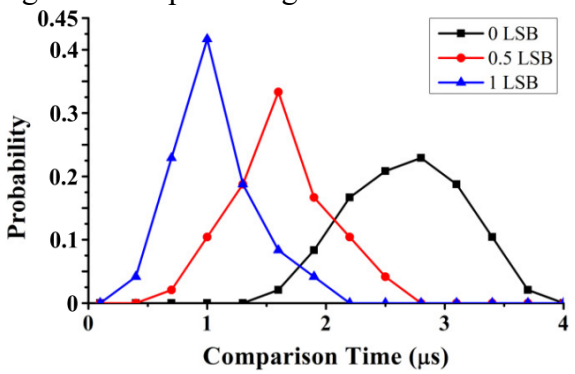
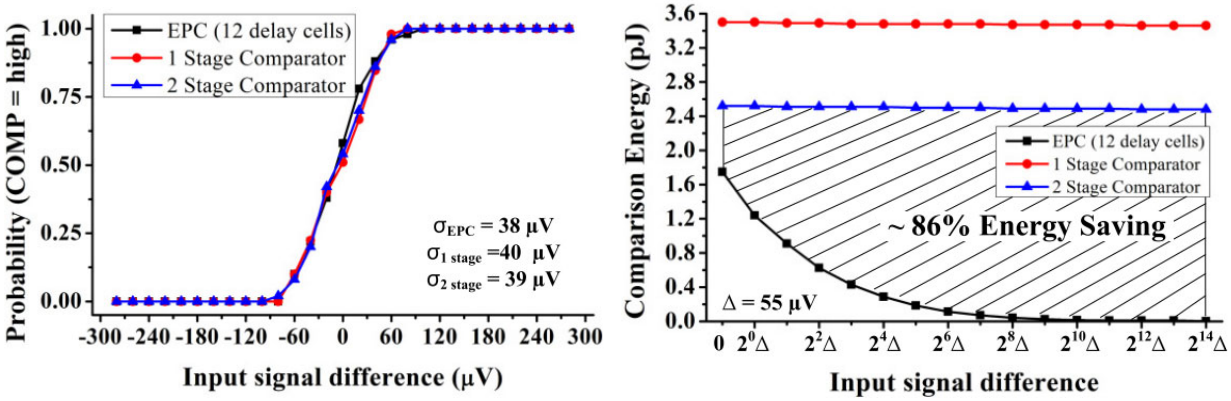


Figure 20. The simulated probability distribution of comparison time

As shown in Fig.21 (a) and (b). The performance of the EPC is very similar to the conventional 2-stage comparator. However, EPC saves approximately 86% of overall energy consumption. And have a more minor input referred noise (Under the condition of 12 delay cells).



(a) (b)

Figure 21. (a)Performance comparisons of the comparators mentioned in section 2.3 (b)Overall energy consumption of the comparators

3. Parallel comparison

The improvement and deterioration of these comparators are labeled in table 1. The Dynamic bias comparator modified the conventional circuit structure to reduce input-referred noise and power consumption at the expense of the operation speed. The Low-Noise Self-Calibrating Dynamic comparator gets the feature of low offset. However, a larger area is required for the self-calibrating circuit. Edge-Pursuit Comparator (EPC). The comparator can automatically adjust the energy consumption according to the input difference by using automatic energy scaling. But at the same time, it may take longer for small input differences.

Table.1. Comparison of different comparators

Technique	Dynamic bias	Self-Calibrating	EPC
Improvement	Reduced input-referred noise&power consumption	Reduced offset voltage	Reduced power consumption
Optimisation rate Compared with conventional two-stage comparator in the same process	61% improvement on power consumption	87% improvement on offset voltage	86% improvement on power consumption
Deterioration	Longer time delay	Larger area	Longer time delay for small input difference

In general, the EPC is the most optimized. However, it breaks completely with traditional design concepts, and its design may be more laborious. The other two comparators make good improvements in energy consumption and offset voltage, respectively. And they are based on the conventional two-stage comparator. The design requirements are not as high as for the EPC. The speed of comparison deteriorates in the EPC and the Dynamic bias comparator, respectively. The speed deterioration of the comparator with dynamic bias is slight and can be ignored with the appropriate choice of common mode input. However, the speed deterioration of the EPC cannot be avoided at low input differentials, which is part of its operating mechanism (Automatic energy scaling). Therefore, when using the EPC as the comparator, particular attention should be paid to the use context, especially when low input differentials and high-speed comparisons are required.

4. Conclusions

This article summarizes 3 comparators focusing on energy optimization and offset voltage elimination. A dynamic bias comparator allows partially discharging the pre-amplifier output nodes. Then reduce the current directly to the ground to save energy. Low-Noise Self-Calibrating Dynamic comparator shows a structure based on the conventional two-stage comparator that significantly eliminates the offset voltage. An Edge-Pursuit comparator (EPC) proposes a novel approach to energy optimization by generating two edges with different propagation speeds.

Future research into comparators could continue to be optimized on the performance of the EPC. For example, reducing the delay generated by the EPC in the case of low input differences.

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