Performance analysis of comparators

Chengyun Tang*

School of Electronic Science and Engineering University of Electronic Science and Technology of China Chengdu, China

*Corresponding author email: 2019340103003@std.uestc.edu.cn

Abstract. This article reviews the innovative and improved structure of three comparators, and summarizes the optimization ideas to further optimize the design parameters of the comparators in the future. The Triple-Tail Dynamic Comparator proposes a multi-stage design to break connection between speed and noise. The Dynamic Bias Latch-Type (DB) Comparator takes an innovative approach to reducing energy consumption by stabilizing the source node voltage of the input pairs. The floating inverter amplifier (FIA)-based pre-amplifier further improves the energy efficiency based on the design of the low-power comparator, and also optimizes parameters such as common-mode output voltage and noise.

Keywords: Triple-Tail Dynamic Comparator proposes, Dynamic Bias Latch-Type (DB), Floating inverter amplifier.

1. Introduction

Comparator is a critical component used in ADCs and Relaxation Oscillators that compares two current or voltage inputs at inverting and non-inverting node respectively and gives out the result in digital form [1]. The bounded thermal noise requirement makes comparator become a major power contributor. In addition to power efficiency, another key requirement of a comparator is that the comparator is insensitive to changes in the input common mode. The input common-mode voltage influences the comparator's noise, speed, and offset, which reduces the system's conversion resolution and accuracy [2].

This paper analyzes and discusses key parameters such as power consumption, speed, noise, and offset through three papers. The Triple-Tail Dynamic Comparator breaks the relationship of mutual influence between parameters, so that each level can optimize specific parameters independently. Triple-Tail Dynamic Comparator optimizes the speed based on double-tail latch type comparator and has little effect on noise. But the proposed comparator consumes over 30% higher energy than the SA latch.

The DB Comparator reduces energy by reducing static operating point fluctuations. The DB comparator increases power by 2.5 times compared to the strong-ARM latch by not fully discharging the pre-amplifier output nodes. However, the longer integration time in the weak inversion region brings a higher CLK-Q delay.

The FIA-based pre-amplifier is further improved on the basis of DB Comparator. The proposed design combines two tail comparators into a floating reservoir and solves the problem of lacking common-mode feedback (CMFB) which makes the design simpler. Also, The FIA-based pre-amplifier improves the speed problem by stabilizing the output common-mode voltage.

The rest of this paper is structured as follows. Section II revisits the Triple-Tail Dynamic Comparator. The circuit structure and innovation of the Dynamic Bias Latch-Type Comparator are introduced in Section III. Section IV elaborates the advantages of the FIA-based pre-amplifier and the effects of parasitic capacitance, and Section V concludes the paper.

2. Triple-Tail Comparator [4]

The article expounds the importance of comparators for high-speed ADCs. The noise, kickback, and common-mode sensitivity of comparators will have a great impact on the overall accuracy of the circuit [3]. So when considering a comparator, these parameters should be weighed at the same time.

However, due to the adverse effect between the noise and speed of the comparator, the trade-off between these two important performance parameters requires our special attention [4].

Therefore, a three-level circuit is designed, which breaks the relationship of mutual influence between parameters, so that each level can optimize specific parameters independently, as shown in Figure 1.

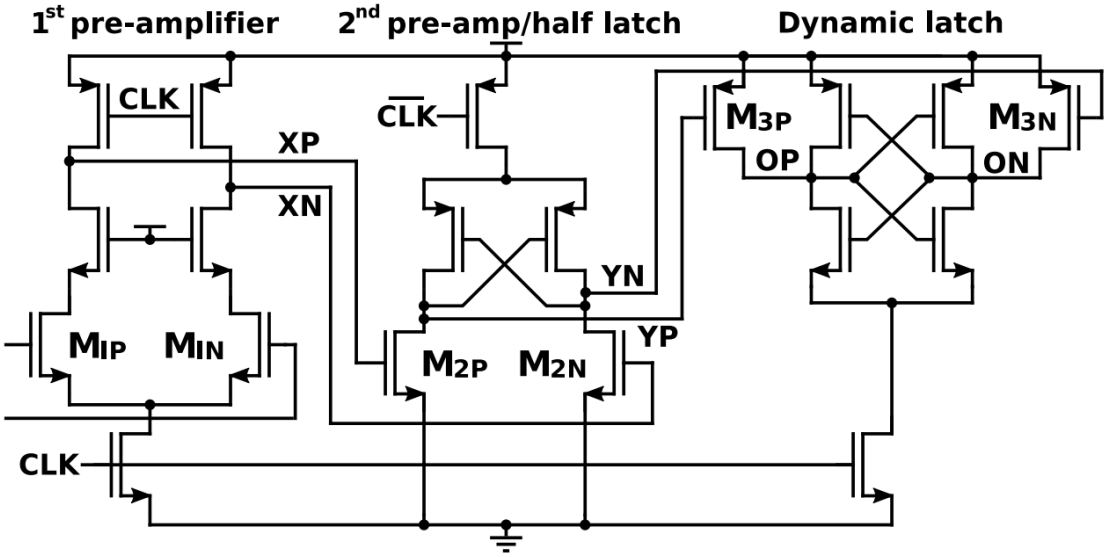
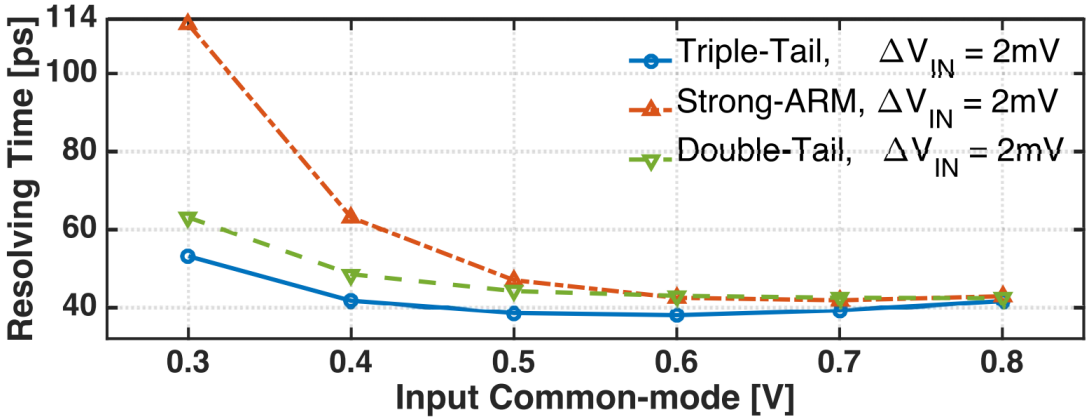


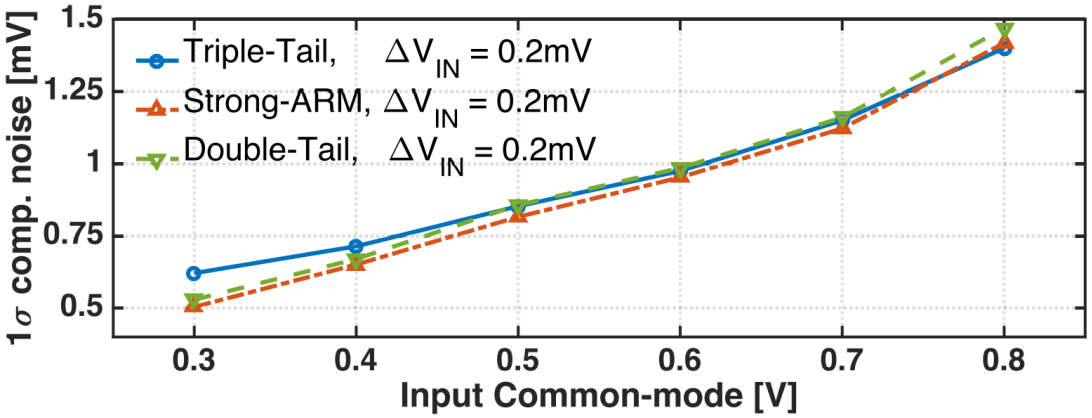
Figure 1. Figure of Triple-tail comparator.

The first stage pre-amplifier provides a high gain, which reduces input-referred noise. Different from the first stage, the second stage preamplifier provides further signal gain through cross-coupling, which minimizes its regeneration time, in addition to that, the second stage suppresses output noise. The final stage isolates both the input and output sources from each other.

The input common-mode voltage has some influence on the comparator's speed and noise. A higher $V_{CM,IN}$ increases the current through the input pair, which brings a faster speed, as shown in Figure 2 (a). However, this leads to an increasing noise integration bandwidth which means an increasing noise, as shown in Figure 2 (b). So it is important to achieve the optimal value between speed and noise.



(a)

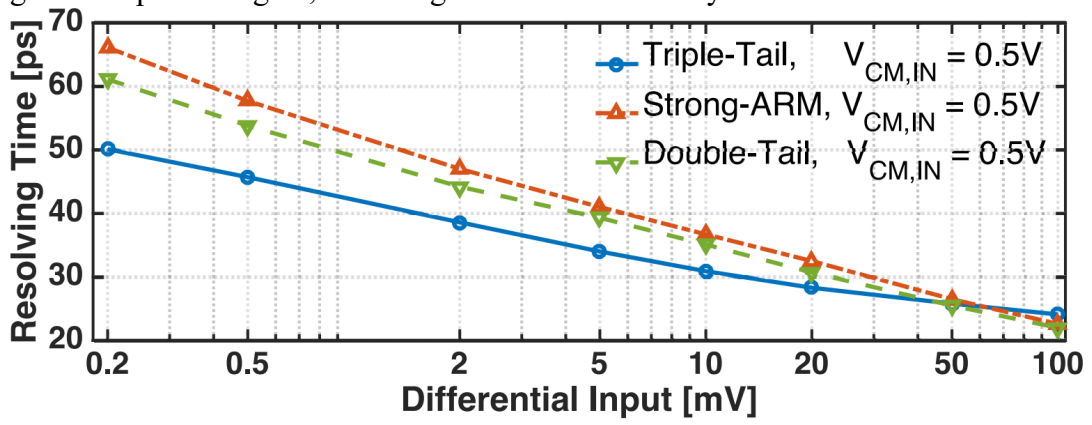


(b)

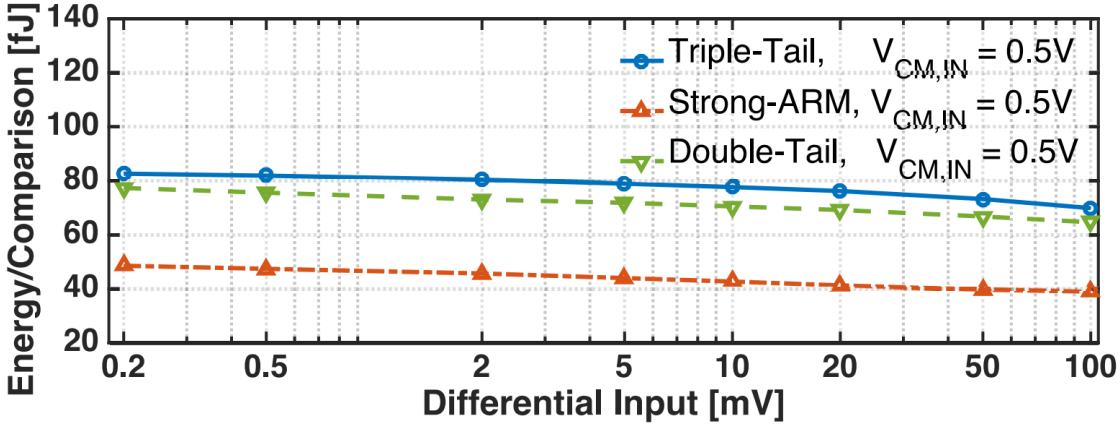
Figure 2. (a) Simulated resolving time of Triple-tail comparator and (b) input-referred noise versus $V_{CM,IN}$.

When the common mode input voltage gradually increases, the resolution time of the three designs decreases, but the performance of the triple tail design always keeps the best. When $V_{I,CM}$ is low, the Triple-tail's noise value is a little amount higher than the noise values of the other two. Also, as the common-mode input voltage gradually increases, the gap becomes smaller and smaller, and even after the common-mode input voltage is greater than 0.5V, it begins to be smaller than the double tail design. Therefore, in practical applications, choosing a common-mode input voltage of 0.5V not only takes into account the speed, but also keeps the input-referred noise small enough.

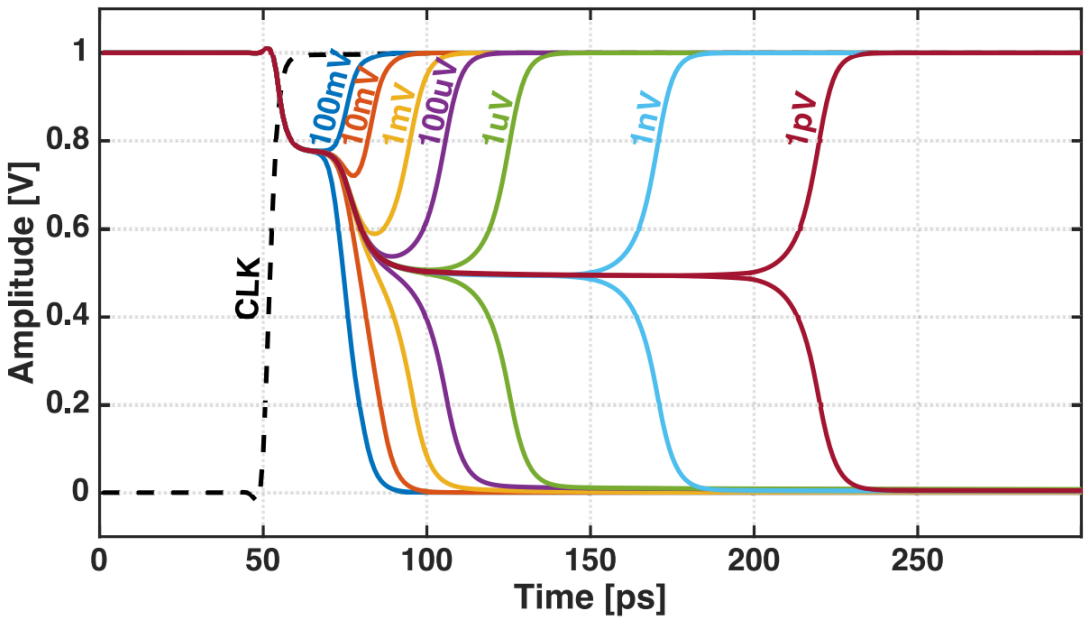
The differential input signal means a lot to the design of the system, as shown in Figure 3. When the differential input signal is small, a large resolving time occurs. This can put the system into a metastable state and cause accuracy degradation. Both issues can be resolved by lengthening the loop or raising the comparator's gain, but doing so would slow the system down.



(a)



(b)



(c)

Figure 3. Simulated comparator (a) resolving time, (b) energy/comparison versus differential and (c) relationship between V_{ID} and amplitude of Triple-tail comparator.

To keep the ADC working at high speed, a larger differential input signal should be chosen. When the differential input signal is less than 50mV, the energy of the Triple-tail is approximately identical to that of the double tail, somewhat higher than that of the SA latch, and the resolution time of both designs is lower than that of the SA latch. Since the speed of the comparator is important to the sampling rate of the ADC, it is a better choice to trade slightly larger energy consumption for faster speed.

3. Dynamic Bias Latch-Type Comparator [6]

Although Triple-Tail Dynamic Comparator increases speed without compromising noise performance, it brings energy penalty. A dynamically biased latch-type comparator is designed to optimize power consumption. Since the comparator requires a large voltage headroom and a smaller kickback, the [6] designs the circuit based on the Elzakker comparator, as shown in Figure 4. Since the employed DB comparator is over 2 times more energy-efficient than the Elzakker comparator, it is perfect for low power applications.

The capacitance of the output node of the Elzakker comparator is completely discharged to the ground at the end of the comparison, which limits further optimization of the comparator's power consumption. The [6] replaces the tail transistor of the Elzakker comparator with a capacitor and a transistor, as shown in Figure 5, so that the output point is partially discharged, thus realizing the function of energy saving.

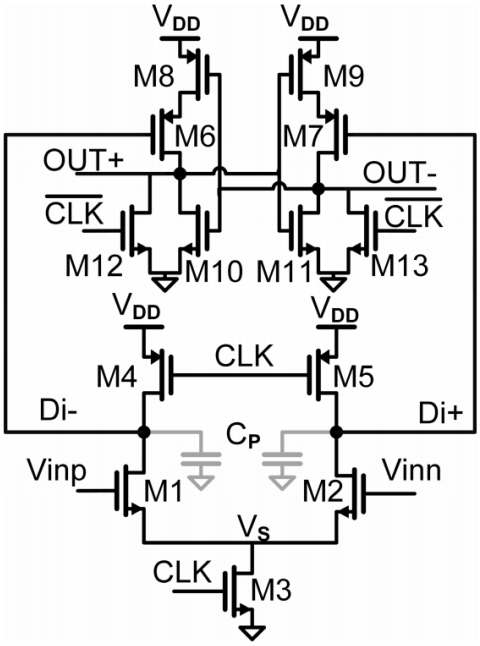


Figure 4. The Elzakker's comparator.

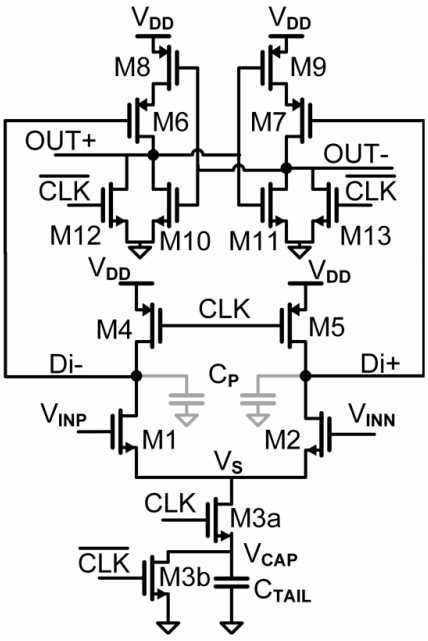


Figure 5. The DB comparator.

The article analyzes the voltage gain of DB Pre-Amplifier,

$$A_V(T_{\mathrm{INT}}) = \frac{C_{\mathrm{TAIL}}}{2n \cdot C_P} \frac{V_s(T_{\mathrm{INT}})}{\frac{kT}{q}} . \tag{1}$$

According to the formula, increasing the voltage at point S can increase the voltage gain, a higher voltage gain means a smaller input-referred noise voltage. When operating in strong inversion region, the input-referred noise is

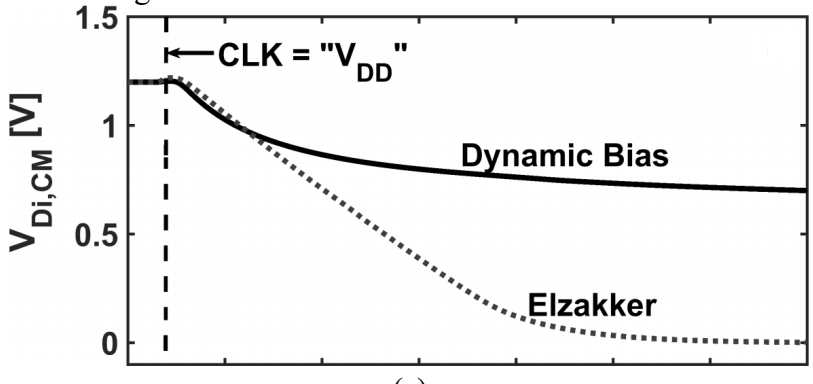
$$E\left[v^2_{\mathrm{n,SI,in}}(T_{\mathrm{INT}})\right] = \frac{4kT\Upsilon}{C_P \cdot \Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) \cdot \left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{\mathrm{SI},T_{\mathrm{INT}}}}, \tag{2}$$

and when operating in weak inversion region, the input-referred noise is

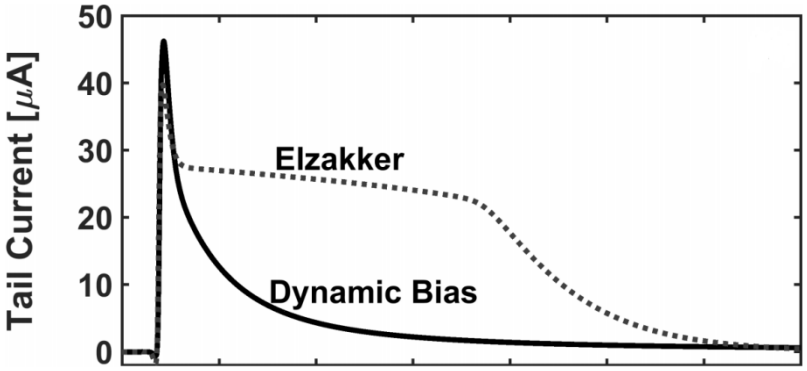
$$E\left[v^2_{\mathrm{n,WI,in}}(T_{\mathrm{INT}})\right] = \frac{2nkT}{C_P \cdot \Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) \cdot \left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{WI,T_{\mathrm{INT}}}}. \tag{3}$$

Typically in 65-nm bulk CMOS processes, the parameters 4kTϒ and 2nkT in Elzakker's comparator and DB Pre-Amplifier are roughly equal in value [6]. Therefore, the input-referred noise of both designs is mainly determined by gm/Id, and reducing V_{OV} increases gm/Id, which reduces the noise.

When V_S is small enough, the circuit will work in the sub-threshold region, this also means a lower energy consumption. A smaller changes in the common-mode output voltage brings a lower energy consumption. A tail current that decreases faster and reaches a steady value will also reduce energy consumption, as shown in Figure 6.



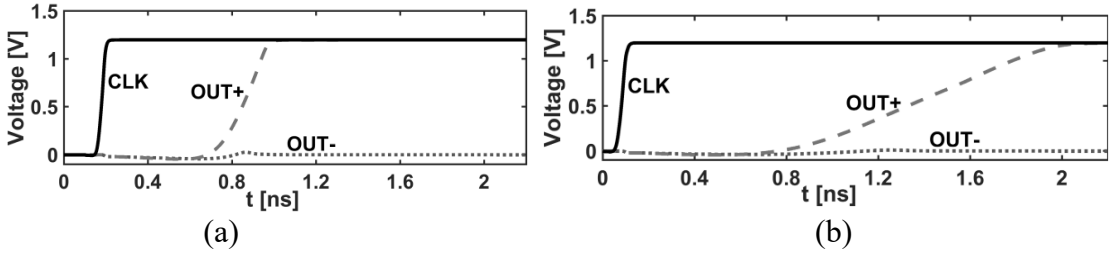
(a)



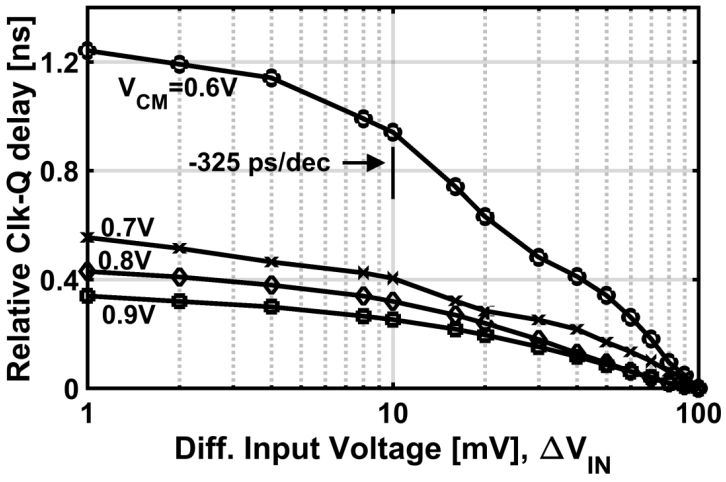
(b)

Figure 6. Simulation results of (a) output common-mode voltage and (b) tail current profile of the two comparators.

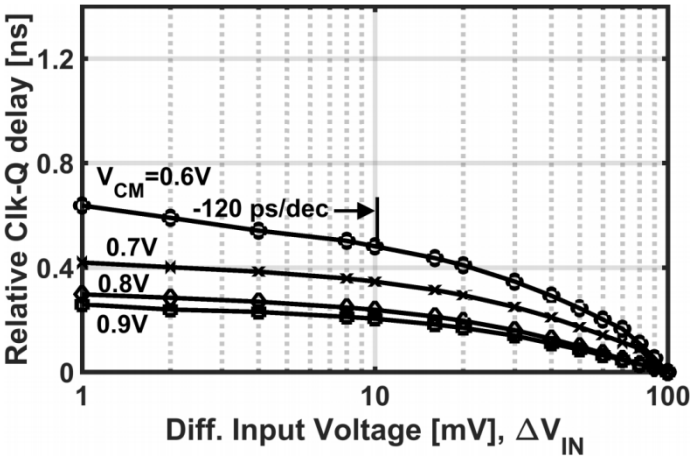
According to the simulation results of the Elzakker comparator and the proposed DB comparator [Figure 7], the OUT of the proposed comparator changes for a longer time, which will lead to a longer delay of the DB comparator. According to the simulation of the Relative CLK-Q delay, this can also be obtained in conclusion.



(a) (b)



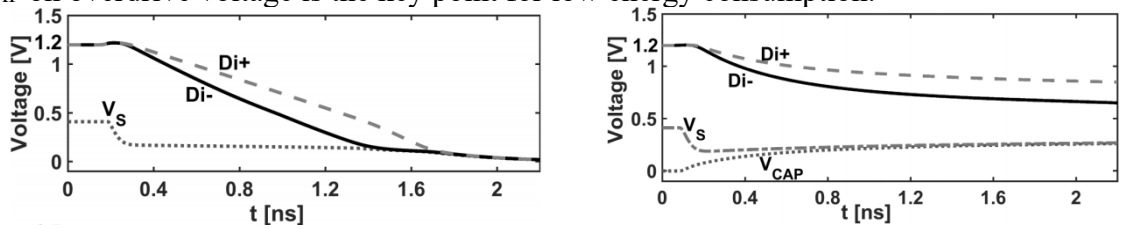
(c)



(d)

Figure 7. (a) Elzakker's comparator and (b) DB comparator timing waveform and delay of the (c) DB comparator and (d) Elzakker's comparator for various V_{CM}.

However, when analyzing the voltage at point S [Figure 8], the V_S of the DB comparator reached a relatively stable value and began to increase slightly under the influence of the voltage of V_{CAP}, while the V_S of the Elzakker comparator was completely discharged with the changes of Di+ and Di- voltages and dropped to zero. This characteristic of incomplete discharge makes the energy consumption of the DB comparator much smaller than that of the Elzakker comparator. So the effect of V_{CAP} on overdrive voltage is the key point for low energy consumption.



(a) (b)

Figure 8. Simulated voltage of (a) Elzakker's comparator and (b) DB comparator at node Di+, Di- and V_S.

In order to get the best energy consumption, the article finally chooses to use the design in the case of V_{CM}=6V. But when considering the delay, setting V_{CM} to 8V will be a better choice. When V_{CM}=0.8 V, the DB comparator saves approximately 2 times the energy of the Elzakker comparator and the CLK-Q delay of the DB comparator is slightly worse than the delay of the Elzakker comparator [6]. Also, when the value of V_{CM} has a small change, it can still ensure that the energy of the former design is much better than that of the latter, and the delay has only a small deterioration.

4. The floating inverter amplifier (FIA)-based pre-amplifier [2]

A floating inverter amplifier (FIA)-based pre-amplifier is used in an energy-efficient dynamic comparator that is proposed to further solve the DB Comparator's difficulties with energy consumption and delay. In comparison to its predecessor, the suggested comparator improves energy efficiency by more than 2.5 times and offers a smaller delay. Additionally, it is guaranteed that the comparator will be insensitive to input common-mode levels.

This article is improved on the basis of DB integration since it stops the loading capacitors from discharging completely, which lowers energy consumption. However, the integration fails in the extreme corner, such as SF or FS, due to the absence of CMFB. In order to provide a constant output common-mode voltage without a CMFB circuit, the two tail capacitors C_{TAIL} in this work are

combined into a single floating reservoir capacitor C_{RES}. The design is a FIA-based pre-amplifier followed by a regenerative latch, as shown in Figure 9.

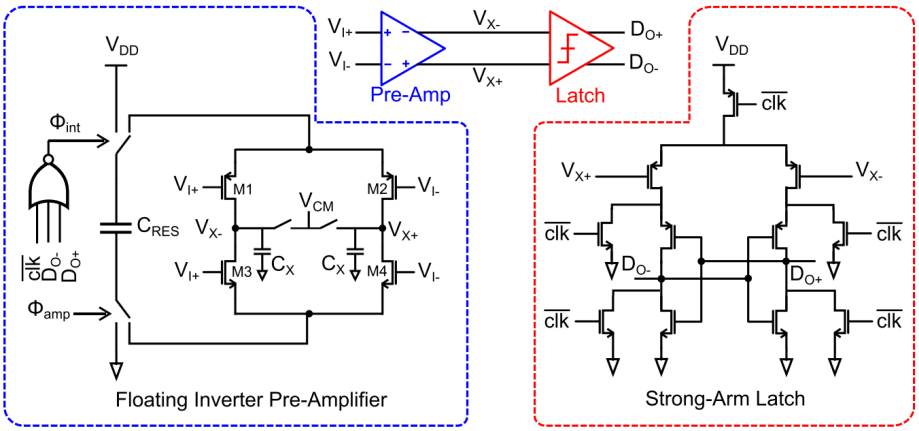


Figure 9. Comparator with FIA.

The noise equation for the pre-amplifier is

$$\sigma_{in,\mathrm{FIA}}^2(T_{\mathrm{INT}}) = \frac{2nkT}{C_{\mathrm{RES}} \cdot \Delta V_S(T_{\mathrm{INT}})} \cdot \frac{I_D}{G_m}. \tag{4}$$

Equation (4) states that the proposed FIA's noise is proportional to I_D/Gm. To balance energy consumption and thermal noise, the article defines a figure of merit to represent the comparator's energy efficiency.

$$\mathrm{FoM}_{\mathrm{FIA}} = 4nkT \cdot V_{\mathrm{DD}} \cdot \frac{I_D}{G_m}. \tag{5}$$

It can be seen that FoM is also inversely proportional to Gm/I_D. By definition, when both energy and input-referred noise are taken into account, a smaller FoM indicates greater performance. Therefore, the energy efficiency of the design can be improved by increasing the value of Gm/I_D [7]. A larger Gm/I_D means a smaller overdrive voltage, which also shows that when the MOS works in the sub-threshold region or even the deep sub-threshold region, it will bring better performance.

Compared to the previous design, the advantage of the proposed comparator is that the noise of the circuit is only related to the introduced capacitance [8]. And the noise of the SA latch comparator and the DB Comparator are affected by their parasitic capacitance.

$$\sigma_{\mathrm{in,SA}}^2(T_{\mathrm{INT}}) = \frac{2nkT}{V_{\mathrm{THN}} \cdot C_X} \cdot \frac{I_D}{g_m}, \tag{6}$$

$$\sigma_{\mathrm{in,DB}}^2(T_{\mathrm{INT}}) = \frac{2nkT}{C_p \cdot \Delta V_{X,\mathrm{CM}}(T_{\mathrm{INT}})} \cdot \frac{I_D}{g_m}, \tag{7}$$

$$\sigma_{in,\mathrm{FIA}}^2(T_{\mathrm{INT}}) = \frac{2nkT}{C_{\mathrm{RES}} \cdot \Delta V_S(T_{\mathrm{INT}})} \cdot \frac{I_D}{G_m}. \tag{8}$$

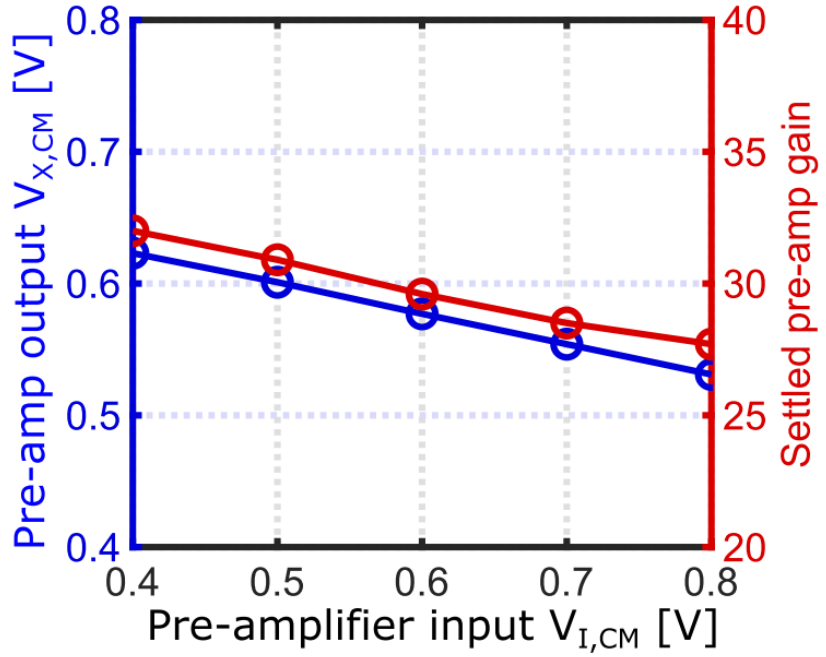
According to the formulation of the SA structure and the Dynamic Bias Latch-Type Comparator, parasitic parameters C_X and C_p influence the input referred-noise. To get a smaller input-referred noise, larger parasitic capacitance C_X and C_p are needed. Transistor size needs to be carefully designed to meet demand, which greatly increases the complexity of the circuit [9]. While the capacitance C_{RES} in FIA pre-amplifier is not a parasitic parameter and can be adjusted independently.

In practice, due to the existence of parasitic capacitance, the common mode output voltage will change slightly. According to the circuit analysis, the formula of the common mode output voltage can be obtained:

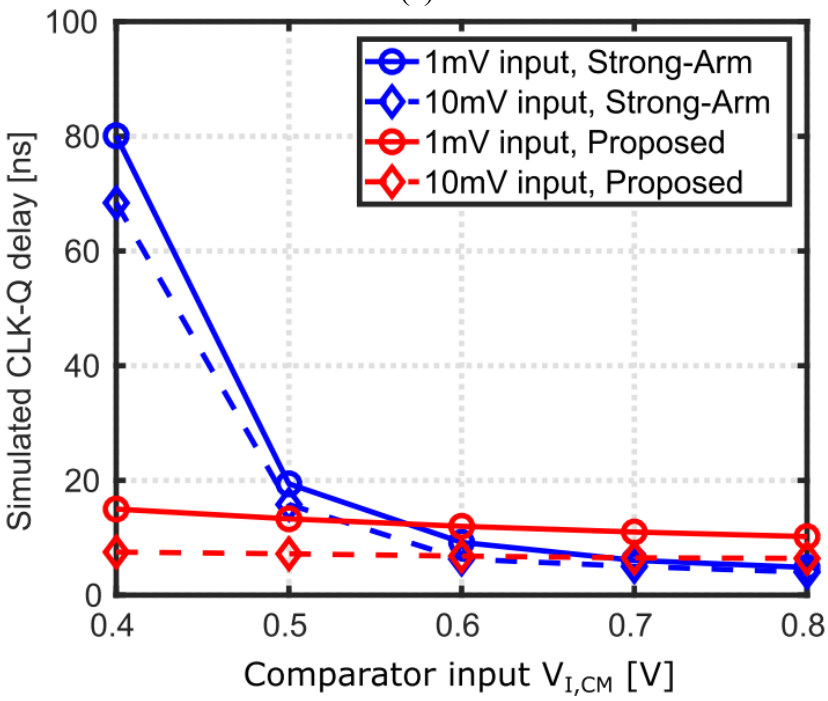
$$\Delta V_{X,\mathrm{CM}} \approx -2 \cdot \Delta V_{I,\mathrm{CM}} \cdot \frac{C_P}{C_X}. \tag{9}$$

Since C_P is not constant, it is necessary to select a larger C_X to obtain a more stable common-mode output voltage, but this will reduce the voltage gain, which will affect the input-referred noise. Also, a larger C_X will bring an area penalty.

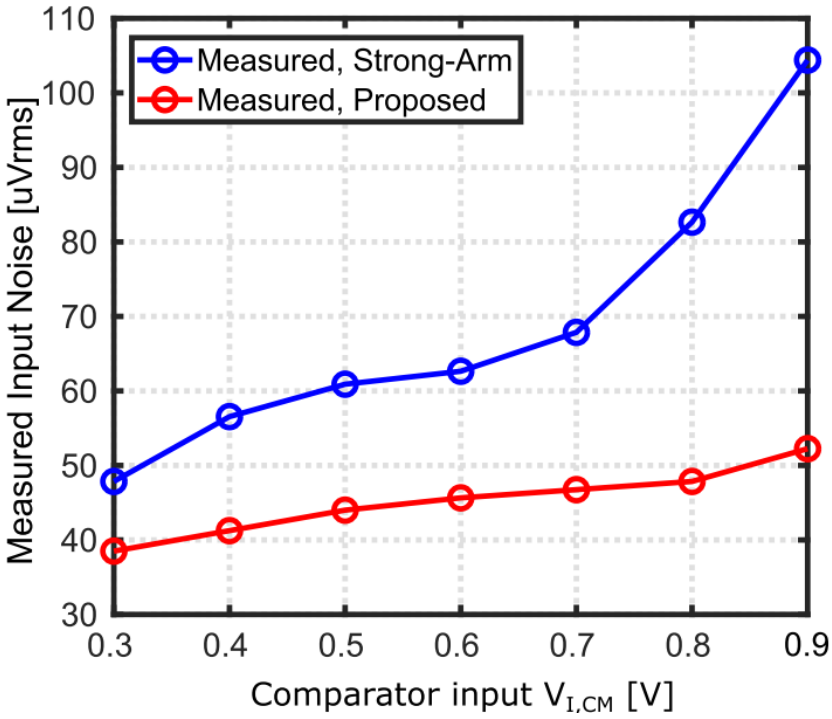
Due to the presence of parasitic capacitors, the input common-mode voltage will also have an impact on the common-mode output voltage in addition to the former. A more stable common-mode output voltage will extend the integration time and increase the gain [10]. At the same time, the common mode input voltage will have an impact on CLK-Q delay and noise, so discussing the common mode output voltage, noise and speed together is necessary.



(a)



(b)



(c)

Figure 10. Results of the simulation of (a) $V_{X,CM}$ and gain of the pre-amplifier versus $V_{I,CM}$, (b) the delay versus $V_{I,CM}$ and (c) the noise for the FIA-based comparator and the SA latch $V_{I,CM}$.

According to the line chart of common mode output voltage, noise and CLK-Q delay, V_{CM}=0.5V is finally selected. When V_{CM}=0.5V, the CLK-Q delay of the FIA-based comparator is still smaller than the SA latch, and noise performance is also better than the SA latch.

5. Conclusion

This paper mainly focuses on the optimization problem of comparator's energy. The Triple-tail comparator breaks mutual influences between speed and noise through a multi-stage structure. However, this structure brings an energy penalty.

By utilizing a floating reservoir capacitor, the FIA-based pre-amplifier achieves current recycling, increases Gm/I_D, and partial discharge of the capacitors. Compared with the DB comparator, the energy consumption is improved by 2.5 times and the structure significantly improves CLK-Q delay.

The DB Comparator improves power efficiency by designing a new structure to prevent the capacitance of the tail current source from being fully charged and discharged. Compared to its predecessor, the DB comparator is more than 2 times energy-efficient.

As the first work which introduce the capacitor as the source tail to further improve energy efficiency, the DB Comparator still needs some improvements in other aspects. The innovation gets a worse speed performance than its predecessor due to its operation in the sub-threshold region. Also, the DB Comparator needs to be balanced between speed and noise. Future work should focus on addressing these two issues.

References

[1] Shweta Srivastava and Nitin Gupta 2017 Conf. on Innovations in Control, Communication and Information Systems

[2] Tang Xiyuan, Shen Linxiao, Kasap Begum, Yang Xiangxing, Shi Wei, Mukherjee Abhishek, Pan David Z and Sun Nan 2020 IEEE Journal of Solid-State Circuits vol 55, pp 1011-1022

[3] Schinkel D, Mensink E, Klumperink E, Van Tuijl E, and Nauta B 2007 Proc. Int. Conf. on Solid-State Circuits pp 314-605

[4] Ramkaj A T, Strackx M, Steyaert M S J and Tavernier F 2018 IEEE Journal of Solid-State Circuits vol 53 pp 1889-1901

[5] Wicht B, Nirschl T, and Schmitt-Landsiedel D 2004 IEEE J. Solid-State Circuits vol 39 pp 1148–1158

[6] Bindra H S, Lokin C E, Schinkel D, Annema A J and Nauta B 2018 IEEE Journal of Solid-State Circuits vol 53 pp 1902-1912

[7] Liu M, Roermund A H M van and Harpe P 2017 IEEE J. Solid-State Circuits vol 52 pp 2979-2990

[8] Lin J Y and Hsieh C C 2015 IEEE Trans. Circuits Syst. I, Reg. Papers vol 62 pp 70-79

[9] Ginsburg B P and Chandrakasan A P 2005 Proc. IEEE Int. Symp. Circuits Syst. vol 1 pp 184-187

[10] Sepke T, Holloway P, Sodini C G and Lee H S 2009 IEEE Trans. Circuits Syst. I, Reg. Papers vol 56 pp 541-553