Research Progresses on Suppressing the Short-Channel Effects of Field-Effect Transistor

Junyuan Huang[1, *]

[1]School of Material Science and Engineering, Shanghai University, Shanghai, China

*Corresponding author: huang1122@shu.edu.cn

Abstract: Recently, with the continuous miniaturization and integration of microelectronic devices in all fields, the conventional MOSFET structure has suffered from severe short channel effects with continuous downsizing. In order to further improve the electrical properties of Very Large-Scale Integration Circuit (VLSI) and obtain the larger device integration density in circuits, new revolution in MOSFET technology is needed, which involves the innovations of new materials, new technologies, and new device structures. This paper explores device structure innovations in traditional planar transistors, such as the device performance enhancement via the high-κ/metal gate and especially the three-dimensional device structure — FinFET, as well as the subsequent development of gate-all-around FET proved to outperform FinFET. The development of high-performance devices based on new materials has become an imperative direction to break through the current bottleneck of silicon-based technologies. This paper focuses on an overview of transition-mental dichalcogenides and ferroelectric materials, including frontier research and current inadequacies. Based on these new approaches, VLSI manufacturing technology has seen many breakthroughs in recent years, which will successfully extend Moore's Law and further promote the development of emerging technologies in multiple fields.

Keywords: Short Channel Effect, FinFET, GAAFET, TMDs, Ferroelectric.

1. Introduction

Chip has become the foundation of the information technology era, in which all electronic products and systems in our life are inseparable from chips. Chips are integrated circuits with transistors and electronic circuits fabricated on the surface of the semiconductor to perform logical operations. Gordon Moore stated in 1965 that the number of transistors per unit area of a chip would double every two years in the future, which is called Moore's Law. At the International Electron Device Meeting (IEDM) in 1975, he emphasized that the continuous growth in the number of transistors on a chip was mainly due to the constant miniaturization of transistor size. Therefore, it is the relentless pursuit of chip manufacturers and researchers to create smaller and less energy-consuming integrated circuits. For nearly 60 years, the growth of the chip industry has been fueled by Moore's Law. Currently, commercial silicon-based transistors are facing increasing challenges to perpetuate Moore's Law as the size scaled down with the advancement of process technology, from the earliest micron scale to nanometer scale. MOSFET is the basic device structure of present integrated circuits and shorten the gate length is the most effective way to enhance the performance of MOSFET devices. With continuous device scaling, short-channel effects (SCEs) induced by the channel length reduction, such as threshold voltage shift, high subthreshold swing and drain-induced-barrier-lowering (DIBL) effect, seriously impede the improvement of the device performance. However, scaling is an inexorable trend. Therefore, various practical measures must be taken in order to reduce these effects. To suppress the SCEs mentioned above, researchers have proposed numerous new transistor structures. FinFET is regarded as the most promising structure to replace planar structures beyond 22 nm process node. It provides superior electrostatic control over the channel by gate-wrapped structure, leading to better SCE control and decreasing leakage current. Compared to planer structure MOSFET, FinFET has advantages of reducing the subthreshold swing with low DIBL. Nevertheless, the need for continuous size downscaling of transistors below 3 nm technology node is a demanding task and requires new structures to further improve gate control. Gate-all-around (GAA) FETs have been

reported to replace FinFET as a dominant structure due to its better control of the channel transport through fully surrounded gate. Apart from device structural optimization, the exploitation and employment of novel materials is constantly emerging. Conventional silicon-based transistors are approaching their physical limits. Whereas continuing downsizing brings unfavorable factors such as SCEs will cause higher power consumption and affect reliability and stability of the device, the breakthrough in the process of silicon-based materials is of greater difficulty. There is an urgent demand to find novel materials as an alternative. Transition-mental dichalcogenides (TMDs) like molybdenum disulfide (MoS_2) are an exciting member of two-dimensional (2D) materials family, featuring smooth surfaces lacking hanging bonds and atomic thin nature. Therefore, devices based on these materials show high electron mobility and high on/off ratios. Intensive research has been conducted on TMD-based FET devices to improve performance and lower leakage current in the past few years. Other emerging materials such as ferroelectric dielectric materials employed in negative capacitance FETs are gaining popularity to enhance the device performance with higher scope of scalability. On the basis of all the above, this paper reviews the existing approaches to suppress the SCEs of transistors in recent years, including device structure improvement and new material development. Future directions for transistor development in the post-Molar era are proposed.

2. Device structure

2.1 FinFET

Traditional planar MOSFETs are more severely affected by the SCEs when developed to the 22 nm-node. In 1998, Prof. Chenming Hu of the University of California at Berkeley first proposed the FinFET structure as a breakthrough to overcome the SCEs [1]. The FinFET structure transforms the original planar structure into three dimensions. The planar structure is shown in Figure 1. The gate-wrapped structure enhances the gate control and provides superior electrical control over the channel, thus reducing the leakage current and suppressing the SCEs. In addition, the FinFET structure eliminates channel doping and suppresses the threshold voltage fluctuation, consequently avoiding the effect of random dopants fluctuation (RDF). Therefore, FinFET becomes a mainstream design in the integrated circuit fabrication industry.

According to the substrate type, the structure can be divided into bulk silicon FinFET and silicon-on-insulator (SOI) FinFET [2]. Figure 1. displays different constructions for SOI and Bulk FinFETs. The former buried oxide layer reduces the source-drain parasitic capacitance and isolates the leakage current; the disadvantage is that the silicon dioxide around the transistor is poor in heat dissipation. Compared to silicon, silicon dioxide has a heat conductivity that is two orders of magnitude lower, which degrades the performance of device. That is called the "self-heating effect". The gate/gate dielectric layer material has evolved from polysilicon gate/silicon dioxide dielectric layer to metal gate/high-κ dielectric layer. As the process node scales down further, the use of high-κ dielectric materials like HfO_2 has been effective in increasing the gate oxide capacitance and alleviating the gate leakage caused by the thinning of the SiO_2 layer. The replacement of polysilicon by metal gates can eliminate polysilicon depletion effect and improve carrier mobility with better combination of high-κ dielectric materials.

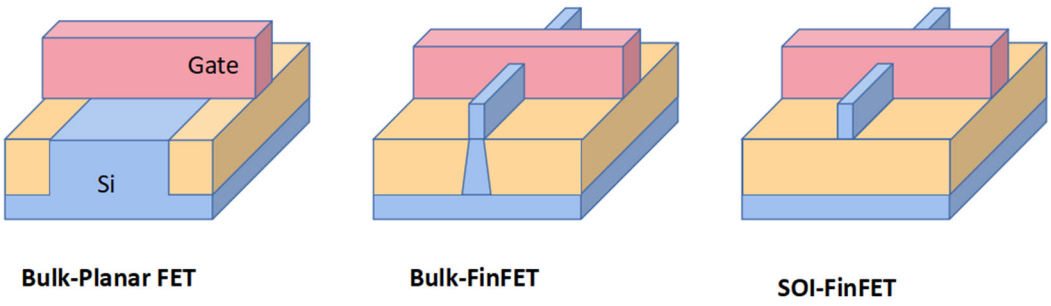

Figure 1. Planar FET and FinFET (Photo credit: Original)

2.2 GAAFET

As the process enters the 3 nm-node technology, higher requirements for gate control are put forward. SCEs such as increased subthreshold swing and reduced drain potential barriers have reappeared as a challenge for MOSFET development. In order to continue Moore's Law, a stacked nanowire/nanosheet GAA structure has been developed based on FinFET, as shown in Figure 2, which offers superior SCE control and more variable width design than FinFET.

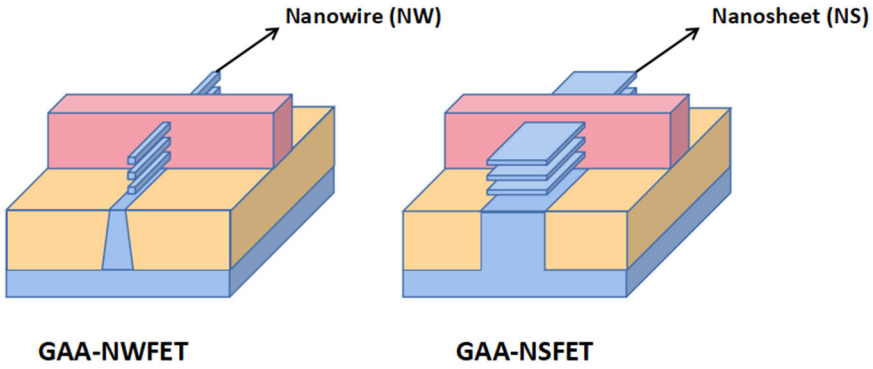

Figure 2. Structure of different GAAFETs (Photo credit: Original)

GAAFETs are reportedly manufactured in two distinct structures: horizontal GAAFET (HFET) and vertical GAAFET (VFET). In 2017, IBM demonstrated the horizontal GAA Nanosheet structure for the first time. Compared to Fin FET, it gets an increase in W_{eff}, using less complex patterning strategy with EUV lithography [3]. However, VFETs exhibit better scalability and ultimately surpass HFETs in terms of both speed and power consumption beyond 7-nm technologies, while further scaling of HFETs is strongly limited by contact resistance [4]. When compared to HFETs from the layout perspective, 2-tier VFET standard cells indicate better advantages, providing a 50.1% area reduction as well as wire length and parasitic capacitance reduction, respectively [5].

Multi-bridge channel field effect transistors (MBCFETs), developed on the basis of GAA, represent a great advancement in CMOS technology by improving device performance while saving area and overcoming current physical limitations. Samsung presented 3 nm MBCFET based on GAA technology with three superior characteristics compared to FinFET—better gate control, higher performance with larger W_{eff} and more flexible design with variable nanosheet widths [6]. TSRI successfully fabricated CMOS devices based on SiGe p-GAAFET and Si n-GAAFET by adopting two selective etching approaches to obtaining the MBCs. The etched surfaces demonstrate an on/off ratio over 10^5 with a subthreshold swing of 90 mV/decade [7].

2.3 Complementary FET (CFET)

CFET is a promising candidate for the development of 3D CMOS technology, which has received a considerable attention for extending Moore's Law. It has nFET and pFETs that are vertically stacked, which allows for a significantly smaller CMOS footprint. To enable access to device pins comprising a CEFT with a 5-terminal structure, double stacked source/drain electrodes are employed [8].

Imec demonstrated the scaling potential of CFET device beyond 3 nm by vertically stacking n-type sheet on p-type fin [9]. It shows a 50% area scaling for both standard cells and SRAM. With TCAD analysis, CFETs can ultimately outperform FinFET devices in terms of power consumption and performance, satisfying the 3 nm target. Samsung proposed a Digital LDO fabricated in a 3 nm GAAFET CMOS process, achieving high current density of 34.15 A/mm^2 and fast response characteristic of 38 mV droop at 1 A/1ns load current condition [10].

3. Materials design

3.1 Transition-mental dichalcogenides (TMDs)

2D materials, particularly TMDs like MoS_2, WSe_2, WS_2 etc. have attracted considerable attention as next-generation semiconductor materials. TMDs with atomic scale thickness as the channel materials for FETs provide the potential to effectively suppress SCEs on device, thus achieving breakthrough in performance and further extending Moore's Law. During the recent years, FETs using TMDs have been extensively investigated with the purpose of improving their performance and reducing leakage further.

A. Kumar et al. reported bilayer WS_2 transistors doped with sub-stoichiometric aluminum oxide (AlO_X) to overcome a sharp degradation in the on/off ratio generally caused by doping. The transistor shows record in WS_2 with an on-current of 80 μA/μm (per layer) and an off-current of approximately $5x10^{-13}$ A/μm along with large on/off ratio up to 10^8 [11].

F. Ahmed et al. proposed an optimized MBCFET fabricated with TMD, which demonstrated improved performance over conventional MBCFET [12]. It consists of WTe_2 nanosheets and Nb_2O_5 as high-κ dielectric, indicating a subthreshold swing of 64.60 mV/decade and a threshold voltage of 0.57 V at room temperature, whose on/off ratio is 2.53 times higher than the conventional devices.

Conventional TMD-based devices remain using Au as the electrode to collect carriers. However, the operating speed and carrier collection efficiency of this structure is limited because of the metal-induced gap states (MIGS) between channel materials and electrode. High contact resistance and low delivery capabilities are caused by Schottky barriers. Thus, nonmetallic materials become a powerful alternative to avoid the above issues. Using graphite for the source/drain electrodes can greatly increase carrier collection efficiency. Comparing MoS_2 FETs with two graphite contact electrodes to those with Au electrodes, the on/off current ratio increases by about two orders of magnitude [13].

Excellent ohmic contact has been observed by MIT and TSMC between semi metallic Bi and semiconducting monolayer TMDs , where the MIGS are effectively suppressed. This technology reveals the true potential of TMD-based transistors, enabling further scaling of devices and extending Moore's Law. W. Li et al. used semi-metallic bismuth in the top-gate of MoS_2 as source/drain electrodes to achieve zero Schottky barrier. The short-channel device sets a new record for top-gate 2D FETs at monolayer thickness with an on-current of 680 A/m at 60 nm gate length [14]. The source/drain electrodes for the MoS_2 FET were made by the Hong Kong University by platinum evaporation in high vacuum and O_2 passivation [15].

Due to the difficulty in removing charge scatters and traps, the creation of reliable high-κ materials combined with 2D TMDs while scaling their capacitance equivalent thickness (CET) has proven to be challenging. J. Huang et al. explored gate dielectric for 2D FET using transferrable $SrTiO_3$ with high-κ single crystals which displays a desirable sub-nanometer CET with little leakage current. Transistors are discovered to have subthreshold swings and on/off ratios of 70 mV/decade and 10^7 mV/decade, respectively [16].

3.2 Ferroelectric materials

The ferroelectric-negative-capacitance-field-effect-transistor (FE-NCFET) is an emerging transistor, which can be realized through incorporating a ferroelectric layer within the transistor's gate in place of the traditional gate dielectric layer. The subthreshold swing and on/off ratio of the transistor can be effectively enhanced by amplifying the effect of the gate voltage on the channel, theoretically lowing subthreshold swing to below 60 mV/decade, which is called negative capacitance effect. Among traditional ferroelectric materials such as $BaTiO_3$, PZT etc., HfO_2-based ferroelectric materials has been projected as one of the most promising materials due to its perfect compatibility with silicon processes. HfO_2-based films with ferroelectricity can possibly be obtained by incorporating cation dopants such as Zr, Si, Al, La etc.

A. Khan et al. constructed NC-FinFET with 100 nm gate length by using an epitaxial $BiFeO_3$ ferroelectric capacitor [17]. The drain current displays steep swings of 8.5 to 50 mV/decade over 6 to

9 orders of magnitude. B. Obradovic et al. investigated the delayed response of FE-domain switching by modeling HfZrO/SiO_2 FE-dielectric FETs [18], referred to as transient NC, where the voltage applied to the ferroelectric layer changes in opposite reaction to the charge over a short period of time. This transient NC phenomenon was first observed in an R-C_{FE} series circuit.

FE-NCFETs are generally available in two architectures: metal-ferroelectric-insulator-semiconductor (MFIS) or metal-ferroelectric-metal-insulator-semiconductor (MFMIS). The intermediate metal works as a floating gate in an MFMIS architecture. G. Pahwa et al. compared two types of devices and the analysis revealed that MFIS device has obviously superior performances regarding on-current as well as subthreshold swing than MFMIS devices [19]. In comparison to its baseline 14 nm FinFET counterparts, NC-FinFETs based on MFIS structure display a better immunity to fluctuation. When compared to baseline FinFETs in n-type and p-type devices, NC-FinFETs exhibit significantly smaller subthreshold swings that are reduced from 76.24 mV/decade to 66.78 mV/decade and from 80.77 mV/decade to 68.75 mV/decade, respectively [20]. S. Cheema et al. reported ferroelectricity in Zr doped HfO_2 grown by low-temperature atomic layer deposition (ALD) on silicon. The research demonstrates that the subthreshold swing of NCFETs with Zr-doped HfO_2 is decreased by 20mV/decade compared to that of NCFETs without Zr doping. In 2022, they reported HfO_2-ZrO_2 superlattice heterostructures as a gate stack with lower leakage current and no mobility degradation than conventional HfO_2-based high-κ materials [21]. It can be scaled down to almost 20 Å and directly integrated onto silicon-based transistors. The Integration of the NC and TMD channel based devices could be an attractive solution to extend power supply scaling. A. Nourbakhsh proposed Al-doped HfO_2 ferroelectric films to develop NC-MoS_2 FETs. The device shows a significant enhancement of the subthreshold swing to 57 mV/decade with 10 nm 7.3% Al:HfO_2 as a gate dielectric [22].

4. Discussion

With the evolution of integrated circuits, the feature size of transistors continues to scale down, propelled by Moore's law. At the 22 nm process node, the conventional planar MOSFET encounters inevitable challenges for further downsizing. The excessive short gate length has a dramatically reduced control over the current, and thus leakage current increases, suffering from severe SCEs. The ensuing FinFET structure was proposed to perpetuate the Moore's Law by transforming the gate from a planar structure to a 3D layout, enhancing the gate's ability to control the channel current. Nevertheless, the FinFET structure is gradually reaching its physical limits below 3 nm technology node. GAA features transistor gate to channel wrapping on all sides, source and drain no longer in contact with the substrate, which provides greater control over the channel, thus breaking through the technical hurdles that FinFET is hard to surpass. Samsung is the first company in the world to use GAA technology, migrating from FinFET at the 5 nm node to GAA at the 3 nm node, proposing MBCFET that use multilayer stacked nanosheets to replace the nanowires in the conventional GAA structure, making manufacturing simpler. TSMC, another Foundry giant, still continues the previous FinFET structure at the 3 nm node and will introduce the GAA structure at 2 nm. Currently, Samsung is leading TSMC announced that the 3 nm process node based on the GAA structure of the chip has begun initial mass production. However, its yield rate remains a problem to be verified in the market. There is no doubt that the switch from FinFET to GAAFET is an inevitable trend after the 2nm process node.

Research on materials to suppress short-channel effects has proliferated in recent years, and the excellent properties of 2D materials have turned them into popular materials for extending Moore's law. The thickness of 2D materials can reach the atomic scale, which means monolayer TMDs can be used as a channel material for transistors, while having good gate control capability, further reducing the size of transistors combined with high-κ dielectrics. Although the TMD is a promising material, it has a long way to go before it can be used commercially in practice, and it has problems such as high contact resistance which results in reduction of mobility below the theoretical value.

Consequently, further research and exploration are required. NCFET adopting ferroelectric dielectric materials is another attractive research direction. Its fabrication process is similar to MOSFET, and it can also be compatible with 2D materials as channel, making the subthreshold swing lower than 60mV/decade and reducing the power consumption of the device. Currently applications based on Fe-NCFET are mainly focused on low-power devices. However, in terms of large-scale adoption, it is essential to solve such problems as the hysteresis phenomenon and gate material coordination, while the prospects for its application are highly promising. The utilization and exploration of new materials and structures is the basis for the continuous development of the chip. Despite the challenges of the process node below the 3 nm, the GAA structure is far from the limit. Combined with Design-Technology Co-Optimization (DTCO), there is considerable potential for reduction in device size and improvement in power performance.

5. Conclusion

The negative impacts caused by SCE have posed a formidable challenge to the continued reduction of chip size. With the advent of the post-Moore era, reducing feature size and improving device performance remain the direction of integrated circuit development. While the innovation and combination of new materials, new processes, and new structures will be the core strategies and targets for extending the Moore's law. This paper reviews the structural development of MOSFETs from planar to three-dimensional structures, from FinFETs to GAAs. GAAs are expected to replace FinFETs as mainstream devices to achieve 3 nm mass production, and even smaller gate lengths are possible. The construction of transistor channel materials with TMDs as representative two-dimensional materials is a new attempt to combine materials and structures, providing an innovation concept for the development of novel transistor devices in the post-Moore era. Other emerging materials such as ferroelectric materials to constitute NCFETs are also an attractive technology direction because of their compatibility with CMOS process and low subthreshold swing, low power consumption characteristics. The development of integrated circuits in the post-Moore era will be a co-optimization technology of design, materials, and structure, combined with new packaging processes to improve performance, reduce power consumption, and promote the development of multi-field emerging technology research such as artificial intelligence and Internet of Things (IOT). Integrated circuits have a promising future and market demand in the information society and digital era.

References

[1] Hisamoto, D., Lee, W. C., Kedzierski, J., et al. A folded-channel MOSFET for deep-sub-tenth micron era [J]. IEDM Tech. Dig, 1998, 1998: 1032-1034.

[2] Deshmukh, R., Khanzode, A., Kakde, S., et al. Comparing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance. In proceedings of: 2015 International Conference on Computer, Communication and Control (IC4). IEEE, Indore, India, 2015: 1-4.

[3] Loubet, N., Hook, T., Montanini, P., et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In proceedings of: 2017 Symposium on VLSI Technology. IEEE, Kyoto, Japan, 2017: T230-T231.

[4] Yakimets, D., Eneman, G., Schuddinck, P., et al. Vertical GAAFETs for the ultimate CMOS scaling [J]. IEEE Transactions on Electron Devices, 2015, 62(5): 1433-1439.

[5] Song, T. Many-tier vertical GAAFET (V-FET) for ultra-miniaturized standard cell designs beyond 5 nm [J]. IEEE Access, 2020, 8: 149984-149998.

[6] Bae, G., Bae, D. I., Kang, M., et al. 3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications. In proceedings of: 2018 IEEE International Electron Devices Meeting (IEDM). IEEE, San Francisco, CA, USA, 2018: 28.7. 1-28.7. 4.

[7] Chang, W. Y., Chu, C. L., Luo, G. L., et al. Investigation on selectively etched SiGe and Si surface for Gate-All-Around CMOS devices fabrication. In proceedings of: 2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA). IEEE, Hsinchu, Taiwan, 2022: 1-2.

[8] Sun, B., Xu, Z., Ding, R., et al. Analytical model of CFET Parasitic capacitance for advanced technology nodes [J]. IEEE Transactions on Electron Devices, 2022, 69(3): 936-941.

[9] Ryckaert, J., Schuddinck, P., Weckx, P., et al. The Complementary FET (CFET) for CMOS scaling beyond N3. In proceedings of: 2018 IEEE Symposium on Vlsi Technology. IEEE, Honolulu, HI, USA, 2018: 141-142.

[10] Kim, S., Lee, H., Lee, Y., et al. A 3nm GAAFET Analog Assisted Digital LDO with High Current Density for Dynamic Voltage Scaling Mobile Applications. In proceedings of: 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits). IEEE, Honolulu, HI, USA, 2022: 190-191.

[11] Kumar, A., Nazif, K. N., Ramesh, P., et al. Doped WS 2 transistors with large on-off ratio and high on-current. In proceedings of: 2020 Device Research Conference (DRC). IEEE, Columbus, OH, USA, 2020: 1-2.

[12] Ahmed, F., Paul, R., Saha, J. K. Comparative Performance Analysis of TMD based Multi-Bridge Channel Field Effect Transistor. In proceedings of: 2020 IEEE 10th International Conference Nanomaterials: Applications & Properties (NAP). IEEE, Sumy, Ukraine, 2020: 01TPNS04-1-01TPNS04-5.

[13] You, J., Zhang, Y., Yang, M., et al. Effect of Graphite as electrodes on electrical and photoelectrical behavior of multilayer MoS2 and WS2 FETs [J]. IEEE Transactions on Electron Devices, 2022, 69(9): 5324-5329.

[14] Li, W., Fan, D., Shao, L., et al. High-performance CVD MoS 2 transistors with self-aligned top-gate and Bi contact. In proceedings of: 2021 IEEE International Electron Devices Meeting (IEDM). IEEE, San Francisco, CA, USA, 2021: 37.3. 1-37.3. 4.

[15] Estrada, C. J., Ma, Z., Chan, M. Complementary Two-Dimensional (2-D) MoS 2 FET Technology. In proceedings of: ESSDERC 2021-IEEE 51st European Solid-State Device Research Conference (ESSDERC). IEEE, Grenoble, France, 2021: 219-222.

[16] Huang, J. K., Wan, Y., Shi, J., et al. High-κ perovskite membranes as insulators for two-dimensional transistors [J]. Nature, 2022, 605(7909): 262-267.

[17] Khan, A. I., Chatterjee, K., Duarte, J. P., et al. Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor [J]. IEEE Electron Device Letters, 2015, 37(1): 111-114.

[18] Obradovic, B., Rakshit, T., Hatcher, R., et al. Modeling transient negative capacitance in steep-slope FeFETs [J]. IEEE Transactions on Electron Devices, 2018, 65(11): 5157-5164.

[19] Pahwa, G., Dutta, T., Agarwal, A., et al. Compact model for ferroelectric negative capacitance transistor with MFIS structure [J]. IEEE Transactions on Electron Devices, 2017, 64(3): 1366-1374.

[20] Gupta, A., Chauhan, N., Prakash, O., et al. Variability Effects in FinFET Transistors and Emerging NC-FinFET. In proceedings of: 2021 International Conference on IC Design and Technology (ICICDT). IEEE, Dresden, Germany, 2021: 1-4.

[21] Cheema, S. S., Shanker, N., Wang, L. C., et al. Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors [J]. Nature, 2022, 604(7904): 65-71.

[22] Nourbakhsh, A., Zubair, A., Joglekar, S., et al. Subthreshold swing improvement in MoS2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO2/HfO2 gate dielectric stack [J]. Nanoscale, 2017, 9(18): 6122-6127.