

A brief review on novel comparator design

Yuan Sun ^{1, *}

¹Department of electronic information engineering, Shanghai University, Shanghai, China

*Corresponding author: 554727113@shu.edu.cn

Abstract: This paper reviewed three different kinds of comparators to show their respective advantage range. The Dynamic-bias comparator extends its pre-amplifier part with a capacitor and has a smaller power with a smaller input referred noise than Elzaker's comparator but has a higher delay. The Quad high-speed comparator introduced the Quad into the comparator's latch part. It has a lower delay and also make the calculation of the output voltage easier for it only depends on the skew factor. The low-power dynamic bias has a cross-couple device on its pre-amplifier part which slows down the discharge of the capacitors. It has a higher delay but lower the energy consumption by 30%.

Keywords: Comparators, Dynamic bias comparator, High-speed comparator.

1. Introduction

With the rapid progress of IC processing, performance of the ADCs has continually been pushed and already achieved the performance limit. In a typical SAR ADC 40%-50% [1] of its whole energy is consumed by the comparator part. In a single comparison the C_p of the pre-amplifier is charged to V_{DD} and then discharged to the ground. In this process, huge amount of energy are actually wasted. It is estimated that about 70%-80% of the energy is taken by the pre-amplifier part. So, in order to improve the energy consumption, it's essential to make some efforts on the comparator.

The typical comparator is consisted of one plus one different section the first pre-amplifier part and the second latch part. Most widely used pre-amplifier use the CMOS as a common mode suppression differential amplification to amplifier the input voltage. And the latch part compared the two different input voltage from the pre-amplifier part and do a logic decision and give out a low or high signal.

This paper has analyzed three different proved comparator and given out their respectively using interval as well as their advantages and shortcomings.

In order to prove the power efficiency of the Elzaker's comparator, a capacitor is added to its pre-amplifier part which stabilized the V_s while making the amplitude of charging and discharging of the circuit more stable in order to decrease the energy consumption. However, the delay of it is largely increased especially when the $V_{cm}=0.6$

The Quad high-speed comparator makes an improvement in the latch part using the Quad to do some stimulation of the circuit. Its delay has been decreased due to the cross-coupled inverters.

The low-power dynamic comparator used a cross-coupled device with a regenerative latch instead of two capacitors in the pre-amplifier and this makes the energy consumption reduced about 30% referring to the original comparator.

This paper is consisted of five parts. Section 2 describes the Dynamic bias comparator. The Quad high-speed comparator is discussed within Section 3. Section 4 reviews low-power dynamic comparator. Finally, the Section 5 makes a brief conclusion of the whole paper.

2. Dynamic-bias comparator

The three different types of comparators are all consisted by two sections. First, the pre-amplifier part and second, the latch type.

Elzaker's comparator Figure. 2 has made some changes on the Double-tail comparator [2] Figure. 1 and makes the power efficiency lower [3].

According to this formula the voltage enlargement of the Double-tail pre-amplifier is determined by the g_m and I_{cm} . These two circuit parameters are given out by the pre-amplifier.

Voltage enlargement of dynamic-bias pre-amplifier is:

$$A_v(T_{INT}) = \frac{C_{TAIL}}{2n \cdot C_p} \frac{V_S(T_{INT})}{\frac{kT}{q}} \quad (2)$$

The voltage enlargement presents by dynamic-bias pre-amplifier is only determined by the C_{tail} and C_p .

This is a very useful improvement because the g_m and I_{cm} are determined by massive elements in the circuit so it's not easy to calculate the theoretical value after some changing in the Double-tail pre-amplifier.

However, the dynamic-bias pre-amplifier's theoretical value can be easily predicted as if the C_{tail} and C_p are known.

The strong inversion noise of the Elzakker's comparator [4] and [5] can be determined by the formula below:

$$V_S(T_{INT}) = \frac{2 \cdot \Delta V_{Di,CM}(T_{INT}) \cdot C_p}{C_{TAIL}} \quad (3)$$

$$E[v_{n,SI,in}^2(T_{INT})] = \frac{4kTY}{C_p \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{g_m}{I_{CM}}\right)_{SI,T_{INT}}} \quad (4)$$

The weak inversion noise of the dynamic bias pre-amplifier is:

$$E[v_{n,WI,in}^2(T_{INT})] = \frac{2nKT}{C_p \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{g_m}{I_{CM}}\right)_{WI,T_{INT}}} \quad (5)$$

The Elzakker's comparator's noise is approximately twice as much as the dynamic bias'.

These formulas indicate that with the increase of $\frac{g_m}{I_{cm}}$ the voltage gain ability of the pre-amplifier is also increasing so the I_{cm} of the pre-amplifier should be as big as possible. But the inversion noise of both comparators shows that in order to get a smaller inversion noise the I_{cm} of the pre-amplifier should be as small as possible.

When working in different input Voltage situation the energy consumption of both comparators doesn't change much. Instead, the V_{cm} of the comparator affects the energy consumption more severely.

Both comparators experienced a 10fJ energy consumption increase when the V_{cm} changes from 0.6V-0.9V.

In each comparison, the energy consumed by the two comparator shows that the Dynamic Bias requires less energy due to the existence of C_p and C_{tail} .

The relative CLK-Q delay of the Elzakker's comparator is much smaller than the dynamic-bias comparator especially when V_{cm} is equal to 0.6 V.

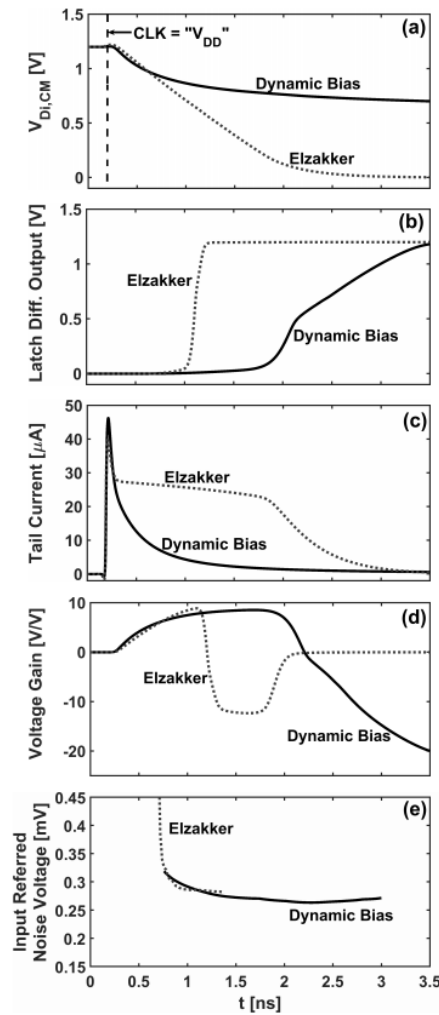


Figure 4. (a) common-mode voltage of output, (b) latch differential output, (c) the profile of the tail current, (d) pre-amplifier differential voltage enlargement, (e) input referred noise voltage by the pre-amplifier

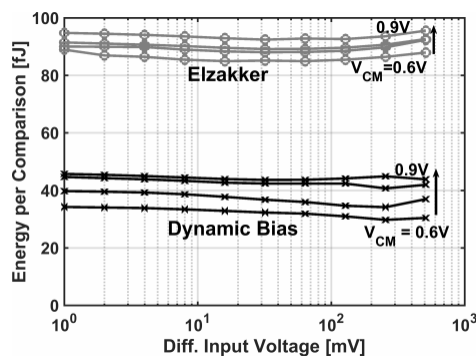


Figure 5. Power efficiency of the two different comparators

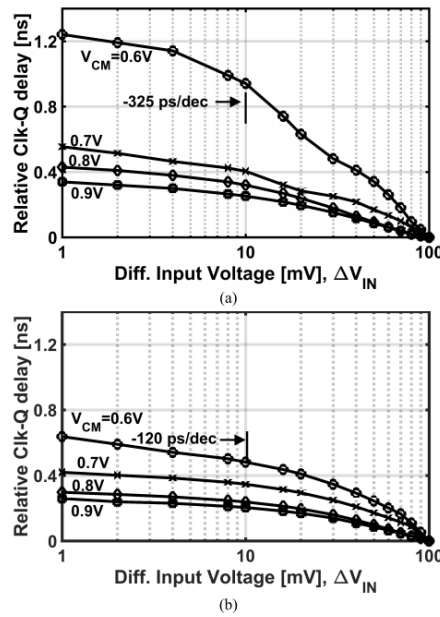


Figure 6. Relative CLK-Q delay of the dynamic-bias comparator

However due to the latch output which is shown in the Figure. 4(b) the Elzaker's output changed directly from 0 to 1 at around 2ns and the Dynamic Bias grow slowly and reached the 1 output at 3.5ns.

That means the dynamic-bias comparator has a higher delay than the Elzaker's comparator. Also the rapid output logic changing indicates that it has a better power efficiency.

So, the dynamic-bias comparator has a better output efficiency when it comes to a situation which need a lower power consuming comparator but it also has a longer delay.

The ideal working range of the dynamic bias maybe when the V_{cm} equal to 0.9V.

According to the line chart Figure 5. though the power efficiency of the dynamic-bias rise with a beginning at 35 fJ to 45 fJ when the V_{cm} rise from 0.6V-0.9V the relative CLK-Q delay decreases from 1.2ns to 0.4ns.

So, the optimum value of the Dynamic bias comparator lies at around 0.8V-0.9V.

When working with an input Voltage of 0V-100 V which is simulated in Figure 6., the energy consumption only rises 10%, the relative delay decreases over 60%.

3. The Quad high-speed comparator

The Quad Figure 7. is consisted of two asymmetric differential parts and give out two output currents. The major output is a liner current and the square-law current is the accessory output.

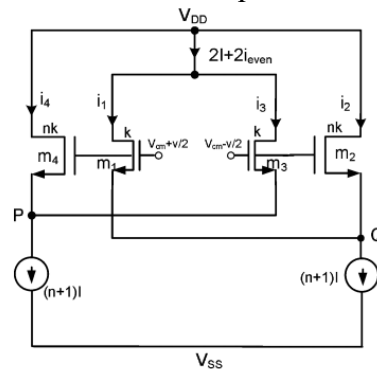


Figure 7. Quad differential skewed pair currents

The four currents i_1, i_2, i_3, i_4 are given as

$$i_1 = I + \gamma kv^2 + 2av\sqrt{k(1 - \beta kv^2)} \quad (4)$$

$$i_2 = nI - \gamma kv^2 - 2\alpha v \sqrt{k(1 - \beta kv^2)} \tag{5}$$

$$i_3 = I + \gamma kv^2 - 2\alpha v \sqrt{k(1 - \beta kv^2)} \tag{6}$$

$$i_4 = nI - \gamma kv^2 + 2\alpha v \sqrt{k(1 - \beta kv^2)} \tag{7}$$

The even function and the odd function [6] of the output are also given as

$$i_4 - i_2 = 2i_{odd} = 4\alpha v \sqrt{k(1 - \beta kv^2)} \tag{8}$$

$$i_1 + i_3 = 2i_{even}(total) = 2I + 2\gamma kv^2 \tag{9}$$

The parameters α β and γ are only determined by the skew factor n given as

$$\alpha = \frac{n}{n+1}; \quad \beta = \frac{n}{(n+1)^2}; \quad \gamma = \frac{n(n-1)}{(n+1)^2}; \tag{10}$$

All of these factors decrease with the increase of n .

By defining the normalized currents $\frac{I_i}{I}$ by y_i and the normalized voltage $\frac{v}{V_{on}}$ by x_i , we can get

a functional relationship between y_i and x_i .

The definition of y_i is given as:

$$y_1 = 1 + i_{even} + i_{odd} = 1 + \gamma x^2 + 2\alpha x \sqrt{1 - \beta x^2} \tag{11}$$

$$y_2 = n - i_{even} - i_{odd} = n - \gamma x^2 - 2\alpha x \sqrt{1 - \beta x^2} \tag{12}$$

$$y_3 = 1 + i_{even} - i_{odd} = 1 + \gamma x^2 - 2\alpha x \sqrt{1 - \beta x^2} \tag{13}$$

$$y_4 = n - i_{even} + i_{odd} = n - \gamma x^2 + 2\alpha x \sqrt{1 - \beta x^2} \tag{14}$$

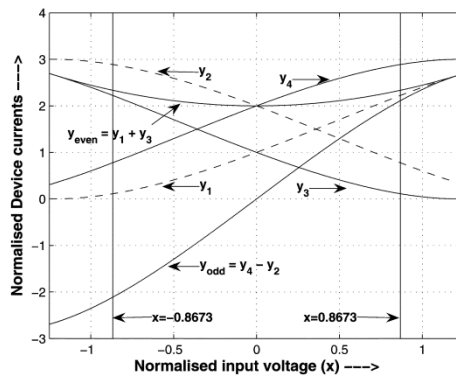


Figure 8. Normalized Device currents in four transistors as normalized input voltage function for $n = 2$

From this line chart Figure 8. we can see that with the normalized voltage changing from -1.25V to 1.25V the y_1 and y_4 continue to grow from 0 to 3 while the y_2 and y_3 decrease from 3 to 0.

The y_{odd} which is equal to $y_4 - y_2$ grows from -2.7 to 2.7 and the y_{even} equal to $y_1 + y_3$ decrease from 2.7 to 2 when x equal to 0 and then rise back to 2.7.

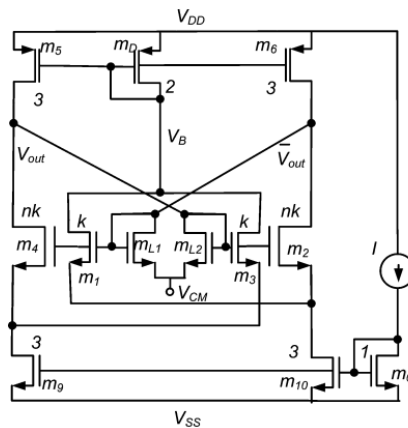


Figure 9. Latch based Quad circuit

Using the Quad, this circuit Figure 9. has two stable states. In one of the two states, the differential voltage $V = V_{out} - \overline{V}_{out}$.

The v can be calculated as

$$\frac{v}{V_{on}} = \pm 2(n + 1) \sqrt{\frac{3n^2 - 2n - 1}{15n^4 + 28n^3 - 22n^2 - 20n - 1}} \quad (15)$$

Bias Current I (μ A)	Single-ended output Rise Time t_r (ns)	Single-ended output Fall Time t_f (ns)	Differential output Volts $V_{L1} - V_{L2}$
10	3.5 (0.81)	2.8 (0.35)	0.26
15	2.2 (0.57)	1.7 (0.34)	0.32
20	1.5 (0.49)	1.2 (0.33)	0.46
25	1.2 (0.44)	0.41 (0.31)	0.54

Figure 10. fall time and rise time comparing with bias current

This is quite useful because when calculating the different Output Voltage in the stable stage because it is only determined by the skew factor n .

The table Figure. 10 given also shows the transition time of different bias current working in the stable states [7]. It shows that with the increase of the bias current, the rise time and the fall time of the Single-ended output both decrease but the different output Voltage rises.

4. The low-power dynamic comparator

The original double-tail comparator in Figure 11. is consisted of a pre-amplifier part and a latch part. Since the C_p cannot be discharged completely to V_{DD} so the pre-amplifier's energy consumption can take 70%-80% of the whole energy [9].

This paper announced a new kind of comparator with a proved pre-amplifier. Instead of using two capacitance a cross-coupled device and a regenerative latch are added to the pre-amplifier part.

The amplification phase of the modified pre-amplifier has two different subphase. The equivalent circuit is shown in Figure 12..

When the M1 and M2 are in conductive region while M21 and M22 working in liner region, voltage of node N1 and P1 will start decreasing. The decreasing rate of N1 will be faster than P1 so the M22 will turn off eventually.

This will force the intN node to discharge the final voltage of intN and intP will be V_{d1} and V_{d2} . Since both of their voltage are lower than V_{DD} , the power efficiency of every comparison can be reduced [10].

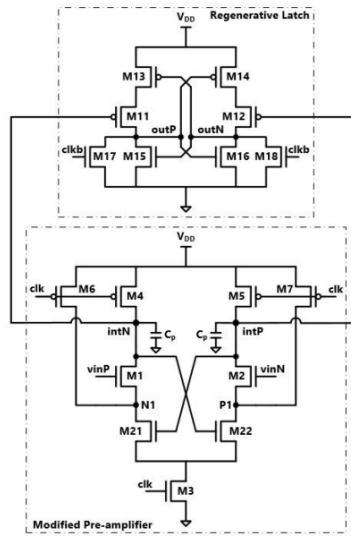


Figure 11. Original double-tail comparator

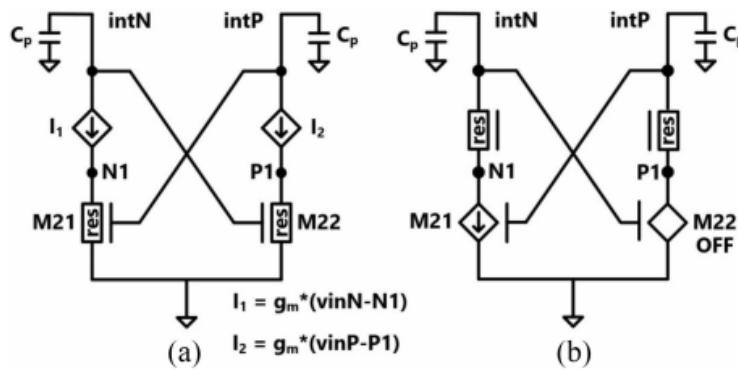


Figure 12. pre-amplifier equivalent circuit in two subphases

The referred noise in Figure 13. of the low-power circuit is slightly higher than the standard one meanwhile the delay of the low-power comparator is over twice as much of the standard one.

With the increasing of the input voltage, the delay of both kinds of comparator are decreasing and are shown in Figure 14.

However, the comparator power of the proposed circuit in Figure 15. is about 30% lower than the standard one the power consumption also increased when the input voltage is over 10mv.

As a conclusion the proposed comparator has a reduction of about 30% of the energy at a cost of huge comparator delay.

The ideal working range of the low-power dynamic comparator may be at 100mv of the input voltage because the delay has dropped about 50% than 1mv input but the power just increased for about 10%.

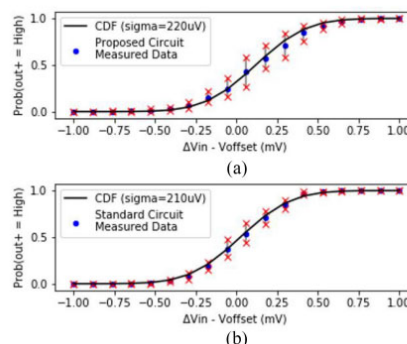


Figure 13. measured input referred noise for (a) low-power dynamic comparator and (b) standard double-tail latch type comparator

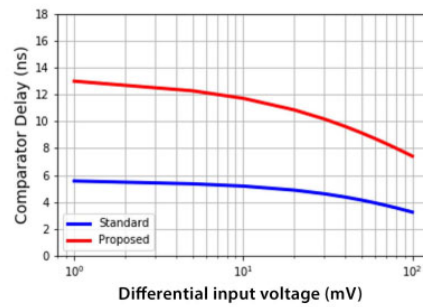


Figure 14. comparator delay of differential input voltage of the Standard and low-power comparator

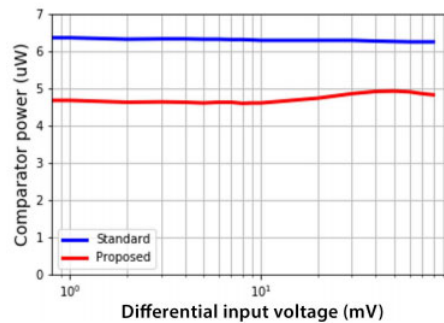


Figure 15. comparator power of the standard and the low-power dynamic comparator

5. Conclusion

In conclusion the Quad high-speed comparator and the low-power dynamic comparator have made some changes to the conventional comparator. The Quad comparator has a smaller delay and the dynamic comparator has a lower power efficiency but has the weak point of a higher delay.

The Dynamic-bias comparator announces a new circuit making the improvement of the voltage gain more available. What's more the energy consumption and voltage inferred noise are both smaller while the delay of it become higher.

So, the future working may lie in how to find the balance point to get a comparator with all these advantages.

Acknowledgement

The author would like to express gratefully acknowledgement to S. M. Wang and Y. Z. Zhu for their financial and technical supports.

References

- [1] Schinkel D., Mensink E., Klumperink E., van Tuijl E., and Nauta B., "A double-tail latch-type voltage sense amplifier with 18ps setup+holdtime," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, CA, USA, Feb. 2007, pp. 314–605.
- [2] Gamad R. S., Meena Panchore, "Low Power and Highspeed CMOS Comparator Design Using 0.18 μ m Technology," International Journal of Electronic Engineering Research, vol. 2, pp. 71-77, 2010.
- [3] Current K. W., "Voltage-mode CMOS quaternary latch circuit", Electronics Letters, v 30, n 23, p1928-9, 10 Nov 1994.
- [4] Wong K. L. J. and Yang C. K. K., "Offset compensation in comparators with minimum input-referred supply noise," IEEE Journal of Solid-State Circuits, vol. 39, no. 5, pp. 837–840, 2004.
- [5] Figueiredo, Pedro M., and Joao C. Vital. "Kickback noise reduction techniques for CMOS latched comparators." Circuits and Systems II: Express Briefs, IEEE Transactions on 53.7 (2006): 541-545.

- [6] Al-Rawi G. A., "A new offset measurement and cancellation technique for dynamic latches," in Proc. IEEE Int. Symp. Circuits Syst., May 2002, vol. V, pp. 149–152.
- [7] Dingwall A. G. F., "Monolithic expandable 6 bit 20 MHz CMOS/SOS A/D converter," IEEE J. Solid-State Circuits, vol. 14, pp. 926–932, Dec. 1979.
- [8] Al-Rawi G. A., "A new offset measurement and cancellation technique for dynamic latches," in Proc. IEEE Int. Symp. Circuits Syst., May 2002, vol. V, pp. 149–152.
- [9] Sepke T., Holloway P., Sodini C. G., and Lee H. S., "Noise analysis for comparator-based circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 3, pp. 541–553, Mar. 2009.
- [10] Lin J. Y. and Hsieh C. C., "A 0.3 V 10-bit 1.17 f SAR ADC with merge and split switching in 90 nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 1, pp. 70–79, Jan. 2015.