Research on A 93.56 FO4(1V), 141.36 Eu(1V) 4-bit Absolute-Value Detector Based on CMOS transistor

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Abstract: In recent years, with the continuous upgrading of the chip manufacturing industry, the requirements of circuit design are not only to complete more and more complex signal conditioning tasks, but also to put forward higher requirements for performance delay and other aspects. This paper designs a 4-bit Absolute-Value Detector circuit and uses half-adder to realize signal conversion. In my circuits, when V dd is 1v, the critical path delay is 63.04 FO4(1V), and the total energy is 186.97 EU(1V). This also provides a solution for circuits that pursue low power consumption and low latency.

Keywords: Absolute-Value detector. CMOS transistor. Critical path delay. Energy.

1. Introduction

In 21st century, integrated circuits have become more and more important, which are widely used in our life and work, and still a core technology in the field of computer hardware. Integrated circuits not only have a wide range of social applications, but also has the advantages of high added valued and high technology content. As an emerging industry that has been rising and evolving, electronic integrated circuits are still a blue ocean in many different aspects of design and research. Especially in my country, until now, we still rely on importing another countries' technology in order to product the high-end chips. This is incompatible with the rapid development of my country's automobile industry, computer industry, network media and other high-tech industries [1]. The people of our country need a lot of high-end chips to help the high-tech industry continue developing rapidly. Unfortunately, due to the outbreak of the epidemic, the surge in demand for chips caused by the decryption of virtual currency, the turbulence and chaos in the international situation, and the outbreak of energy problems, without any doubt, the import and export of chips has been affected. In these years, many high-tech industries are developing rapidly in my country, but integrated circuit technology has not developed as fast as we imagined. Therefore, the adaptation requirements gradually exceed the performance requirements. But this does not become a reason for the integrated circuit industry to not make progress. On the contrary, the integrated circuit industry, which is aware of many problems, has become more diligent to make technological breakthroughs and seek possible opportunities to change the relatively slow development status quo.

In some information technology and computer industries, most have very high specifications for power consumption and circuit delay. Therefore, a relatively low-power, low-latency absolute value detector circuit is designed in this paper, which consists of CMOS circuits without using overly complex materials, while being adequately designed. The absolute value detector is an important component, especially in the field of MCU and FPGA [2]. Determining whether a signal is too large is an important process in designing chip pins.

2. Design 4-bit Absolute-Value Detector

2.1 Design summary

The table1 shows the Final delay and Total energy. Circuit Topology: Combination of half adders. Circuit Style: PTL for 2:1 MUX static CMOS for others.

Table 1 The main data of my circuit

V_{dd}	Critical path delay	Total energy
1V	$t_{p_IN\rightarrow OUT}$ =63.04 $FO4_{(1V)}$	$t_{p_IN\rightarrow OUT}$ =186.97 $E_{U(1V)}$
0.775V	$t_{p_IN\rightarrow OUT}$ =93.56 $FO4_{(1V)}$	$t_{p_IN\rightarrow OUT}$ =112.29 $E_{U(1V)}$

This is our relevant data conclusion and equipment choice, including the critical path Delay and total Energy. When V_{dd} is 1v, the critical path delay is 63.04 FO4(1V), and the total energy is 186.97 EU(1V). When V dd is 0.75v, the critical path delay is 93.56 FO4(1V), and the total energy is 112.29 EU(1V). It is not difficult to find that when the delay is larger, the energy is smaller, so we will find a balance in it.

2.2 The determination of the number of network layers

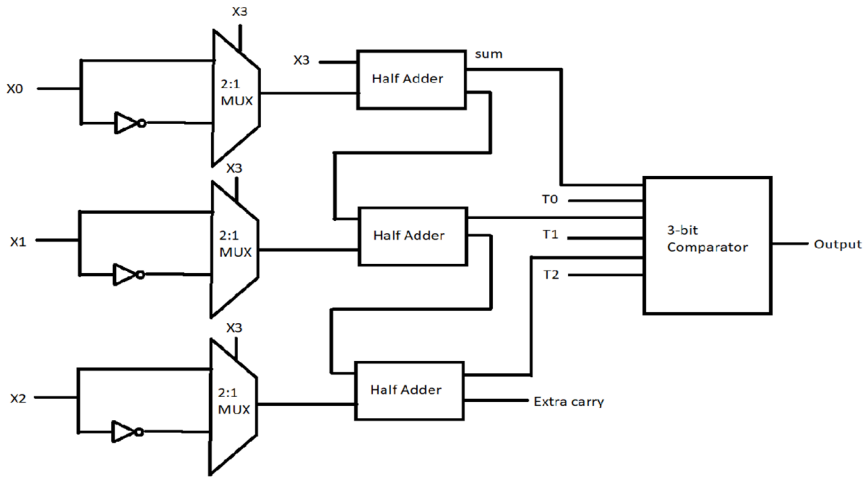


Figure 1. Schematic diagram of overall circuit structure

The network structure is shown in Figure 1. And, we use less logic gates in adder process, but more in circuit. Ripple-carry adder were considered, it is a combination of 2 half adders, which doubles the needed logic gates. The function of 2:1 MUX is to determine whether the 4-bit value is positive or not, and output the original or flipped absolute value according to sign bit. The combination of 3 half adders is to add 1 to the value from MUX if the original value is negative, so the 2's complement can be finished.

The comparator is from instruction, and it will compare the 3-bit absolute value with 3-bit threshold value. If the absolute value is larger than threshold, the output will be 1, and vice versa.

I chose not the All-Adder that people usually use, [3] but the Half-adder. And after thinking about it, I thought: using the Half-adder is a good design solution. First of all, because two Half-adders are one All-adder, using Half-adder will make the design more flexible, because I only need the function of Half-adder to generate carry, but All-adder has one more input for receiving carry than half adder. So, the All-adder has to consider the carry from the low order every time, and the Half-adder does not need to consider it, just add the two binary numbers directly; second, because I think that although more gates may be generated, the final energy and delay may be relatively smaller [4].

2.3 Critical Path Analysis

Figure 2 is the critical path I drew, which is the highlighted part in the above figure. I calculate the delay according to this line.

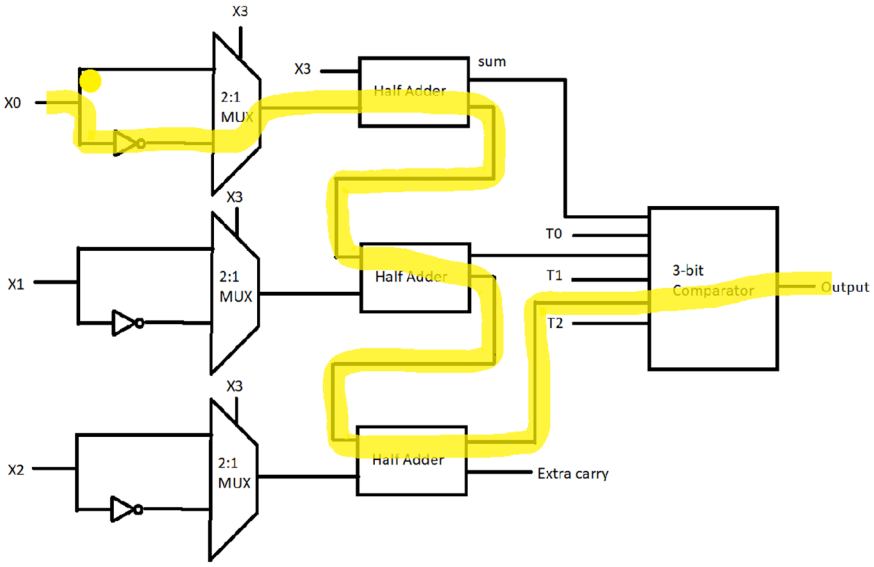


Figure 2. The location of Critical Path

Designing a circuit diagram doesn't mean everything is done, on the contrary, it should be the beginning. Finding the Critical Path is a key step in our calculation of Delay and Energy [5].

$$T_{critical} = \mathrm{T}_{mux} + 3 * T_{halfadders} + T_{comp} \quad (1)$$

$$block\ diagram\ of\ design\ /\ critcal path\ delay\ equation \quad (2)$$

If the wrong Critical Path is found, it will cause the entire calculation to fail, which is what we try to avoid in this project. The method we use to find the Critical Path is to enumerate and try to find the longest path of the link element as much as possible, that is the Critical Path we need to find.

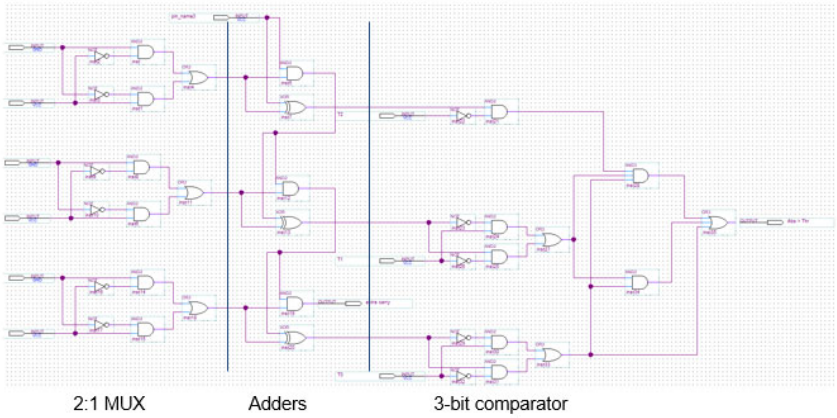


Figure 3. the whole circuit in the simulation software Quartus II.

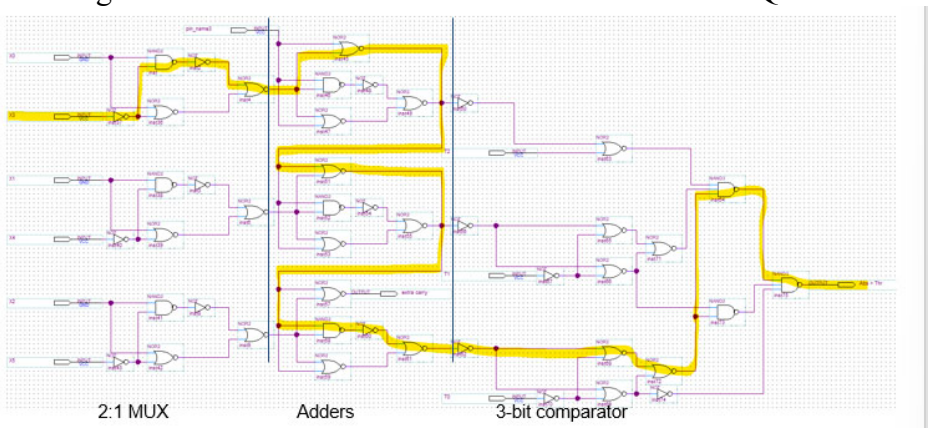


Figure 4. Critical path in the simulation software Quartus II.

Then, in figure 3 and 4, we used the Quartus II software to simulate the composition of the circuit, and verified the feasibility and correctness of its path. The simulation proved that the Critical Path

we had drawn by freehand was accurate, and further simulation verification by the computer also laid the foundation for our subsequent calculations [6].

$$\text{Delay} = \sum (G_i * B_i * H_i + P_i) \tag{3}$$

$$\text{Delay} \propto V_{dd} / (V_{dd} - V_t)^2 \tag{4}$$

$$\text{Energy} = CL * V_{dd}^{\ 2} \tag{5}$$

These three formulas let us understand how to calculate delay and energy, and understand that Logical Effort, Electrical Effort, Branching Effort and other factors are related to the delay and energy of each path.

Therefore, through the above three formulas, we can clearly realize that if we require the Delay and Energy of Critical Path, we need to pay attention to what values. These three formulas will also be key takeaways for our next content.

3. The energy and delay of my circuit

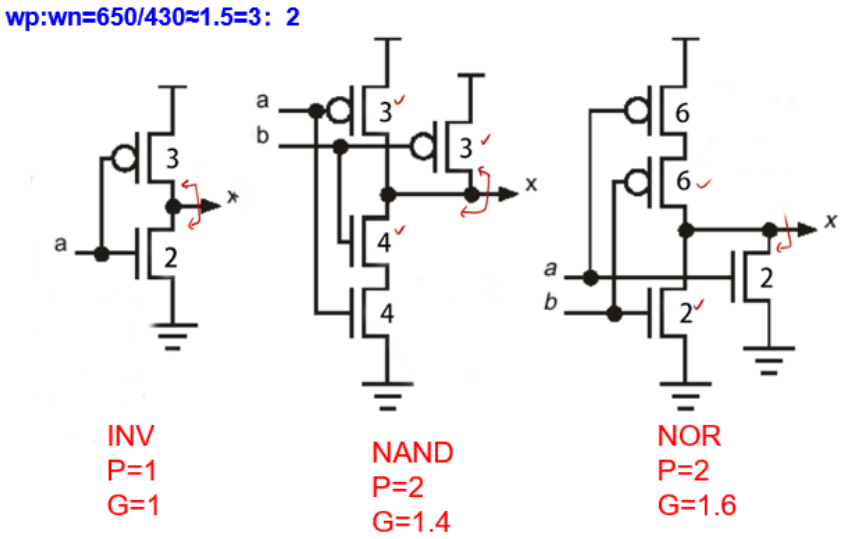


Figure 5. MOSFET structure and size

As shown in Figure5, these basic experimental data are provided by the professor of the project team, and we will process on the basis of this data, and finally calculate the Delay and Energy.

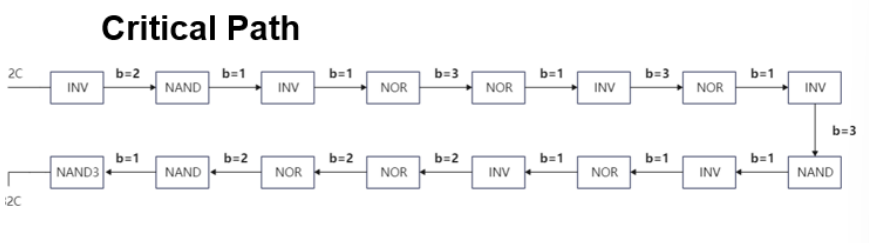


Figure 6. Critical path diagram

Figure6 is the path diagram of Critical Path in our project. Drawing a diagram can make our calculations more intuitive.

Logical Effort: G =82.87
Electrical effort: H = C_{out} / C_{in} = 16
Branching Effort: B = 432
Path Effort: PE = B*G*H =572769.97
Best stage Effort: f =$PE^{1/16}$ = $(572769.97)^{1/16}$ =2.29 (6)
Delay: D = Pi + Gi * Hi = 16 * 2.29 + 26 = 63.04
Energy = α * Ci * V_{dd} * V_{dd} = 186.97

Some of the above formulas and Tables2 below are our main basis for the calculation process [7]. Because of the good preparation in the early stage, the difficulty of calculation has been reduced, and we have reached the final conclusion through the joint calculation of the analog circuit and Excel.

Table 2. Calculation data of the critical path delay and energy

	Type	G	B	H	P	Cin	Delay	Size	Energy
MUX	INV	1	2	2.29	1	10.01	3.29	2	2
	NAND	1.4	1	1.64	2	11.47	4.29	2.29	2.29
	INV	1	1	2.29	1	18.76	3.29	3.75	3.75
	NOR	1.6	3	1.43	2	42.95	4.29	8.59	8.59
HF1	NOR	1.6	1	1.43	2	20.49	4.29	4.1	4.1
HF2	INV	1	3	2.29	1	29.33	3.29	5.87	5.87
	NOR	1.6	1	1.43	2	22.39	4.29	4.48	4.48
HF3	INV	1	3	2.29	1	32.04	3.29	6.41	6.41
COM	NAND	1.4	1	1.64	2	24.46	4.29	4.89	4.89
	INV	1	1	2.29	1	40.01	3.29	8	8
	NOR	1.6	1	1.43	2	91.61	4.29	18.32	18.32
	INV	1	2	2.29	1	131.12	3.29	26.22	26.22
	NOR	1.6	2	1.43	2	150.13	4.29	30.03	30.03
	NOR	1.6	2	1.43	2	107.44	4.29	21.49	21.49
	NAND	1.4	1	1.64	2	76.89	4.29	15.38	15.38
	NAND3	1.8	1	1.27	2.4	125.76	4.69	25.15	25.15
		82.87	432	16	26	160	63.04	32	186.97

4. Result and some extra calculation

After Gate Sizing and Power Scaling, we obtained an Absolute Value Detector with an energy consumption of 93.56 FO4(1V) and a total delay of 141.36 FO4(1V).

Our Gate Sizing strategy takes into account various scenarios and compares them. Critical Path's small latency versus energy consumption for different gate sizing strategies is shown in the following table.

Table 3. Different gate sizing results from V_{dd} of different sizes

V dd %	10%	25%	40%
V dd	0.939	0.866	0.808
Gate sizing%	40%	25%	10%
	116.88	116.51	108.86

When we only change the Gate Sizing. It can be seen from the above table that the smaller the V dd, the less energy the system consumes. In the circuit, we can provide energy smaller than the gate size to achieve the purpose of reducing energy consumption [8].

If VDD scaling is the only variable that changes (1.5x), the V_{dd} and energy be like:

$$\begin{aligned} &\text{Delay} \propto Vdd/(Vdd-Vt)^2 \\ &Default: Vdd = 1V, Vt = 0.2V \\ &1.5*delay, Vt = 0.2V \\ &Final_Vdd = 0.775V \\ &Energy = 112.29E_{u(1V)} \end{aligned} \tag{7}$$

When we use another method – V_{dd} scaling to make the delay 1.5 times, we can also make the energy smaller.

The use of these two methods may allow us to obtain smaller energy in a limited system, which helps us better adjust the overall circuit system. How to balance performance and power consumption needs to be chosen according to the specific application environment.

Switching the operating mode of the device by scaling the supply voltage is a commonly used modern energy-saving technique [9].

5. Conclusion and Improvement

We discuss and design the sizing on non-critical paths in order to reduce energy consumption. Because when we calculate the delay of its entire circuit, we only calculate the delay of its critical paths. The delay of non-critical path is not so important. So, without affecting the delay of critical paths (in another word, we are going to ensure that Delay of non-critical paths should be not greater than critical), we Reduce devices' size on unimportant path is OK. If we consider using alternatives, we may change it into carry look ahead adder. We carry one bit by one bit when we change before, and this alternative will give us a simultaneous carry. Using the carry look ahead adder may reduce the delay a lot, but it may make the circuit more complicated, and the total number of MOS tubes and other components used will be much more [10].

Here's some important features of our design. Our design generates minimum delay by gate sizing, and we used half adders only for the adder section. Also, for our design, we only used NOR, NAND and NOT gates, which means that we convert the original AND, OR and XOR gates to those gates that can be implemented by static CMOS directly.

And here are some things that we would do different. First is that we can change the topology for getting shorter critical path. We notice that the Delay and Energy are lower in the presentation of other groups, this may be caused by the topology difference. We can try carry look-ahead adders for shorter critical path, and we may get a better value. Second, we can find the best combination of gate sizing and VDD scaling. Different contribution of VDD scaling and gate sizing to delay can vary, so a good combination of VDD and gate sizing can lead to the best delay and energy.

We can also do gate sizing partially instead of globally. And we can try MATLAB instead of Excel Solver in optimization part. When we were doing the optimization section with Excel Solver, there were some glitches and we either cannot get results, or we got strange results. MATLAB may be able to solve those problems that we met.

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