

Contrastive Analysis of Low Power Low Noise Amplifiers Used in Three Different Applications

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Abstract. In this paper, three kinds of low power low noise amplifier used respectively in biomedical applications, RF receivers and ultra-wideband (UWB) applications are compared and analyzed. Their prime simulation results are showed as well. Since, their application fields are different, the parameter characteristics of signals as well as their circuit structures and used topologies are various. In order to analyze them more clearly and distinctly, on one hand, the parameter characteristics of signals, which is vital factor when decide circuit structures and used topologies, are compared. On the other hand, their circuit structures and used topologies are introduced and qualitatively compared while their performance, such as band width, gain, noise, power, supply voltage, are quantitatively compared. Folded-cascode topology, current reused topology, inverter-based shunt feedback topology, and parallel summation structure are analysed in this paper.

Keywords: RF receivers, ultra-wideband, Folded-cascode topology

1. Introduction

In recent years, low power, low noise amplifiers are used more and more frequently in many fields. Their performance of low power consumption and low noise has drawn the attention of researchers looking for advanced integrated circuit structure to improve them. There are many ways to design a power amplifier integrated circuit in terms of their different application fields. Each integrated circuit configuration has different operation and output characteristics. As a result, power amplifier can be used in many fields, such as industrial engineering, wireless communication, consumer electronics and so on. In order to express the full range of their low power consumption and low noise ability, researcher proposed a variety of amplifiers with different circuit structure and topology such as logarithmic low power low noise amplifiers, transconductance low power low noise amplifier, folded-cascode low power low noise amplifier.

In audio field, Tang F. et al. proposed a class-AB power amplifier used in audio applications with low power consumption which was created using a 55nm CMOS technology and has dynamic transconductance adjustment [1]. Torres J. et al. proposed a high-PSRR audio amplifier with very low power consumption [2].

In radio frequency filed, Ananda M and Kalpana A B proposed a design of low noise amplifier which is used for RF receiver and can achieve high gain [3]. J.k.kasthuri Bha and P.Aruna Priya used FinFET to design a cascode amplifier with low noise to realize power optimization of RF transceiver [4].

In biomedical filed, Xuan Liu and Yali Su proposed a kind of low noise preamplifier with very low power consumption which can be applied to acquire portable signals [5]. Chaya N. et al. proposed an operational transconductance amplifier with ultra low power consumption and low noise that could be applied to front-end applications related to biomedical field [6].

This paper looks at low power low noise amplifier applied to three application fields including biomedical applications, RF receivers and ultra wideband (UWB) application. In this paper, three kinds of amplifiers with low power consumption and low noise used respectively in the mentioned three application fields are introduced and analyzed by comparison. Their various applications result in their various circuit structures and topologies, therefore, have further affect their performance such as band width, gain, noise, power, supply voltage.

Section 2-4 briefly introduce the design of forementioned three low power low noise amplifiers. Next, Section 5 compared their performance and reasons that result in their difference are analyzed in this section as well. Finally, Section 6 is the conclusion of this paper.

2. Low power, low noise amplifier used for biomedical applications

2.1 Application background

In biomedical field, low power integrated circuits and systems are focused for its ability to realize function with relative lower power consumption, which plays an important role in saving energy. Though the input signal can have high dynamic range, logarithmic amplifiers can convert them into output signal which only has a defined range. As a result, they are frequently utilized in biomedical applications.

2.2 Circuit structure

A kind of front-end logarithmic amplifier with ultra low power consumption and wide dynamic range was proposed in [7]. Parallel-amplification structure as well as parallel-summation structure are applied to it and the corresponding circuit structure are shown in Figure 1. It takes into account four stages and the gains are 1, 9, 90 and 900, which correspond to dB values of 0 dB, 9 dB, 39 dB, and 59 dB, respectively. As shown in Figure 2, a kind of fully differential OTA using current-reuse technique is utilized in order to increase the value of g_m/I_D and achieve well common mode rejection ratio, thus,

implement each gain amplifier.

Noise is also a key factor to be considered when optimizing amplifiers' performance. In this design [7], in order to cancel the DC offset voltage, in other words, to reduce low frequency flicker noise and eliminate EDO, a high-pass cut-off frequency is required. Therefore, ultra-low frequency signal components have been suppressed by using RC filter. A particular class of pseudo-resistors shown in Figure 3 has been used in RC filter to avoid needing huge on-chip capacitors.

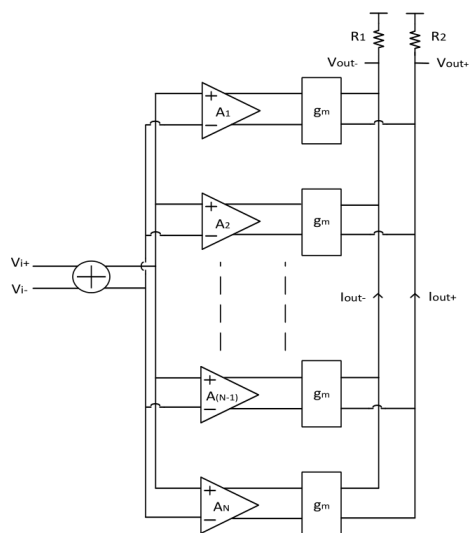


Figure 1. Schematic diagram of the logarithmic amplifier with fully differential input [7].

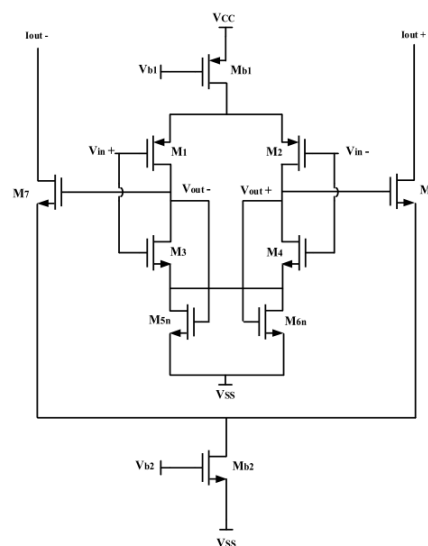


Figure 2. Schematic diagram of the logarithmic amplifier with parallel paths [7].

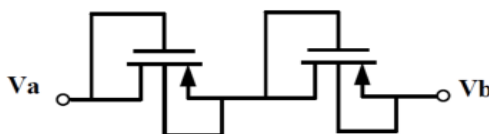


Figure 3. Pseudo-resistor architecture [7].

2.3 Simulation results

This logarithmic amplifier dissipates just 3.36W since the bulk of transistors operate in subthreshold region, according to the simulation results shown in [7]. According to Figure 4, which plots the frequency response, the voltage gain in the roughly 0.2Hz to 10kHz frequency range is 62dB. In addition, from the simulation results the value of CMRR, PSRR+ and PSRR- of this amplifier can be known, which are 192dB, 183dB and 214dB respectively. It can therefore effectively exclude unwished sounds and common mode signals brought on by the power supply. The input-output characteristics curve shows linearity in the range of $10\mu\text{V}$ to 160mV, according to Figure 5. Since the output voltage ranges from 17 to 560 mV and the input dynamic range is 84 dB, the input signal is compressed to produce a narrower output with dynamic range of 32dB.

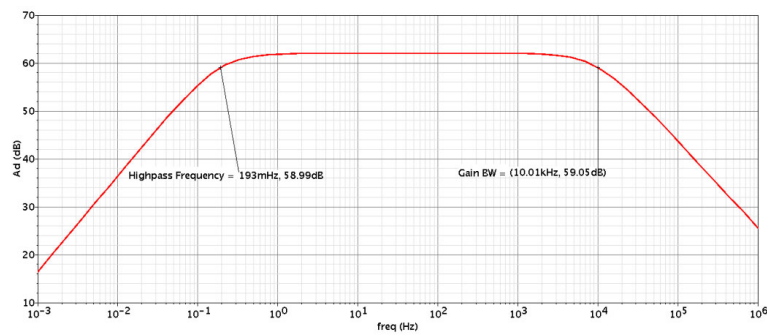


Figure 4. Frequency response [7].

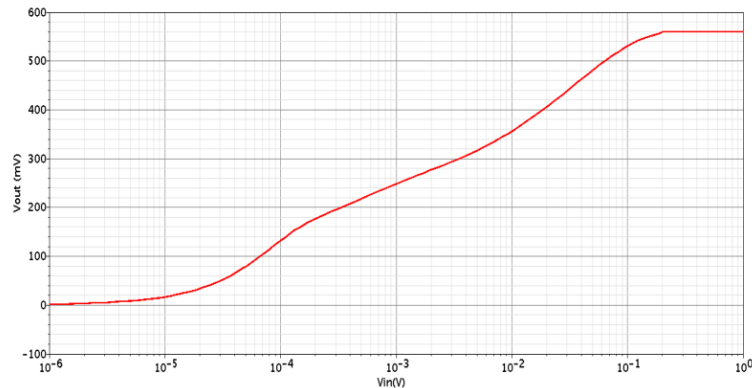


Figure 5. Transfer function [7].

The RMS input referred noise is increased and has a value of $4.2 \mu\text{V}$ after using the RC filter while integrating from 0.1-4kHz. The power spectral density of it is shown in Figure 6.

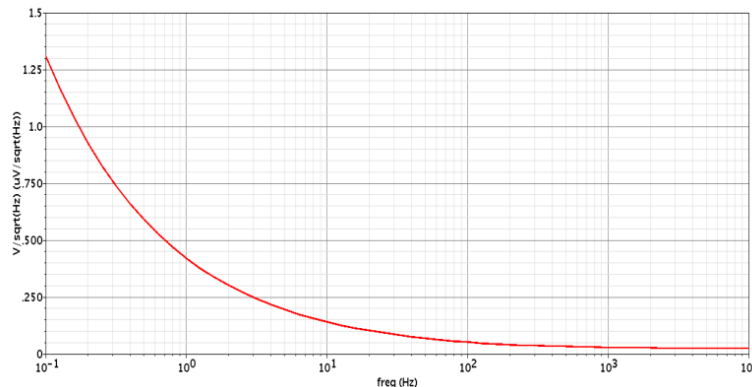


Figure 6. Spectrum of the input referred noise [7].

3. Low power, low noise amplifier used for RF receivers

3.1 Application background

In radio frequency front-end (RFFE) field, most wireless communication applications rely heavily on radio-frequency integrated circuit. Achieving the desired performance with the least amount of power usage is especially important. Hence, there are lots of topologies, for example, current-reuse gm-boosting LNA and inverter-based LNA, that have been proposed and created with the intention of giving RF signals enough gain while using very little power.

3.2 Circuit structure

A kind of LNA with ultra-low power consumption which is used for RF receivers and operates at 900 MHz, is designed in [8]. It is based on the inverter-based shunt feedback LNA topology since this topology is suitable for ULP applications. As for this circuit, the chosen topology is implemented in two stages efficiently. The components of input and output matching networks are similar, including an inductor and two capacitors. With the appropriate inter-stage matching, the inverter-based LNAs are sequentially cascaded. Table 1 lists the component values for the circuit. Figure 7 shows the LNA circuit schematic as well as the input and output matching networks.

Table 1. Circuit component description [8].

Component	Value
C_1	710fF, $Q=797.5$
L_{in}	37.074nH, $Q=8.67$
C_2	1.291pF, $Q=897.6$
C_3	1.035pF, $Q=961$
R_{bias} and R_F	60K Ω
N_1 and N_2	28um/60nm
P_1 and P_2	80um/50nm
C_4	1.211pF, $Q=693.5$
C_5	517.8fF, $Q=961$
C_6	3.1pF, $Q=961$
C_7	704fF, $Q=809$
L_{out}	32.96nH, $Q=11.21$

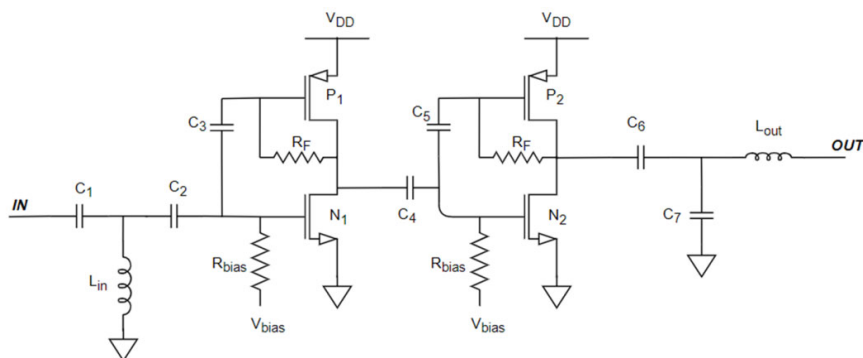


Figure 7. Proposed LNA circuit schematic [8].

3.3 Simulation results

As shown in the results of pre-layout simulation [8], the peak gain appeared when the operating frequency is 900MHz. With 1 dB bandwidth of 115 MHz, the value of the peak gain is 12.09dB. Around 114.2 W of overall power are consumed, which is slightly above the limit (100 μ W), according to DC simulation result. Throughout the whole DC to 10 GHz frequency range, the LNA is unconditionally-stable. In order to analyse stability, $B1f$ and Kf are the parameters taken into account in the simulation of s-parameter.

The post-layout simulation shows the result that the proposed LNA in [8] was able to attain a gain of 10.2 dB at 900 MHz. Signal reflections at both ends are minimized because of input and output matching networks. The value of the overall power consumption is very low, which is just about 112.9 μ W according to the results of post-layout DC simulation. The proposed LNA operates infallibly stably in the frequency range of DC to 10 GHz. Figure 8 shows the results of both the pre-layout simulation and post-layout simulation with comparison plots while Figure 9 shows the stability plots.

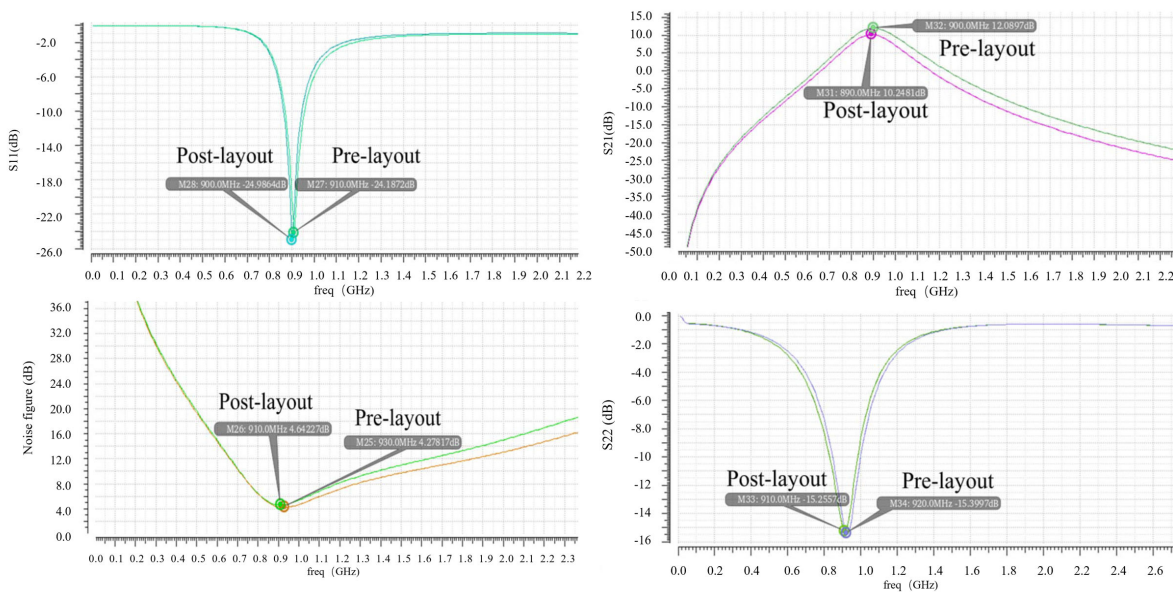


Figure 8. Comparison plot of performance in the pre-layout and post-layout simulation [8].

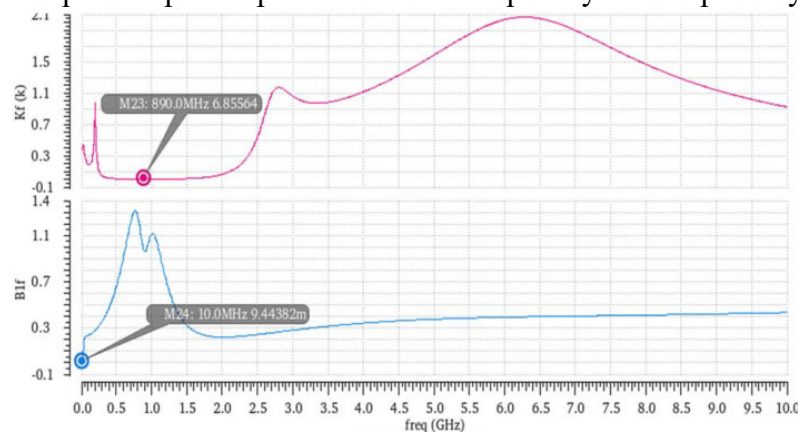


Figure 9. Simulation plot of Kf and $B1f$ [8].

4. Low power, low noise amplifier used for UWB applications

4.1 Application background

In ultra wideband (UWB) field, it is crucial to reduce power consumption and increase data rate when transmitting data. As a result, LNA with low power consumption is very important in UWB receiver systems in order to attain enough gain and low NF over the required wide frequency range. Other factors like low cost and high integration are further considerations [9]. Hence, there are a number of CMOS LNA topologies for UWB receiver systems, including current-reused technique.

4.2 Circuit structure

There are two categories of current reused techniques. One is made of NMOS and PMOS pairs in a shunt configuration. On one hand, with the same amount of power, this technique enhances effective transconductance all around. On the other hand, because NMOS and PMOS transistors have varying levels of mobility, this technique may also result in linearity issues. Another is the current reused topology which shares the same current source with a two-stage cascade. For the proposed high gain UWB LNA with low power consumption in [9], it uses technology of $0.18\mu\text{m}$ CMOS and has two stages. In the first stage, high-pass filters (HPF) are used in order to satisfy the impedance matching of wide input. In the second stage, the forementioned second category of current reused technique is utilized to meet the requirements of low power consumption as well as sufficient voltage gain.

A detailed schematic is shown in Figure 10. To obtain impedance matching over the entire frequency band, a simple HPF type matching network is utilized in an input stage. One of the key factors of UWB LNA is the flat gain throughout the entire bandwidth. Between the core stage and output buffer, peaking inductor L_{D2} is inserted to extend the 3-dB bandwidth and modify the flat gain at high frequencies.

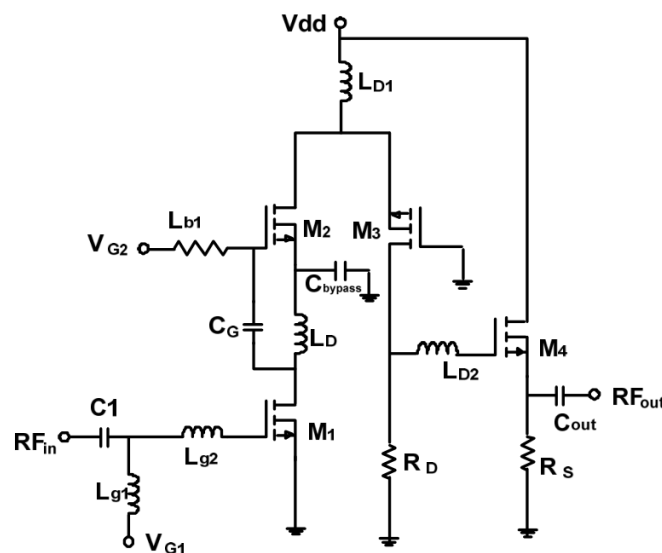


Figure 10. Complete circuit structure [9].

4.3 Simulation results

The designed UWB LNA's simulated S-parameters are shown in Figure 11. The frequency range of 3.1 GHz to 10.6 GHz can be covered with a 10 dB return loss bandwidth. The simulated voltage gain ranges between 17.6 dB and 19.7 dB throughout the whole UWB frequency band. Using the simulated S-parameters, the stability factor has been determined, and over the whole bandwidth, it has a value greater than 1. The intended frequency band's simulated NF varies from 1.8 dB to 2.2 dB. According to Figure 12, P1dB is -15.3 dBm at 6 GHz while IIP3 is -5.31 dBm. The suggested UWB LNA's total power consumption is 4.0 mW while core power consumption is only 2.93 mW.

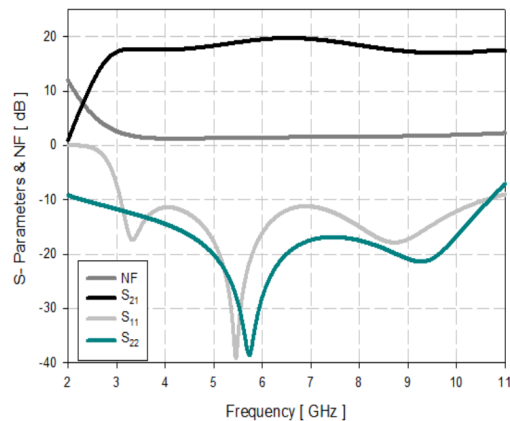


Figure 11. S-Parameter simulation results for the proposed UWB LNA [9].

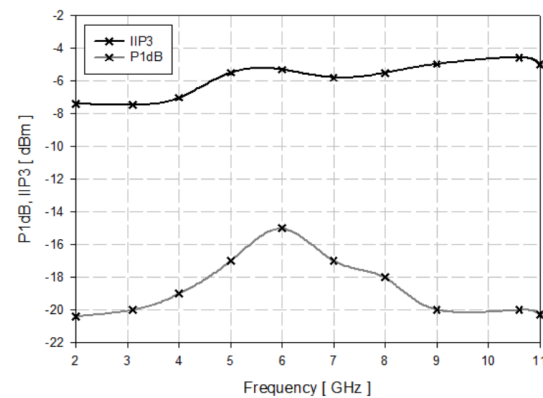


Figure 12. Simulated IIP3 and P1dB of the proposed UWB [9].

5. Comparative analysis of the mentioned three amplifiers

Performance summary and comparison of the aforementioned three low power, low noise amplifiers are showed in Table 2. Their different application fields result in their varied circuit structure and topologies. Therefore, they performance vary greatly.

Table 2. Performance summary and comparison of three amplifiers.

Parameters	[7]	[8]	[9]
	0.18 μ m	0.18 μ m	0.18 μ m
Technology			RF Cmos
Bandwidth	0.19-10k Hz	200 Mhz	3.1-10.6 GHz
Gain(dB)	62	10.2	13.0-19.5
Supply	1.2	0.56	1.0
Voltage(V)			
Noise	NEF: 3.76	NF:4.66dB	NF: 1.8-2.21dB

5.1 Parameter characteristics of signals

The input signals and output signals of amplifiers are varying when used in different applications, thus, all sorts of circuits structures are needed.

For biomedical applications, on one hand, the amplitude and frequency of bio-medical signals can be very weak, for instance, the frequency of EEG signals ranges from 0.1 to 100Hz while the amplitude is from 1 and 160V pp [10], Figure 13 [10]. As for biomedical front-end receivers, they must satisfy all design criteria while consuming relatively little power. Signals from extracellular systems must be amplified because they are so weak without amplification [6]. On the other hand, the voltage of input signals can vary in a very wide range, for instance, the output voltage of the mentioned amplifier [7] ranges from 17 to 560 mV and its input dynamic range is 84 dB, as a result, it narrows the output's dynamic range to 32 dB by compressing the input signal.

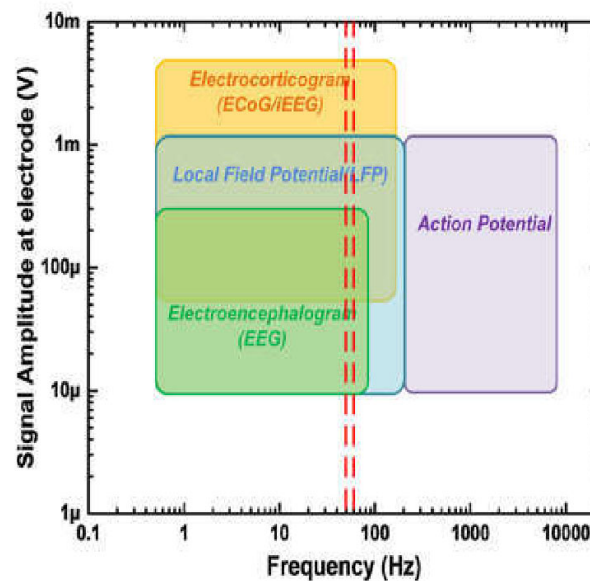


Figure 13. Amplitude and frequency ranges of neural signals [10]

For RF applications, they operate at very high frequency, but radio-frequency amplifier (PA) cannot amplify the signal received by the antenna, while low noise amplifier (LNA) can, for instance, in Radio Frequency Receiver system, the weak signal can be amplified with no noise by LNA amplifies and then be feed as input to Mixer [3]. After amplification, the low noise amplifier can work in frequency of a large range. In the mentioned IF LNA [8], the power consumption is very low when it operates at 900 MHz frequency. Analogously, for ultra wideband (UWB) application, they operates at very high frequency as well. UWB systems are allocated for use of frequency band between 3.1GHz to 10.6GHz. UWB LNA plays an important role in the initial circuit design of UWB receiver since it can amplify weak signals from across the whole UWB band. It is required to have great linearity, low noise, and enough gain to cover the whole UWB spectrum [11].

5.2 Types of amplifiers and used topologies

Among the various types of amplifiers, logarithmic amplifier is a typical one. In the processing of high frequency signals, such as radar or radio receivers, logarithmic amplifiers are frequently utilized. Not only that, logarithmic amplifier is applied to biomedical applications gradually because of their great character. In the mentioned amplifier [7], a type of logarithmic amplifier that used for biomedical applications is introduced. The single stage type and piecewise approximation type constitute the foundation for the realization of logarithmic amplifiers. The latter type mainly concludes two classes: parallel summation and series linear limit. In the implementation of a unity-gain buffer with high-accuracy, the structure of parallel summation is employed rather than the structure of series linear in order to save chip space and reduce power consumption [7]. The aforementioned amplifier [7] has presented a parallel-amplification logarithmic amplifier using parallel-summation to realize input signals with a wide dynamic range within an appropriate frequency range. Another parallel-summation logarithmic amplifier is introduced in [12], in which the input neural and bio-potential signals are amplified through a series of limiting amplifiers, and then a parallel summation technique is utilized to actualize the logarithmic feature. Topology is another key factor that influence the feature of amplifier. In ULP applications filed, LNA is frequently designed using a variety of topologies. As for the aforementioned LNA [8], it is based on inverter-based shunt feedback topology. In order to reduce power consumption, an intuitive and effective method is altering the supply voltage and making it lower. By lowering the threshold voltage of transistors in a cascade, they can operate in the saturation region and need very little voltage headroom. Therefore, MOSFET body-to-source connections can be used. To make LNAs operate at low supply voltage, this technique is typically incorporated into inverter-based LNA topologies [13]. For UWB receiver systems, CMOS LNAs can be used and current-reused technique is adapted in the mentioned

LNA [9]. In addition, using the folded-cascode topology with current reused technique, this LNA adapt the current reused topology in which two stages cascade sharing the same current source without causing linearity problem, rather than another kind of current reused technique which is made of NMOS and PMOS pairs in shunt configuration in order to achieve transconductance with same power consumption [9]. Figure 13 and Figure 14 show some mentioned structures of the ULP LNA topologies.

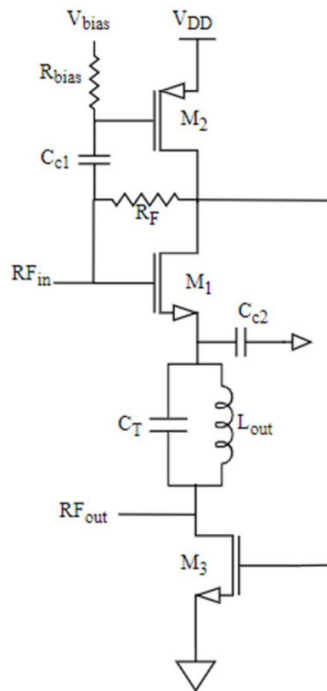


Figure13. Current-reuse gm-boosting LNA.

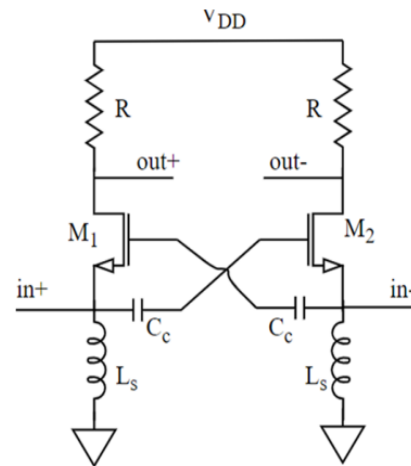


Figure 14. Cross-coupled common gate LNA.

6. Conclusion

In various application fields, different kinds of low power low noise amplifiers are used since they are connected to different output device. The difference between their signals and required functionality result in their varied integrated circuit structures and chosen topologies, ulteriorly, has a great influence on their performance including band width, gain, noise, power, supply voltage and so forth. With the development of integrated circuits, advanced techniques that can optimize the performance of low power low noise amplifiers, especially lower power consumption and lower noise effect, are used and they have a close relation with circuit structure as well.

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