Comparison of Low Power High Speed Comparator for Flash ADC

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Abstract. The analog to digital converter (ADC), a bridge between digital world and analog world, plays a crucial role in the modern semiconductor industry. Among different types of ADCs, the flash ADC (also known as the direct-conversion ADC) is exceedingly fast, whose high sample rate enables many large bandwidth applications, such as optical communication, radar detection. The comparator circuit is one of the critical components of flash ADC. The characteristics, like latency, gain and power consumption, of comparators determine the overall performance of flash ADCs. This paper analyzes and compares different types of comparator architecture and suggests a high-performance design for flash ADC.

Keywords: Comparator, Flash ADC, Power dissipation, Propagation delay

1. Introduction

The signals generated in nature are usually analog signals, which are continuous signals representing other quantity. But for the benefits of digital signal in processing and storage, ADCs are designed to convert continuous-time, analog signals to binary-coded, discrete-time, digital ones. At present, low-power and high-speed ADCs are much-needed in many fields. Bioimaging applications like Magnetic Resonance Imaging (MRI) and Computed Tomography (CT) need high sample-rate and high-resolution ADCs [1]. For wearable biomedical applications, low power dissipation is prior [2].

Various types of ADC architecture have respective advantages and drawbacks. Flash ADCs are the fastest one among these designs because of its simple paralleled structure [3], at a cost of area and power consumption by a huge number of comparators. Because of the huge quantity of comparators, the overall function of flash ADC is largely determined by the performance of comparators.

This paper includes three sections. Section 2 gives a brief description of flash ADC architecture. Section 3 compares various comparator topologies. Finally, section 4 gives a recommended topology as conclusion.

2. Flash Adc Architecture

Figure 1 gives a brief structure of a flash ADC consisting of resistor ladder, comparators and encoder.

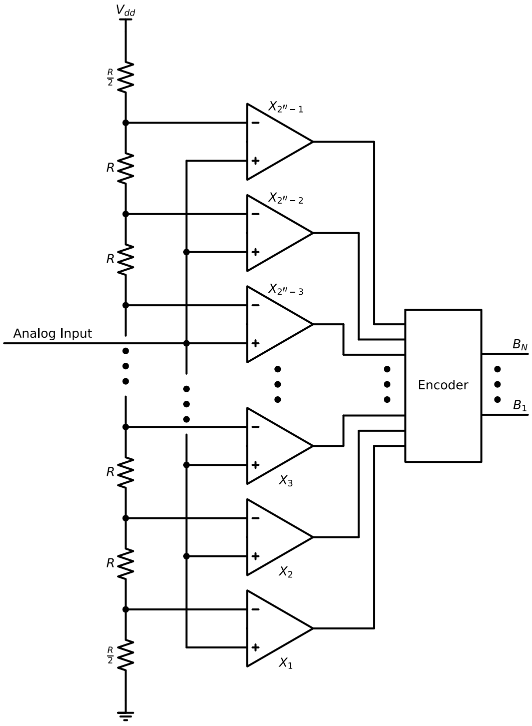

Figure 1. Schematic flash ADC diagram.

The resistor ladder is used to provide successive reference voltage. One end of these series resistors is connected to $V_{dd}$and the other end is connected to GND. For a N bits flash ADC, at least 2^N resistors are needed to divide the reference voltage into $2^N - 1$ reference voltages. Comparators are the most crucial components, which determine the overall performance of flash ADC. To build a N bits flash ADC, at least $2^N - 1$ comparators should be used. The corresponding reference voltage of resistor ladder is connected to the V_- of each comparator and the V_+ of all comparators is attached to the input voltage. The comparisons of input voltage and reference voltage is logic number either 1 or 0. The encoder converts the thermometer code, generated by previous comparators, into the straight binary code [4].

3. Comparator TOPOLOGIES

Different comparators are compared in aspects of power consumption, latency, etc. in this section to reach a suggestion of a high-performance flash ADC.

3.1. Conventional comparator

A conventional comparator is usually comprised of two stages: a former stage named pre-amplifier stage and a later stage named the latch stage. The two-stage structure is shown in Figure 2.

Comparator operation is divided into reset phase and evaluation phase [5]. When $clk = 1$ and $\overline{clk} = 0$, the comparator is in reset mode. Both M4 and M5 are on to discharge the outputs of the former stage and M1 is cut-off to preventing outputs from charging. M6 and M9 are on to charge the outputs of later stage to Vdd. During the evaluation phase, clk goes high and $\overline{clk}$ goes low. Then the outputs of the former stage start to change. The charging rate depend on the ratio of the current flowing through either of the transistors to the node capacitance value. Gradually, the former stage generates differential voltages at the output nodes caused by the different charging rate. Once either of the output voltages is over the trigger voltage of M10 or M11, the dynamic latch is on. Because of the positive feedback feature of the latch, the one of the output node voltages reaches V_{dd}, while the other locks at GND. Both outputs of pre-amplifier stage reach V_{dd} eventually.

In this topology, the outputs of the former stage are charged during the evaluation stage and discharged during the reset stage, which demands for larger transistors and causes huge power dissipation. This drawback makes this conventional comparator an inappropriate structure for low power applications.

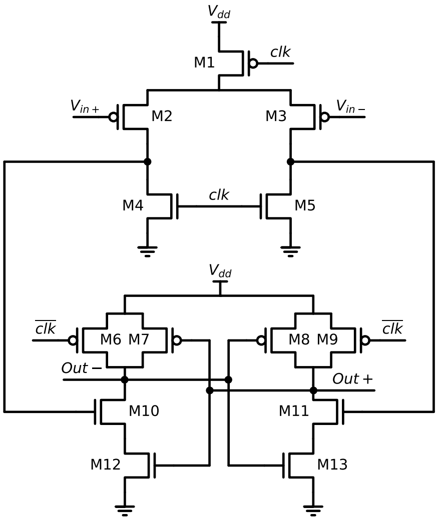

Figure 2. Circuit diagram of conventional comparator.

3.2. Transconductance-improved comparator

The transconductance of the latch is increased in this dynamic comparator (shown in Figure 3) to reach a lower latency. In the reset phase, when $clk = 0$, the outputs of former stage are charged to Vdd. M6, M7 are on and M8, M9 are off. The outputs of the later stage are charged Vdd via M6 and M7. At the beginning of evaluation stage, clk' is delayed, so that M8, M9 are switched on later to reduce the energy consumption of short current through M10 and M13. At the same time, the final output nodes are discharged from V_{dd} while $D_{+/-}$ are charging from GND. Therefore, transistors M6, M7, M11, M12 are working in triode region. When $clk' = 1$, M8 and M9 are turned on, hence the outputs of the second stage are rapidly discharged to $D_{+/-}$. And then the final outputs are locked at V_{dd} or GND.

The overall transconductance of this latch stage structure increases higher and faster than its counterpart. This benefit makes this comparator achieves faster comparison and lower power consumption.

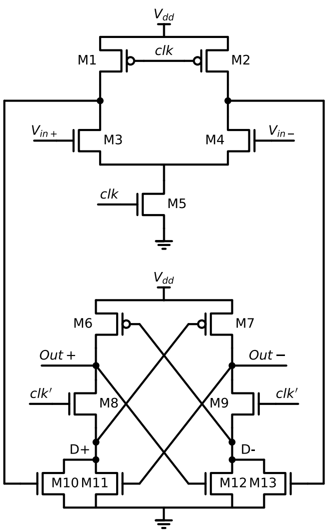

Figure 3. Circuit diagram of transconductance-improved comparator.

3.3. Improved two-stage comparator

Figure 4 represents an improved two-stage comparator. At the reset phase, clk, clk', clk'' are high to discharge the outputs of the pre-amplifier and the latch to GND through M14 and M17. When in the evaluation phase, the clk and clk' firstly toggled to 0 to start pre-amplification. The cross-coupled circuit (M_{4-6}) increases differential voltage while reduces the common-mode voltage at the former stage outputs, which provide strong driver for the latch stage. Finally, clk'' is turned to 0 to activate the PMOS latch and clk' toggled to 1 simultaneously in order to turn off M1, which avoid excess power consumption.

There are two features in this comparator design. The first one is adding a cross-coupled circuit into the pre-amplifier, which exceedingly larger the pre-amplifier gain. The second one is activating and disactivating pre-amplifier and latch in sequence to reduce energy consumption. These advantages make the improved two-stage comparator a low offset low power high speed comparator.

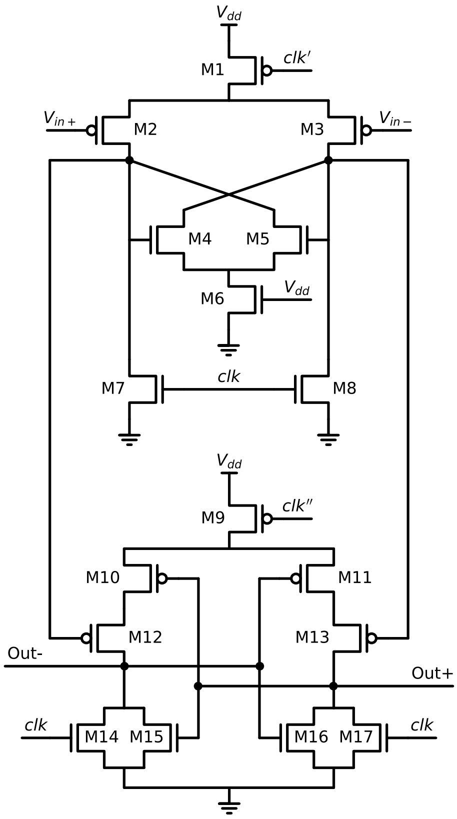

Figure 4. Circuit diagram of improved two-stage comparator.

3.4. Fully differential double tail comparator

Figure 5 shows a fully differential double tail comparator. When $clk = 0$, in the reset mode, transistors M1, M2, M8 and M11 are on. Both the outputs of the former and the later stage are changed to V_{dd}. When clk goes high, the comparator is in evaluation mode. Transistors M1, M2, M8 and M11 are off to stop charging. The outputs nodes of the second stage are discharging to GND through transistors M3-6 that are well tuned to ensure the same current in different pair [6]. Due to difference between input voltages, one of the differential pair is discharging faster than the other. When voltage of either the former stage outputs is over the trigger voltage of the latch, the final outputs are locked to either V_{dd} or GND.

In this comparator design, M1 and M2 convert a single tail comparator into the double tail comparator with a differential input, which reduces the power consumption and decreases offset voltage with an acceptable propagation delay increase.

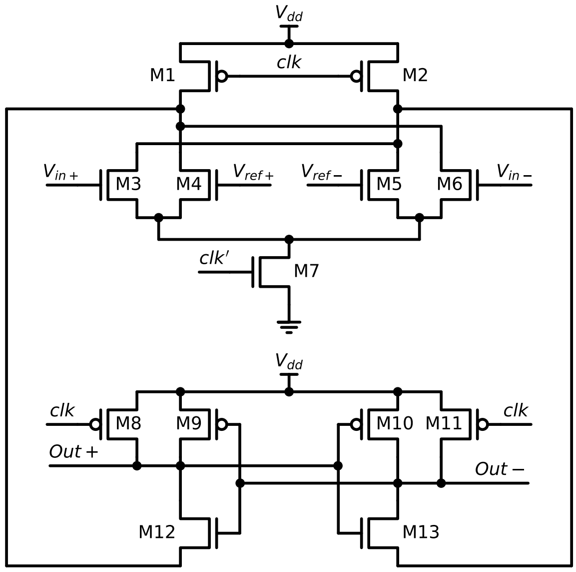

Figure 5. Circuit of fully differential double tail comparator.

4. Comparative Analysis

Various techniques are used to cut power dissipation, reduce delay and improve operation frequency in various comparator design. Table 1 shows a comparison of the key performance indicators of comparators mentioned above, which shows that the transconductance-improved comparator has most suitable power consumption whereas the improved two-stage comparator has the lowest propagation delay.

Table 1. Comparison of comparator topologies

	Technology	**Area**	**Operation frequency**	**Power dissipation**	**Delay**
Conventional comparator [7]	-	440μm^2*	0.5GHz*	420μW*	301ps*
Transconductance-improved comparator [8]	180nm	252μm^2	2GHz	72.2μW (0.5GHz)*	268ps*
Improved two-stage comparator [9]	180nm	530μm^2	0.5GHz	230μW	263ps*
Fully differential double tail comparator [10]	180nm	257μm^2	1.3GHz	265μW	370ps

* Simulations values.

5. Conclusion

This paper compares different novel comparator topologies for Flash ADC. Among the mentioned comparators, transconductance-improved comparator has the lowest power consumption of 72.2μW and the operation frequency of this comparator is up to 2GHz, which is the highest. So, it is a relative suitable choice to make flash ADC for low-power high- speed applications.

The future work is to implement a flash ADC by this comparator structure and simulate or measure the total propagation and latency of the ADC, which can be combined with other techniques such as reducing number of comparators in flash ADC.

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