

## Current state and challenges of ECG amplifiers

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**Abstract.** This paper describes and compares three amplifiers for ECG recording, namely a four-transistor stage band-pass amplifier, a DDA-based fully differential CMOS instrumentation amplifier and an OTA amplifier using current reuse. The performance metrics of the three amplifiers are listed, their respective advantages are compared, what factors limit their disadvantages are analyzed, the current state of the art and the direction of development of the ECG amplifier are indicated, and suggestions are given for further enhancement of the ECG amp. These amplifier circuits are designed in 0.35  $\mu\text{m}$  CMOS and are verified by layout followed by simulation simulations. The results show that running at 2V dc supply, the quad-transistor stage amplifier and the DDA fully differential amplifier consume 672nW, obtain at least 2uVrms of input reference noise, and obtain greater common mode rejection ratios of 86dB and 83dB, while the OTA amplifier consumes less 320nW, obtains the most 2.05uVrms of input reference noise, and obtains a smaller common-mode rejection ratio of 65dB.

**Keywords:** Bio-signal amplifier, Class AB, current reuse, ECG recording

### 1. Introduction

An Electrocardiogram (ECG) is the most extensively used diagnostic method in clinical cardiology that measures and records the electrical activities from muscle fibers of heart's different parts and is one of the most important information for wearable and portable devices to detect from human bodies as well to provide monitoring and diagnostic functions [1,2]. The ECG can be useful in the screening of a substantial number of cardiac pathological, however, a resting ECG captured at one moment is not instructive for the potential irregularities of the heart and delayed detection is accordingly one of the main reasons leading to the high death rate of cardiovascular diseases [2,3]. Continuous ECG monitoring is therefore of significant value for early detection and subsequent treatment of cardiovascular diseases. Conventionally, the ECG is captured via 12 leads on body surface and is usually conducted by trained clinicians and staff, hence the availability and usefulness of which is largely limited outside the clinic [2]. With the growing health awareness of the public, this leads to the rapid development and the wide use of portable and wearable ECG devices.

ECG signals are usually of an amplitude range from micro volt to mill volt and a frequency range from 0.1 to 150 Hz. When captured from the electrodes, the ECG signals are always accompanied by various types of noise, including flicker noise, power line interference and the offsets caused by the impedance of electrode-skin interface. Because of the characteristics of low amplitude and low frequency and the presence of noise and offsets, it is of high necessity to design an input amplifier circuit with appropriate amplification, adequate noise suppression and sufficient common-mode rejection rate and DC offset cancellation for raw ECG signal recording and subsequent processing and interpretation [4-6]. Moreover, the designed amplifier circuits are required to have high input impedance for safety reasons and low output impedance to minimise distortion [5]. For portable ECG solutions, small size and low power consumption of the input amplifier circuit are of high importance

due to the portability and battery life of the product. Therefore, the trade-off between the performance of the amplifier and the ability for continuous operation is important when designing ECG amplifiers.

P. Pantuprecharat et al. [7] proposed an amplifier topology composed of a four-transistor current-feedback instrumentation amplifier and a RC feedback network. The power consumption is 0.672uW with no off-chip components. Because of the compact structure, simply four transistors, an input referred noise of 2uVrms, an NEF of 2.71 and a PEF of 13.2 are achieved in a dimension of simply 257\*277 um<sup>2</sup>, fabricated in 0.35um technology. With a standard high-swing cascade current mirror, the four-transistor amplifier reaches a high common-mode reject rate of 86dB without additional processing techniques. A similar amplifier topology was proposed in [8] where eight transistors were used to establish a compact instrumentation amplifier and RC feedback loops were also employed to provide the AC-only amplification. Fabricated in 0.35um process, at the same dimension and power consumption as [7], the input referred noise, NEF, PEF and CMRR of this topology are 1.54uVrms, 2.02, 8.16 and 84.2dB respectively.

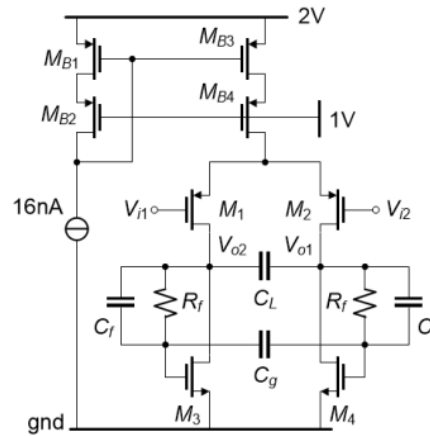
J. Zhang et al. [9] proposed a current-reused OTA based amplifier topology consisting of a two-stage current-reused OTA, a bias circuit for quiescent point control and a common mode feedback (CMFB) circuit. In the proposed OTA structure, the inverter-based fully-differential input pair and class-AD output stage are used and the control unit for the class-AB output structure is integrated in the input stage to utilize the supply current in both input and output stage efficiently. Fabricated in 0.35um process, the chip size is 300\*600 um<sup>2</sup> but the power consumption is simply 0.32uW. The input referred noise, NEF, PEF and CMRR are 2.05uVrms, 2.26, 10.2 and 65dB respectively.

This paper compares and analyses the three typical designs of ECG amplifiers, indicates the current situation and future development of ECG amplifier techniques, and gives suggestions for further improvement. The literature review of the three amplifiers' topological and performance analysis are included in Section II, III and IV respectively. Section V compares and analyses the advantages and limitations of three different amplifier designs. Conclusion and further suggestions are provided in Section VI.

## 2. A four transistors amplifier

### 2.1. Design and construction of the amplifier

A four-transistor stage amplifier combining a typical wide-swing cascaded current source with a capacitor-resistor is presented in [1] to achieve a low noise and high input impedance ECG acquisition system. The structure of this pre-amplifier is shown in the Figure 1, with transistors M1-M4.4 using differential inputs, and adjusting their aspect ratios to obtain high input impedance and low noise. To achieve this, first let M1-M4. all have the same trans-conductance and the transistors generate an IA. MB1-MB4 act as current mirrors and the bias current is supplied to the IA via MB1-MB4. If the transistor size becomes smaller, the gate-source parasitic capacitance of M1 and M2 becomes smaller and the input impedance becomes larger. The connection of the poly capacitors  $C_f$  and the feedback pseudo resistors Rf (made of a diode connected to the MOS) between M1-M4 acts as a filter. Vo2 and Vo1 are connected to M3 and M4 via the feedback resistors, and by determining the size of the M3 and M4 transistors a suitable common mode level can be obtained. IA also controls the output noise of the amplifier circuit. The thermal noise equation is expressed approximately as  $V_{n,in}^2 \cong 32n_p kT / 3g_m$ , where k is the Boltzmann constant, T is the absolute temperature and  $g_m$  is the trans-conductance of M1-M4. By setting the aspect ratio of M1-M4 one can control the trans-conductance  $g_m$ , which affects the thermal noise.



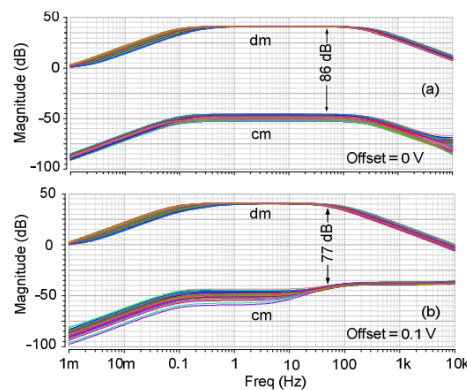
**Figure 1.** Transistor-level topology of the ECG amplifier [7].

## 2.2. Performance Analysis

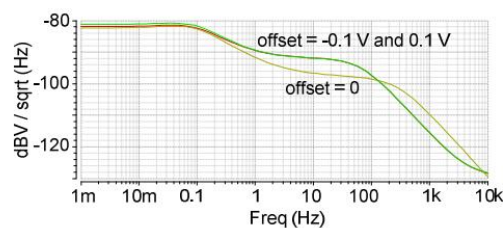
The four-transistor stage amplifier circuit was simulated using 0.35  $\mu\text{m}$  CMOS data, with the transistor lengths, widths and circuit component parameters shown in Table 1. Figure 2 shows the amplitude response of the amplification circuit at different offsets. The images present typical band-pass filter characteristics with a low cut-off frequency of 0.1 Hz and a high cut-off frequency of 279 Hz, corresponding to a DC gain result of 0 dB and a mid-band gain of 40dB. The corresponding common mode rejection ratios are 86 dB and 77 dB for an input offset of 0 and 0.1 V, respectively, at a bandwidth of 50 Hz. Under normal conditions, the common mode rejection for these two offsets are greater than 60 dB under normal conditions, which is a good solution to the problem that ECG devices can suffer from interference or internal electrode impedance imbalance. Figure 3 shows the analogue output noise power spectral density. The reference noise is integrated to  $2\mu\text{V}_{\text{rms}}$  between the low and high cut-off frequencies according to the setting of the M1-M4 aspect ratio data in Table 1. Figure 4 shows the magnitude of input impedance in amplifier at different frequencies, which is 295 M Ohms as the frequency increases to 50 Hz. As the frequency increases to 300 Hz, the input impedance decreases to 70 M ohms. The input impedance is greater than 10M ohms within the controlled frequency range of the circuit, which indicates that the amplifier circuit can meet the minimum readout criteria for ECG [1]. The simulation results show that the parameters of the transistors in the amplifier are crucial. The internal additional capacitors and resistors act as filters, while  $M_1$  and  $M_2$  act as differential inputs. Adjusting the size of the aspect ratio allows the values of the input impedance and output noise to be changed, thus increasing the common mode rejection to a minimum input impedance of 10 dB and the minimum CMRR of 60 dB for cardiac devices. in addition, the amplifier occupies a much smaller area and generates less noise than other amplifiers.

**Table 1.** Circuit Parameters [7].

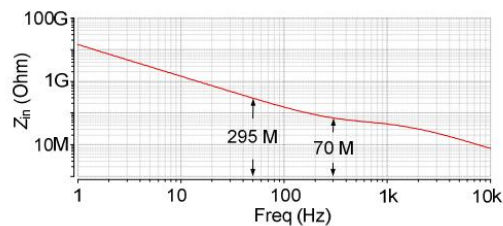
MOSFET	W(um)	L(um)
$M_1, M_2$	400	4
$M_3, M_4$	160	20
$M_{B1}, M_{B2}$	3.6	1.8
$M_{B3}, M_{B4}$	80	1.8
$M_R$	1	4
Capacitor	Value(pF)	
$C_f, C_g, C_L$	0.35,20,10	
Biasing	Value	
$I_{total}, V_{DD}, V_{B1}$	336nA, 2V, 1V	



**Figure 2.** (a) zero offset and (b) offset = 0.1V corresponding to the AC response [7].



**Figure 3.** Offset corresponding to the output noise spectral density [7].



**Figure 4.** Simulated amplifier input impedance [7].

### 3. A DDA based eight transistors amplifier

#### 3.1. Design and construction of the amplifier

This ECG circuit consists of eight transistors, two capacitors and two resistors. This amplifier needs to capture the low input reference noise to capture the small amplitude of the electrical signal. Because of the need to achieve a high common mode rejection ratio, an input resistor of greater than 10m ohms is required. Also, the use of MOS pseudo-resistor is proposed to make DDA miniaturized and low power consumption. In order to achieve miniaturization, the use of off-chip devices should also be avoided, because the use of off-chip devices will lead to large area. As shown in Figure 5,  $M_1-M_4$ (the main transistor elements  $g_{mA}$  and  $g_{mB}$ ) act as the DDA together with the MB1-MB4 to provide the bias current for the amplifier. While the amplifier is at rest, the source coupling pair: MB4 will provide a tail current, and the  $M_1-M_4$  mentioned above will draw this current, based on which it will be divided into two parts, ID1 and ID2. This allows the ECG signal to account for its own scattering and flickering noise within a controlled range. Large physical devices can be used to effectively suppress flicker noise.  $M_1-M_4$  needs to be amplified to keep the angular frequency of the flicker noise below 10HZ, so that the chip area is acceptable, and the capacitor will still be dominant.

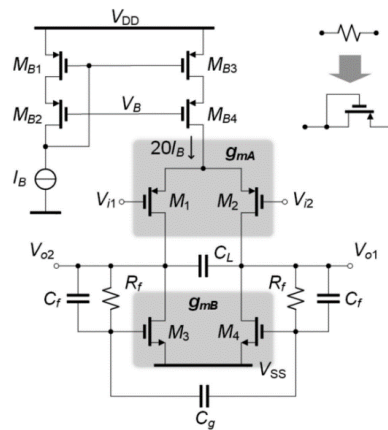


Figure 5. Transistor-level ECG amplifier [8].

### 3.2. Performance Analysis

The amplifier does not require a CMFB circuit. Therefore, power saving can be achieved not only by share the bias current ( $g_{mA}$  and  $g_{mB}$ ), but also the power consumption and area of the circuit (CMFB). In order to adapt to the large power line interference or common mode rejection ratio and supply voltage (VDD), the authors used the standard wide pendulum common source and common gate 20 times current for the current mirror circuit ( $M_{B1}$ - $M_{B4}$ ). When the output voltage starts to saturate, the  $V_{ID}$  will exceed  $\pm 400\text{mV}$ . The results showed that the Kdc (gain) could be keep in the range of  $\pm 360\text{mV } V_{ID}$ , the rate of change of gain per unit distance is  $\pm 5\%$ . The mean  $\pm$  standard deviation of CMRR in the range of 80.33 dB-87.08 dB was  $83.24 \pm 2.04$  dB. Figure 6 shows the noise output of the amplifier in the case of zero to +100mV paranoia. The CMRR were 86.4, 84.2 and 69.4dB. Figure 7 shows the measurement results of the CMRR of the poly-chip. The input offset also affects the linearity of the amplifier, as shown in Figure 8. At zero offset, 0.12% of the Total harmonic distortion is related to the amplitude of 5MV. For  $\pm 100$  mV bias, THD rose to 2%.

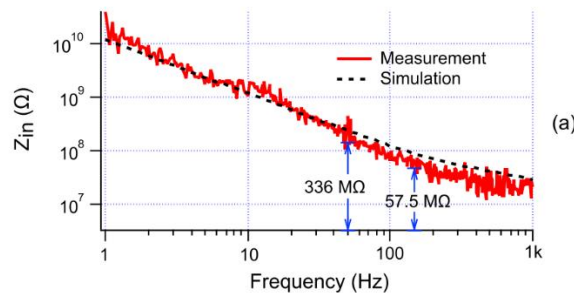


Figure 6. Output noise spectral density with input offset (0 mV to + 100 mV) [8].

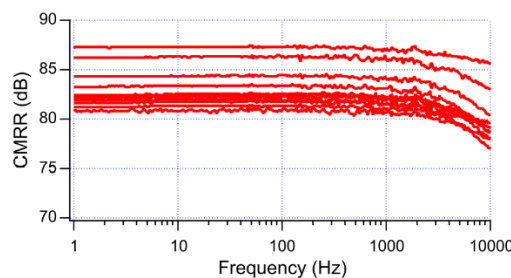
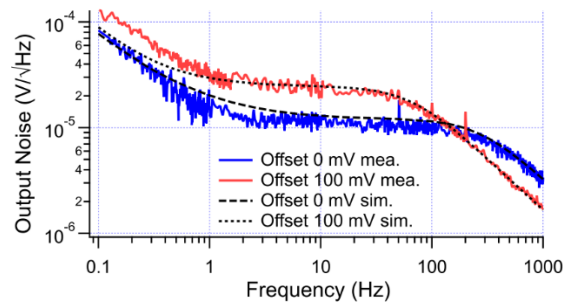


Figure 7. Multi-chip CMRR measurement [8].

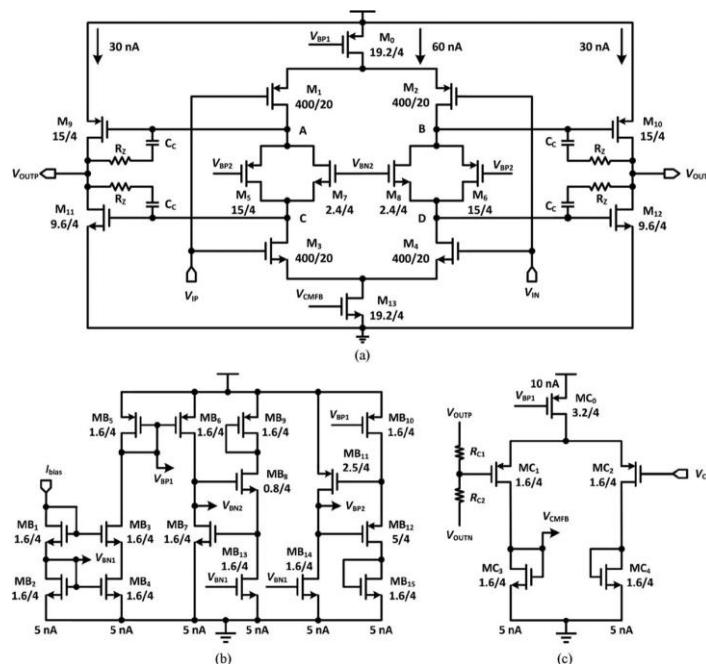


**Figure 8.** The measurement of THD with various input offsets ( $-100\text{ mV}$  to  $+100\text{ mV}$ ) for input amplitude starting from  $2\text{ mV}_p$  to  $5\text{ mV}_p$  [8].

## 4. A current-reused OTA based amplifier

### 4.1. Design and construction of the amplifier

A current-reused OTA based amplifier was proposed in [9] to achieve portable ECG recording at low noise level and power consumption. This amplifier topology is composed of a two-stage current-reused OTA, a bias circuit for OTA quiescent point control and a continuous-time common mode feedback (CMFB) circuit, shown in Figure 9(a), (b) and (c) respectively. The two-stage OTA architecture is adopted rather than single-stage topology due to better performance in terms of open-loop gain, output swing and linearity. At the input stage, the inverter-based input pair is adopted to reach double trans-conductance at the same bias current, enhancing PNR, and the fully differential input structure is used to remove the inferences from power-line and common-mode artifacts. At output stage, the class-AB output structure is applied for high current efficiency and output driving capacity, improving power consumption efficiency and reducing output distortion. In this OTA topology, the control unit circuits of the class-AB output stage are integrated into the input pair (between nodes A&C and B&D), which are used to provide stabilized quiescent current, to dispense with the need of an extra bias branch. Therefore, the supply current is used in both input and output stage to enhance current efficiency, therefore this OTA architecture is named as 'current-reused' OTA by the authors.



**Figure 9.** Topology of the proposed amplifier: (a) the two-stage current-reused OTA; (b) the bias circuit; (c) the CMFB circuit [9].

#### 4.2. Performance Analysis

The amplifier circuit is manufactured in 0.35 $\mu$ m CMOS process with a core area of 0.3\*0.6 mm<sup>2</sup>. With this current-reused OTA based low-noise low-power capacities-feedback amplifier topology, an input-referred noise of 2.05 $\mu$ V<sub>rms</sub> and a current consumption of 160nA under a 2V supply are achieved, and the noise efficiency factor (NEF) is hence calculated as 2.26. The bode plots of differential-mode, common-mode and power supply gains are shown in Figure 10. The designed closed-loop gain of the amplifier is 100 and the differential-mode gain is measured to be approximately 40dB with a bandwidth of 0.2-200 Hz. The common-mode gain and power-supply gain are measured as lower than -25dB and -30dB respectively, leading to a common-mode rejection ratio (CMRR) of higher than 65 dB and a power supply rejection ratio (PSRR) of larger than 70 dB respectively. A total harmonic distortion (THD) of lower than 1% at the maximum peak-to-peak input of 15mV and 20Hz is achieved, measured by a 10-bit ADC with a sampling rate of 500S/s. With the current-reused structure, the current efficiency of this amplifier is improved and a NEF of 2.26 is reached, which is of excellent performance among 2-stage OTA architectures under similar processes. Hence, under a 2V power supply, the power efficiency factor (PEF) can be calculated as 10.2. This is mainly limited by the minimum value of supply voltage because the 0.35 $\mu$ m technology limits the high threshold voltage of the transistors. However, this can be further improved by using more advanced CMOS technologies and lower PEF can be expected.

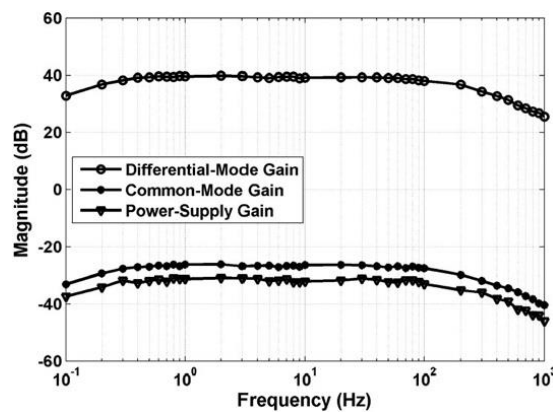


Figure 10. Measured differential, common-mode and power supply gains [9].

#### 5. Comparison and Discussion

Table 2 shows the performance of four and eight transistor amplifiers and an OTA amplifier based on current reuse. The results show that both the four and eight transistor amplifiers have very similar circuits and images and that the area of the circuit system is the same. the difference in CMRR is only 2.76 dB and the difference in Gain is only 0.6dB. their VDD and power are identical at 2 V and 0.672 $\mu$ W respectively. this is because both ECG amplifiers use differential inputs and by adjusting the differential parameters of the partial transistors to vary the CMRR and noise. The advantage is that the input impedance and noise can be easily adjusted, but the current consumption is higher and the power loss is greater. the OTA amplifier has a larger area but less power. the area of the OTA amplifier is nearly twice as large as that of the quad and octal transistor amplifiers. the CMRR of the OTA is greater than 65dB and the gain is similar to that of the first two amplifiers. However, the bandwidth of the OTA is the smallest at 0.2-200Hz. the OTA uses a current reuse structure and the current efficiency and power efficiency factor of this amplifier is improved, but the 0.35micron technology limits the high threshold voltage of the transistors and a lower PEF can be obtained with more advanced CMOS technology. However, all the amplifiers will eventually reach saturation, which will make the ECG signal invisible [10], which means the goal for the future development is to preserve common mode on the analogue front end, improve differential input performance, and increase differential mode dynamic range.

**Table 2.** Performance summary and comparison [7-9].

	Four transistors amplifier	A DDA based eight transistors amplifier	OTA current-reused amplifier
Tech[um]	0.35	0.35	0.35
Itotal[uA]	0.336	0.336	0.16
VDD[V]	2	2	2
Power[uW]	0.672	0.672	0.32
Gain[dB]	40	40.6	39.8
BW[Hz]	0.1-279	300,1k	0.2-200
NEF	2.71	2.02,2.63	2.26
PEF	13.2	8.16,13.9	10.2
IRN[uVrms]	2	1.54,2.01	2.05
CMRR [dB]	86	83.24	>65
Area[mm <sup>2</sup> ]	0.071	0.071	0.18

## 6. Conclusion

This paper analyses three simple, compact and effective ECG amplifiers using four transistors, two pairs of PMOS, NMOS tubes and a technique based on current reuse OTA. The measurements show that all of these amplifiers have a high common-mode rejection ratio, a high input impedance and a low noise level. The four- and eight-transistor amplifiers use fewer components and are compact enough to achieve input impedance of 10 M ohms without the use of complex chopping techniques, resulting in common-mode rejection ratios greater than 80 dB, while the OTA amplifiers reduce energy consumption by increasing power-to-noise efficiency through inverter-based difference and reducing amplifier power consumption by removing excess bias current. In the future, ECG will also need to enhance the design of front-end amplifiers. At some point the amplifier will saturate and the ECG signal will not be visible, so maintaining analogue front-end common mode, differential input performance and extending differential mode dynamic range is the challenge for the future.

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