# An Review of Dynamic CMOS Comparators

Yuchuan Liu*

School of Electrical and Electronic Engineers, University of Electronic Science and Technology of China, Chengdu, Sichuan Province, 610000, China

*Corresponding author email: 2510695l@student.gla.ac.uk

**Abstract.** CMOS dynamic comparators contributes a major role on the implementation of mixed signal successive approximation register (SAR) type of analog to digital converters (ADC). High precision, dynamic range, low voltage operation, high speed, low power consumption, reliability and offset voltage are the critical factors to be considered while designing CMOS dynamic comparators. This paper reviewed the performance of some popular dynamic CMOS comparators such as StrongARM latch comparator, double- tail dynamic-latched comparator, dynamic bias comparator and triple stage somparator.

**Keywords:** Comparator, Analog-to-digital converter (ADC), CMOS, latch, amplifiers, double-tail latch-type comparator, StrongARM comparator, Elzakker's comparator, low power consumption, low-noise, high gain, high speed, dynamic biasing, three-stage, partially charge, kickback-noise.

## 1. Introduction

Comparators, which are the second most widely used analog blocks in the world after operational amplifiers, plays an essential role in many applications. Generally speaking, it is a device which can compare the voltages and currents at its input pairs and generate a digital signal at outputs to distinguish which one is larger. Comparators play an essential role on analog circuits and can achieve a variety of important functions. There are two major uses of comparators, data converters and portable battery operated communication circuit [1]. The influences of comparators on those devices are on the perspective of parameters, like power consumption, immunity to noise, mismatches and offset, speed of conversion, resolution, etc [2].One of the most significant parameters is gain, which can influence the resolution of converters and then directly affect the function of the circuit [1]. Therefore, improving the gain of comparators is a vital thing considered by many engineers, especially the high gain for tiny differential inputs [1]. Another important parameter is power consumption. With time passed by, although the performance of ANALOG-TO-DIGITAL converters (ADCs) have been considerably improved, the power consumption of comparators still occupies nearly 50%–60% of the total power consumption [3]. In addition, widespread use of battery powered applications also necessitate low-power signal processing circuits, resulting in the widespread use of dynamic comparators which can achieve a very low power dissipation and an inactive state when closed [2, 4].

## 2. Literature Review

### 2.1. Strong Arm Latch Comparator

StrongARM comparator, as shown in Figure 1, is the first in the class of dynamic comparator and widely used as regenerative comparator [5]. It has many applications, such as A/D converters and wireline receivers in virtue of its fast decisions and high-power efficiency due to the strong positive feedback and nonexistence of static power consumption [3, 5, 6] The power consumption of StrongARM comparator originates from the charge and discharge of capacitances which is approximately equals to $f_{CK}(2C_{P,Q} + C_{X,Y})V_{DD}^2$. However, because of the single stage [7], there are many problems such as large voltage headroom and considerable kick-back noise [4, 5]. The offset and speed are also highly dependent on the common-mode voltage [5, 7]. Therefore, the solution of these problems is always separate the pre-amplifier from the latch, changing it to double-tail latch type comparators [8].

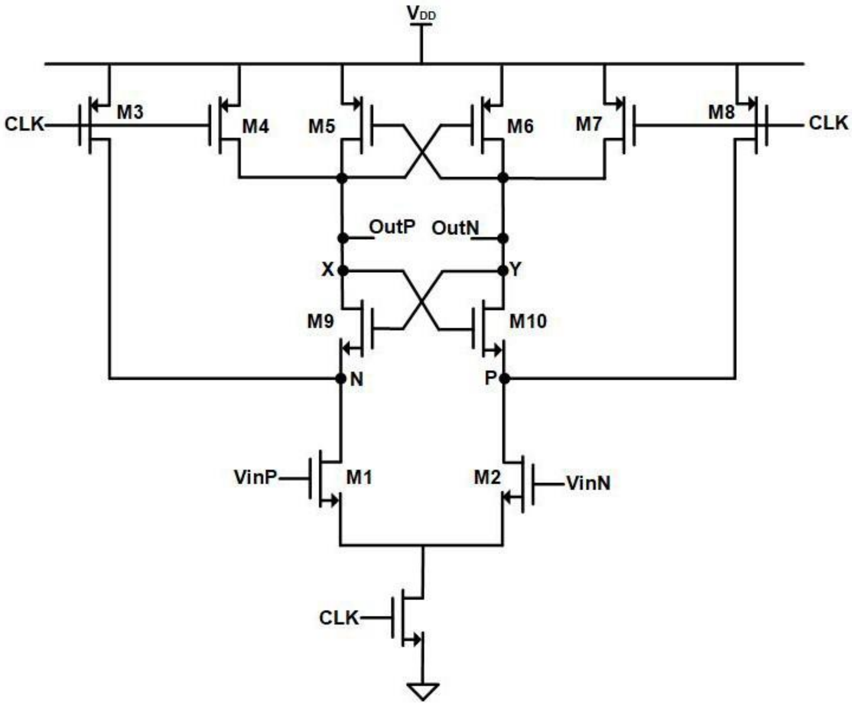


**Fig. 1:** Circuit diagram of StrongARM comparator [5]

### 2.2. Triple-Latch Feedforward Dynamic Comparator

Mixed signal systems, such as ADCs and wireline data links, necessitate high speed, high sensitivity, and low power consumption comparators. The proposed circuits, a three-stage fully dynamic triple-latch comparator with an additional bypassing feedforward path, is introduced to meet the needs and solve the problems existed in prior designs, such as StrongARM and double-tail latch-type comparator [7]. Its multistage nature enables a separate optimization of each stage and a high total gain. The direct path and feedforward path in the proposed circuit can further amplify the differential voltage to stage3, which contributes a lot to rapid regeneration. The whole design achieves altogether a low delay, a low noise/offset, a low sensitivity to VCM and an acceptable power consumption for mixed signal systems. The proposed triple-latch feedforward fully dynamic comparator is shown in Figure 2, which is the combination of three-stage configuration plus a parallel feedforward path, enabling high gain, low delay and separating optimization of each stage.

Stage 1, including an amplifier M1P/M1N and an NMOS latch M2P/M2N, can provide a high gain to decrease the contribution of the following stages. Stage 2, including an amplifier M4P/M4N and a PMOS latch M5P/M5N, is more like an isolating gain between input and output which can minimize the delay if the input differential is too small. As for stage 3, The minimum regeneration time is optimized by its load. Finally, there are two paths remain, the direct path with M9P/M9N and the feedforward path with M8P/M8N, which can minimize the delay for the full range of $\Delta V_I$($V_{inP}$ $V_{inN}$ . M7P/M7N with minimum size are also added to direct path to avoid performance degradation due to the memory effect in the high clocking rate. The signal can trigger the final latch for regeneration through the path of direct, feedforward, or the parallel combination of them.

The time consumed by proposed circuit are calculated as follows:

$$\tau \approx \tau_1 + \tau_2$$

$$\tau_{FF} \approx \frac{2}{1+\frac{g_{m4}}{g_{m5}}} + \frac{3}{1+\frac{g_{m9}}{g_{m6}}}, small\ differnetial\ voltage$$

$$\tau_{FF} \approx \frac{\tau_3}{1+\frac{g_{m8}}{g_{m6}}}, large$$

Where gm4, gm5, gm6, gm8, and gm9 are the transconductances of M4P/M4N, M5P/M5N, M6P/M6N, M8P/M8N and M9P/M9N, respectively, and τ2 and τ3 are the time constants of stage2 and stage3.

During the reset phase (CLK=0), M2P/M2N, M3P/M3N, M5P/M5N, M6P/M6N, M7P/M7N, M4P/M4N and M9P/M9N are conducted while $M_a$, $M_b$ and $M_c$ are closed. As for transistors M4P/M4N and M9P/M9N, they can obviate the need for dedicated reset devices and reducing the load on their critical nodes. The nodes VXP/VXN, and outputs $V_{OP}/V_{ON}$ are precharged to $V_{DD}$ while the nodes $V_{YP}/V_{YN}$ are discharged to ground.

During the comparison phase (CLK=$V_{DD}$), the voltage difference is generated at the drains of M1P/M1N and then is enhanced by M2P/M2N at $V_{XP}/V_{XN}$. After that, the improved differential voltage is further amplified through the direct path with the MOSFET of M4P/M4N–M9P/M9N chain and the feedforward path with the MOSFET of M8P/M8N. Therefore, the minimized total delay on whole $\Delta V_I$ range can be achieved and the latch of stage3 can regenerate faster on the largest signal provided by the two paths. The simulations about delay versus $\Delta V_I$ and power consumption are carried out on the proposed circuit and prior techniques including StrongARM, Double-Tail, and three-stage comparator without feedforward. To achieve a fair comparison, all the comparators are dimensioned for similar input referred noise ( 1m$V_{rms}$), offset ( 11m$V_{rms}$), and latching drive strength, while the same output load is provided to all of them. The results represent that when $\Delta V_I$ is equals to 5mV, the TLFF circuit shows the 40%, 30% lower as well as a similar delay and the 32%, 15% larger as well as a similar power consumption compared to StrongARM, Double-Tail, and three-stage comparator without feedforward respectively. When $\Delta V_I$ equals to 200mV, TLFF achieve an approximately results of 25%, 25% and 32% lower delay compared to the aforementioned circuits respectively. In real test, the measured delay for 5m$V_{PP\ diff}$ input of prototype comparator in 28nm bulk CMOS with a core area of 78 $\mu m^2$ is 26.8ps and the delay versus $\Delta V_I$ slope is 6.4ps per decade, which is closed to the simulated results. In addition, TLFF can achieve a performance of ¡ 70ps delay across a wide $V_{CM}$ and $V_{DD}$ range.

## 2.3. Elzakker's Dynamic Comparator

A type of dynamic two-stage comparator, designed by van Elzakker et al usded in SAR ADCs is shown in Figure 3. By delaying the conduction of the latch stage until a sufficient gain is obtained at the output of pre-amplifier, a more advanced solution to improve the power consumption [9].

There is no explicit tail transistor in the latch stage. The whole circuits can be divided in two parts: the pre-amplifier with a differential input (InP, InN) as well as a differential output (OutP, OutN) and the latch stage with a simple voltage amplifier and a positive-feedback amplifier. At the start of the comparator operation (CLK=0), transistors M4, M5, M6, M7, M12 and M13 are conducted, while transistors M3,

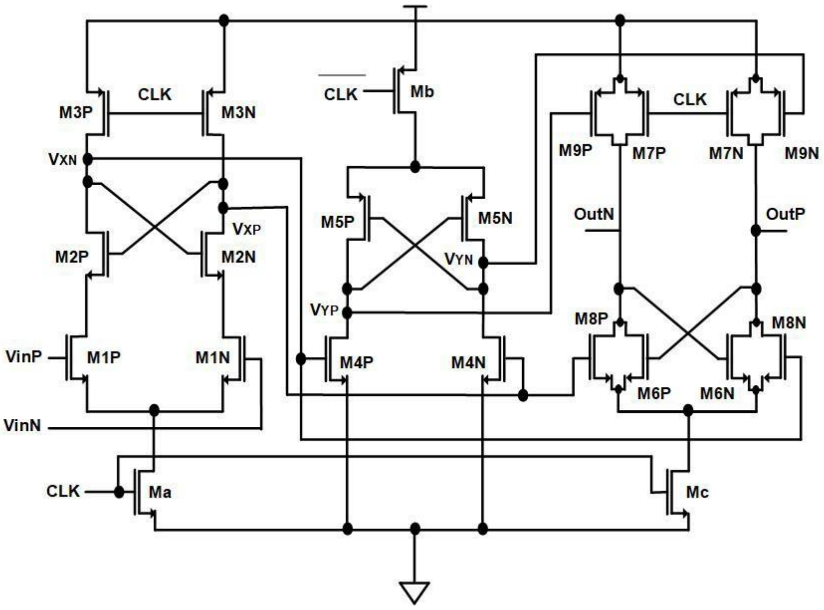


**Fig. 2.** Circuit diagram of triple-latch feedforward dynamic comparator [6]

M8, M9, M11 and M12 are closed, which means the output of the pre-amplifier (InN, InP) are at $V_{DD}$ and the latch stage only begin to conduct when the common-mode voltage of the output is below the threshold value of M8 and M9. At the regeneration stage (CLK=$V_{DD}$), which means M8 and M9 become conducted, the sufficient differential voltage (gain) at its input to perform the regeneration operation. Further improvement can focus on pre-charge reduction of the pre-amplifier.

The gain of the pre-amplifier is 5 which is feasible for an energy-saving amplifier and lower than the intrinsic gain of a conducted CMOS transistor thereby without wasting energy for high gain. In addition, the power consumption per comparison under the supply voltage of 1.0V is about 60J. Further comparison with other comparators will be shown in the following contents.

### 2.4. Dynamic Bias Latch-Type Comparator

About 70%-80% total energy consumed by pre-amplifier [9, 10] Therefore, the concentration on pre-amplifier for reduction of energy consumption is feasible. A dynamic bias comparator, as shown in Figure 4, uses a tail capacitor at pre-amplifier to provide a dynamic bias for differential pair and then achieve a partially discharge of nodes N and P to reduce the energy consumption [3]. It can operate in high gain, low input referred noise with small input and small propagation delay with large input.

During the reset phase (CLK=0), transistors M3, M4, M6, M11, and M14 become conducted while M5,

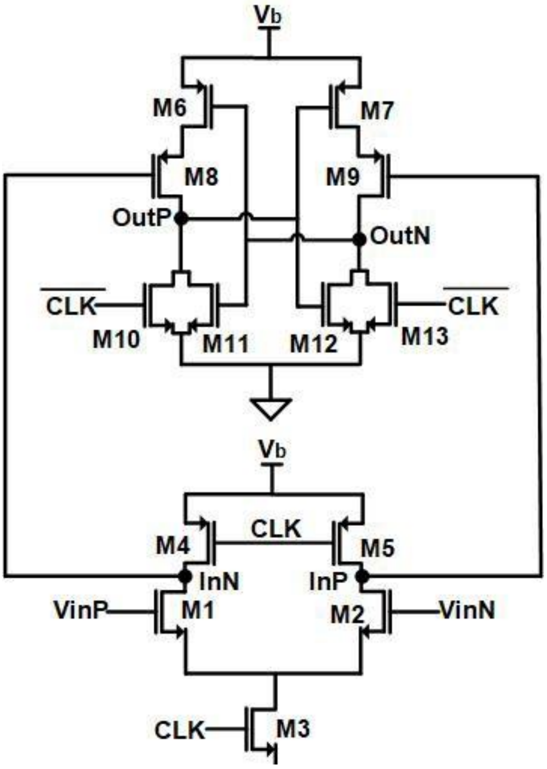


**Fig. 3:** Circuit diagram of Elzakker's dynamic comparator [7]

M7 and M8 closed. Th nodes P as well as N are pre-charged to $V_{DD}$ and M11 as well as M14 reset the latch. As for the tail capacitor $C_{Tail}$, it is discharged since tail transistor M5 is closed and M6 is conducted.

During the comparison phase (CLK=$V_{DD}$), the transistors M3, M4, M6, M11 and M14 become closed while the tail transistor M5 is conducted. Therefore, the nodes P and N start discharging and there is a common-mode current through the tail transistor to charge $C_{Tail}$, resulting $V_{Tail}$ (voltage of $C_{Tail}$) increasing thereby the continuously current decreasing and voltage reduction of $V_{GS}$ of M1 and M2. The decreasing of $V_{GS}$ provides the dynamic bias to the differential pair. In addition, the value of $g_m/I_d$ will increase due to the increase in $V_{Tail}$ and then achieve its maximum when P and N stop discharging. When $V_{GS}$ reduces to the threshold value of transistors M1 and M2, the transistors will turn off, while the voltage of P and N will become static and the voltage of $C_{Tail}$ will reaches its largest value.

This increases the voltage $V_{CAP}$, which reduces the gate–source voltage, $V_{GS}$ of the differential pair ($M1/M2$), thereby providing a dynamic bias to the differential pair during the comparison phase. There- fore, the energy consumed by pre-amplifier in the reset phase can be calculated as $2C_PV_{DD}^2 - C_PV_{DD}(V_{D1} + V_{D2})$ and have a better performance compared to the $2C_PV_{DD}^2$ of power consumption of Elzakker's comparator mentioned above.

In the condition of $V_{CM} = 0.6V$, the measured rms input referred noise is 0.4mV, which is 15% larger than the estimated value of 0.34mV constituted by 0.32mV from pre-amplifier and 0.02mV from latch stage. And the energy consumption per comparison is about 34 fJ for 1mV differential input. However, since for larger input common-mode voltage, the discharge of N and P nodes will also increase thereby lead to larger energy consumption, the energy consumption will become 45fJ/comparison when $V_{CM} = 0.9V$. However, the performance of dynamic bias comparator is not as good as Elzakker's comparator, which is 325 ps/decade and 120 ps/decade respectively since the latch stage of dynamic bias comparator has longer working time in weak inversion for the same input compared to Elzakker's comparator.

### 2.5. Low-Power 1-V Supply Dynamic Comparator

A low-power dynamic comparator design using 65nm CMOS with a supply voltage of 1V is shown as Figure 5. It reduced the power consumption of comparators considerably by preventing the comparator internal nodes from discharging fully to the ground. Instead of using any extra capacitors or complex logic, a simple cross-coupled mechanism is added around the input differential [4].

The widely used Elzakker's architecture has been discussed in C and its structure can be divided into two parts, the preamplifier and the regenerative latch. For every comparison, the capacitors of output nodes (InP and InN) of the preamplifier will be discharged fully to the ground and then recharged to VDD. They are connected to the transistors M8 and M9, whose threshold value of conduction path for regenerative latch is $V_{latch}$. However, when the nodes' voltage of InP and InN is low enough for triggering, the voltage decreasing will not stop until completely discharged, which means the cost of more energy to reset the nodes' voltage. The further discharge, which is the drawbacks of Elzakker's structure, has no benefit to improve the noise or conversion time. Therefore, the ideal for less power consumption is the prevention of the discharge once the nodes' voltage reaches $V_{latch}$.

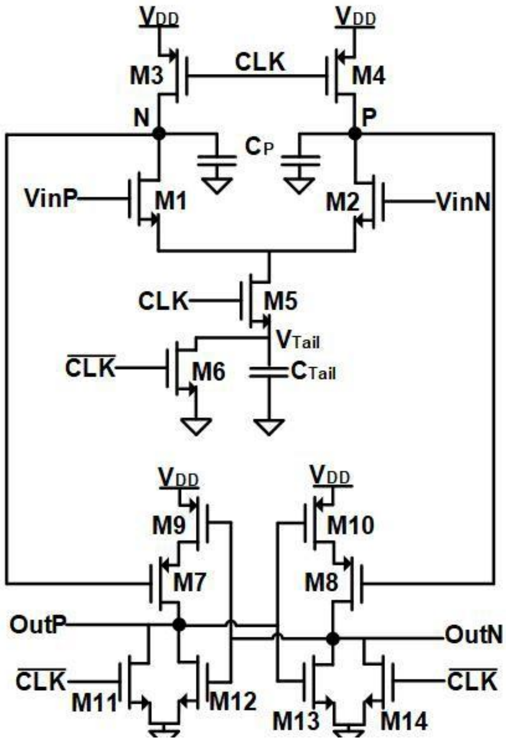


**Fig 4.** Circuit diagram of dynamic bias latch-type comparator [3]

The technique used by proposed architecture just adds a cross-coupled mechanism around the output of pre-amplifier and the operational behavior can be divided in two stages. The whole operational behaviors can be divided into two phases, the reset phase and the amplification phase. In the reset phase, the clock is low, so the transistors M6, M7, M8, M9, M14 and M17 are conducted and M5 is closed. Therefore, nodes InN, InP, N1, P1 are precharged to $V_{DD}$ while nodes OutN and OutP are reset. In this phase, ideally there is no charge flow to the ground. In the whole amplification phase, the clock is high, which means the transistors M6, M7, M8, M9 are closed and M5 is conducted. The transistors M3 and M4 are conducted initially due to the potential at InN and InP. According to the boundary of whether node InP becomes static, the phase can still be divided in two subphase.

For the first subphase, the equivalent node N1 quickly gets discharged through the path provided by M3 and M5 and the similar process also happens on node P1. When the transistors M1 and M2 become conducted, the voltages of InN and InP, which is also the gate voltage of M3 and M4, begin to decrease. It causes a little potential increasement of nodes N1 and P1 because the decreasing gate voltage also influence the on resistance of M3 and M4. In addition, since $V_{inP}$ is larger than $V_{inN}$ , the discharge rate of InN and InP is not equivalent. When InN reaches the threshold value of M4, the conduction path will close, which means InP will stop to discharge and become static. For the second subphase, M4 is closed and M3 as well as M1 behaves as a cascode current source. Since M3 is fixed, node InN discharges at a reduced rate. Both Elzakker's and proposed comparator are measured at a clock rate of 25MHz. About 30% reduction of power consumption can be achieve by proposed comparator compared with Elzakker's comparator under the similar noise level.

However, the proposed circuit also brings some slight costs. The input referred rms noise of proposed circuit is $220\mu V$, which is slightly larger than the $210\mu V$ of Elzakker's circuit's. In addition, the proposed and Elzakker's circuits are produced on the same die with the standard of 65nm CMOS process and use the same regenerative latch in order to have a fair comparison. Compared with the area of $24\mu m\times 40\mu m$ of Elzakker' circuit, proposed circuits occupies 6% more area with the size of $41\mu m\times 25\mu m$. Finally, the delay of propsed circuit is larger than Elzakker's. This is because of the less effective of $V_{gs}$ and reduced initial $g_m$ of input pair, more time will be spent by proposed circuit in the region of weak-inversion and then cause higher conversion time

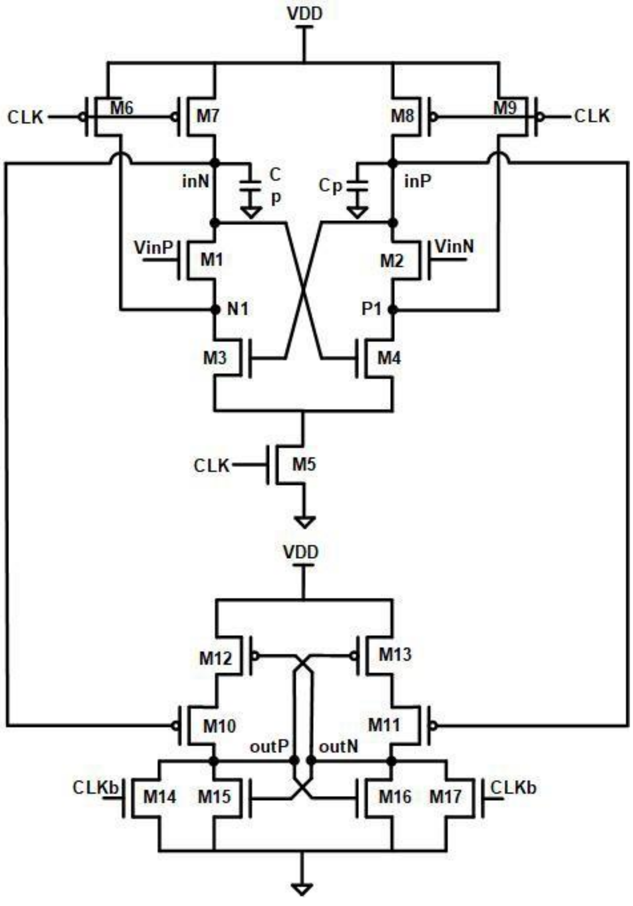


**Fig 5.** Circuit diagram of low-power 1-V supply dynamic comparator [4]

## 3. Conclusions

In this paper, a series of dynamic comparator designs that developed recently have been reviewed. Some analysis as well as some comparison between these designs are carried out. All the comparators have to face these issues, such as power consumption, noise and delay. However, the different degrees of concentration on different issues will lead to different comparator architectures and then achieve different functions. Dynamic comparators are zero in static power consumption and low delay, thereby gradually widely used in many applications over static comparators, such as data converters and portable battery- operated communication circuit. The main method for reduction of power consumption in this paper is partially discharging the input of pre-amplifier. However, the decrease of power consumption causes the increase of noise, offset voltage and area. Another example is Triple-Latch Feedforward Dynamic Comparator, which achieves much smaller delay across wide common-mode ($V_{CM}$) and supply ($V_{DD}$) range but causes a much larger power consumption. Therefore, the management of trade-off between these parameters is a vital indicator to measure whether a design is successful.

## References

[1] Yogesh Sachdeva, Nalin Nehra, Shikhar Bansal, and Garima. Review of dynamic comparators for adcs. In 2021 Second International Conference on Electronics and Sustainable Communication Systems (ICESC), pages 83–90, 2021.

[2] R. Sangeetha, A. Vidhyashri, M. Reena, R. B. Sudharshan, Sangeetha govindan, and J. Ajayan. An overview of dynamic cmos comparators. In 2019 5th International Conference on Advanced Computing Communication Systems (ICACCS), pages 1001–1004, 2019.

[3] Harijot Singh Bindra, Christiaan E. Lokin, Daniel Schinkel, Anne-Johan Annema, and Bram Nauta. A 1.2-v dynamic bias latch-type comparator in 65-nm cmos with 0.4-mv input noise. IEEE Journal of Solid-State Circuits, 53(7):1902–1912, 2018.

[4] Subhash Chevella, Daniel O'Hare, and Ivan O'Connell. A low-power 1-v supply dynamic comparator. IEEE Solid-State Circuits Letters, 3:154–157, 2020.

[5] Behzad Razavi. The strongarm latch [a circuit for all seasons]. IEEE Solid-State Circuits Magazine, 7(2):12–17, 2015.

[6] T. Kobayashi, K. Nogami, T. Shirotori, Y. Fujimoto, and O. Watanabe. A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture. In 1992 Symposium on VLSI Circuits Digest of Technical Papers, pages 28–29, 1992.

[7] Athanasios T. Ramkaj, Michiel S. J. Steyaert, and Filip Tavernier. A 13.5-gb/s 5-mv-sensitivity 26.8-ps-clk–out delay triple-latch feedforward dynamic comparator in 28-nm cmos. IEEE Solid-State Circuits Letters, 2(9):167–170, 2019.

[8] Daniel Schinkel, Eisse Mensink, Eric Klumperink, Ed van Tuijl, and Bram Nauta. A double-tail latch-type voltage sense amplifier with 18ps setup+hold time. In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, pages 314–605, 2007.

[9] Michiel van Elzakker, Ed van Tuijl, Paul Geraedts, Danie¨l Schinkel, Eric A. M. Klumperink, and Bram Nauta. A 10-bit charge- redistribution adc consuming 1.9 ¡formula formulatype=”inline”¿¡tex notation=”tex”¿μ¡/tex¿¡/formula¿w at 1 ms/s. IEEE Journal of Solid-State Circuits, 45(5):1007–1015, 2010.

[10] Harijot Singh Bindra, Chris E. Lokin, Anne-Johan Annema, and Bram Nauta. A 30fj/comparison dynamic bias comparator. In ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference, pages 71–74, 2017.