Research on the Function and Application of Some Classical Combinational Logic Products

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Abstract. Digital signals are discrete and discontinuous signals both in time and quantity. The circuits used for digital signal processing are digital circuits. Digital electronics came into being. It is a fully developed technology, through the construction and use of specific digital circuits to achieve the logical operation of digital quantities and required logical functions. Therefore, the basic characteristic of digital circuit system is logical operation and logical processing function. The main applications of digital electronic technology are combinational logic circuit, sequential logic circuit, pulse waveform generation and shaping, digital and analog conversion circuit, etc. Here only describes the practical application products of combinatorial logic circuit and sequential logic circuit, namely decoder and counter.

Keywords: Digital electronics; Combinational logic circuit; Sequential logic circuit; Decoder; Counter.

1. Introduction

Digital circuit is the basis of modern electronic technology, computer hardware circuit, communication circuit, information and automation technology. And it is also the basis of integrated circuit design. Its two main applications are combinatorial logic circuit and sequential logic circuit [1]. In asic design and pld design, the most simplified design of combinatorial logic circuit is very important. The design is often required to be implemented with minimal logic gates or wires. In asic design and pld design, it is needed to deal with a large number of constraints, but the number of items with a value of 1 or 0 is limited. Combinatorial logic circuit products can solve this kind of problem effectively [2-3]. A sequential circuit is an output that is not only related to the current input, but also to the original state of its output state. It is equivalent to adding a feedback to the input of combinatorial logic. In its circuit there is a memory circuit which can hold the state of the output. So sequential logic circuits have a memory function [4]. These two circuit products are widely used in reality and can solve many practical problems effectively [5].

The first part of this paper focuses on the 3 to 8 decoder in combinatorial logic circuit and analyzes its logic function through its truth table. Secondly, it describes the expansion of 3-8 line decoder, which can be transformed into 4 to 16 decoder. The application of decoder is briefly analyzed through some examples. The second part mainly introduces the most widely used hexadecimal and hexadecimal counters in sequential logic circuits and analyzes their functions through the state transition diagram. Compared with the real chip diagram, describe the function of each pins. Finally, based on two carry loop methods, it is analyzed in details how to extend these two basic counters into any n-carry counter.

2. Existing combinatorial logic products

2.1. Binary Decoder

Decoding is a broad concept, and it can even be considered that all decoders are products widely used in digital circuits. It also belongs to combinatorial logic circuit products. In terms of its name, most of the logic problems can be considered as the type of decoding problems. As long as the truth table is given, it will be acessible to achieve the logic setting. Due to a wide range of decoders, only binary decoders are mainly described here [6].

The logic diagram of binary decoder, also known as 3 to 8 decoder, 74HC138. And logic diagram is shown below (figure 1):

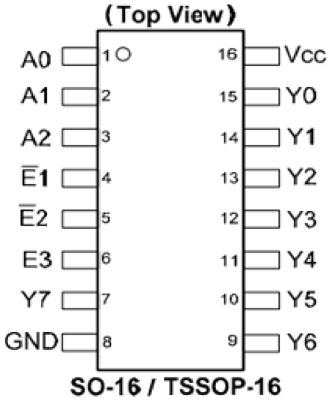

Fig 1. Logic diagram of 74HC138.

2.1.1. Origin of binary decoder

However, to get deeply understanding of the functions that the chip can achieve, it is impossible to get any useful information only by the logic block diagram [7-8]. It is needed to deeply understand the logic diagram of the chip (figure 2).

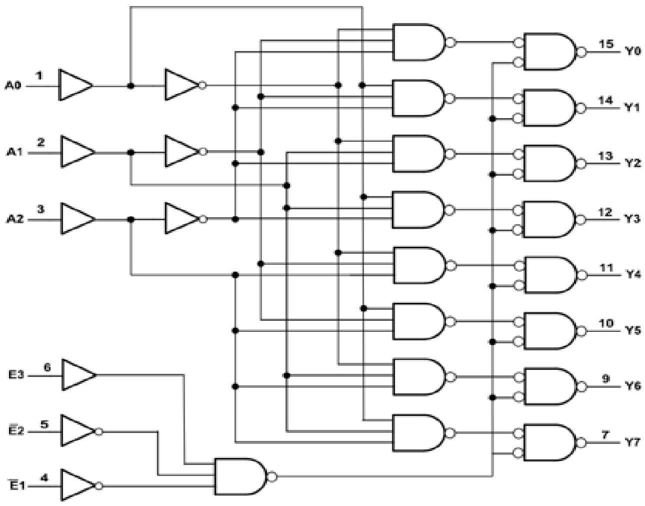

Fig 2. Logic diagram of the chip.

2.1.2. Logical function of binary decoder

It seems a little bit complicated with so many logic gates and hard to get its actual logic function. But fortunately [9], function table solve this problem efficiently, and function table is shown below (figure 3):

Control			Input			Output							
$\overline{E1}$	$\overline{E2}$	E3	A2	A1	A0	$\overline{Y7}$	$\overline{Y6}$	$\overline{Y5}$	$\overline{Y4}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	–	–	–	–	–	–	–	–	–	–	–
X	X	L	–	–	–	–	–	–	–	–	–	–	–
L	L	H	–	–	–	–	–	–	–	–	–	–	–
–	–	–	L	L	L	H	H	H	H	H	H	H	L
–	–	–	L	L	H	H	H	H	H	H	H	L	H
–	–	–	L	H	L	H	H	H	H	H	L	H	H
–	–	–	L	H	H	H	H	H	H	L	H	H	H
–	–	–	H	L	L	H	H	H	L	H	H	H	H
–	–	–	H	L	H	H	H	L	H	H	H	H	H
–	–	–	H	H	L	H	L	H	H	H	H	H	H
–	–	–	H	H	H	L	H	H	H	H	H	H	H

Fig 3. Function table diagram.

The function table is divided into two parts: truth and control.

For the truth part, the output end $\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$ indicates that the output level is low, corresponding to the minimum items $\overline{m}0$, $\overline{m}1$, $\overline{m}2$, $\overline{m}3$, $\overline{m}4$, $\overline{m}5$, $\overline{m}6$, $\overline{m}7$ respectively [10]. There are 8 and expressions composed of three logical variables A2, A1 and A0 at the input end, in which each logical variable only appears once as the original variable or the inverse variable.

And the control part is executed by three control terminals $\overline{E}1$, $\overline{E}2$ and E3. In other words, these three control terminals have both slice selection and expansion functions. Chip selection function, that is, to determine whether the chip is in the select state. If the chip selection signal is valid, the chip is selected, and then the logical function begins to be executed [11]. Otherwise the chip selection signal is invalid, the chip cannot enter the logical function state. $\overline{E}1$ and $\overline{E}2$ indicate that the low level is valid, and the signal starts to work only when E1 and E2 are connected to the low level. However, $\overline{E}1$ and $\overline{E}2$ need to be used together with E3. When $\overline{E}1$ and $\overline{E}2$ supply the low level and E3 supplies the high power level, the chip can perform the logical function. Expansion function is to use two or more chips to connect into 16-bit or more output through expansion to meet the actual demand. For the expansion of 3 to 8 decoder into 4 to 16 decoder, the implementation process is as follows (figure 4):

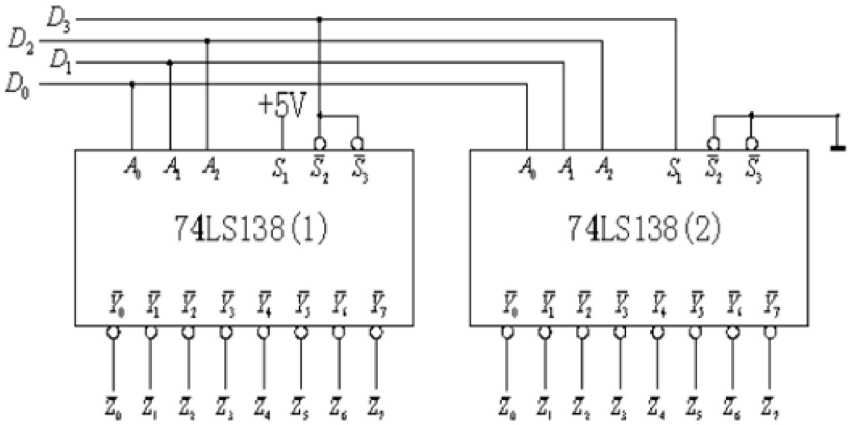

Fig 4. 4 to 16 decoder.

In the figure, 74hc138 on the left is referred to as the low level chip, and 74hc138 on the right is referred to as the high level chip. S1 in the figure is equivalent to the E3 input terminal, while $\overline{S}2$ and $\overline{S}3$ correspond to $\overline{E}1$ and $\overline{E}2$, with the same functions except for the different pin names. There are four input terminals D3, D2, D1, D0.When the highest bit D3 inputs low voltage, only the low level chip outputs Y0-Y7. At this time, the high level chip is required not to output, so D3 needs to access the high level effective control terminal S1 of the high level chip at the same time. So that the high level chip will not enter the logical function state. When D3 inputs high level voltage, the low level chip will not enter the logical function state, while the high level chip will enter the logical function state [12]. At this time, the high level chip $\overline{S}2$ and $\overline{S}3$ need to be connected to the low level voltage and the high level chip outputs Y8-Y15. D2, D1, and D0 are all connected to the input terminals A2, A1, and A0 of the low and high chip. So we can effectively output 16 different values.

2.1.3. Simple application of binary decoder

Through the previous analysis, it can be concluded that the basic principle of the decoder is that the n-bit binary decoder gives all the minimum quantities of n variables. The main purpose is to implement a set of n - bit binary decoder containing n variables and or logic functions. The use method is to combine the minimum term of the output of the N-bit binary decoder through the gate circuits [13]. It can be given that any form of combinatorial logical functions whose quantities of input variables are not greater than n.

So the 3 to 8 decoder can be used as a function generator. For example, there are three logical functions now needed to implement:

$$Y_1 = AC, Y_2 = \overline{A}\overline{B}C + A\overline{B}\overline{C} + BC, Y_3 = \overline{B}\overline{C} + AB\overline{C} \quad (1)$$

To solve this problem, firstly define: the input data A, B, C is connected to the three data input ports A2, A1 and A0 of 74hc138 decoder respectively in sequence, namely A=A2, B=A1, C=A0, At the same time, the chip selection control terminal S1 is connected to high level voltage, and S2 and S3 are connected to low level voltage. So 74hc138 decoder will output the smallest terms Y7, Y6, Y5, Y4, Y3, Y2, Y1, and Y0.

Therefore, the three logical functions of Y1, Y2 and Y3 are first transformed into the standard minimum term expression, and then can be compared with the logic function of 74hc138 decoder. The three logical functions of Y1, Y2 and Y3 are transformed into the standard minimum term expression as follows:

$$\begin{aligned} Y_1 &= AC\,(\overline{B} + B) = A\overline{B}C + ABC = \mathrm{m}_5 + m_7 = \overline{\overline{m}_5\overline{m}_7} = \overline{\overline{Y}_5\overline{Y}_7} \\ Y_2 &= \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + ABC = \overline{\overline{m}_1\overline{m}_3\overline{m}_4\overline{m}_7} = \overline{\overline{Y}_1\overline{Y}_3\overline{Y}_4\overline{Y}_7} \\ Y_3 &= \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + AB\overline{C} = \overline{\overline{m}_0\overline{m}_4\overline{m}_6} = \overline{\overline{Y}_0\overline{Y}_4\overline{Y}_6} \end{aligned} \quad (2)$$

According to the above results, connect the output ends with the gate, and the connection circuit diagram can be obtained (figure 5).

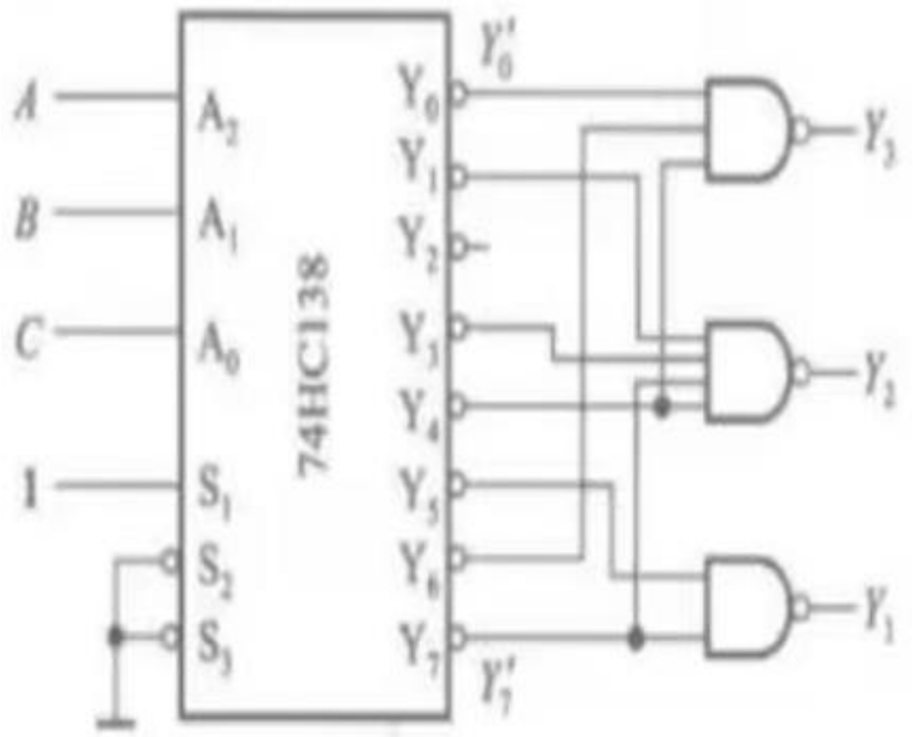

Fig 5. The connection circuit diagram.

In order to avoid the phenomenon of risk and competition which can lead to logic errors in subsequent circuits, it is not recommended to use logic gates with two or more inputs as peripheral circuits. But because of the 3 to 8 decoder, only one output is changing state at any one time. In this special case, even if two or more input NAND gates are used to make the necessary transformation, there will be no phenomenon of risk and competition [14].

2.2. Counters

Counters are the most widely used products in the sequential logic circuit, and also the most variety products in the sequential logic integrated circuit. Its basic logic function is to count the time sequence signal CLK and outputs in the way of cumulative coding. The two most basic counters 74LS161 and 74LC160 are described below.

2.2.1. Four bit binary counter (74LS161)

To investigate this counter further, it is needed to understand the state cycle diagram of the counter (figure 6). Since it is a four-bit binary counter, there is 16 counting states in a loop. Every 16 states of outputs completes a cycle, and the carry output terminal c will output a carry pulse signal, so it is also called a hexadecimal counter. The corresponding highest counting status is 1111, the carry output terminal C outputs 1, and other state output is 0.

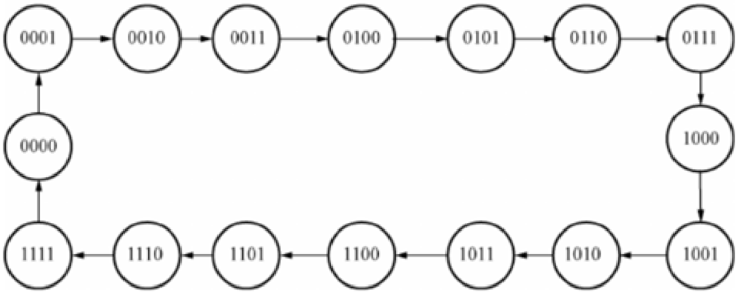

Fig 6. State cycle diagram.

2.2.2. Logical function of four bit binary counter

Figure 7 is the logic block diagram of the Four Bit Binary Counter. Because the counter is controlled by the CLK clock signal, it can only count at the rising edge of the clock signal. This state is called the active state of the clock pulse. When $\overline{R_D}$ terminal inputs a low level voltage signal, the output state will be immediately cleared to zero (Q1Q2Q3Q4=0000) ,regardless of whether the clock pulse signal is valid or not, and regardless of whether the functional state of other control ports is valid. Since the zerosetting operation is independent of the clock pulse signal, it is called asynchronous zerosetting.

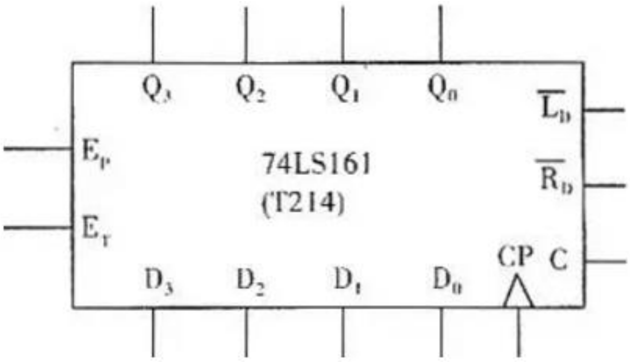

Fig 7. Logic Block Diagram of 74LS161.

$\overline{LD}$ Is the synchronous preset control terminal of the counter? When the data D3D2D1D0 of the input port needs to be loaded into the chip, just connect the $\overline{LD}$ terminal to a low level voltage signal and the $\overline{R_D}$ terminal to a high level voltage signal to realize synchronous data setting. However, when the data is set synchronously, the chip does not load the input data D3D2D1D0 immediately until the upper rising edge of the next clock pulse cycle. At the same time, the output state of the counter chip is changed to the loaded data (Q3Q2Q1Q0=D3D2D1D0). Then, when the next rising edge of the clock pulse comes, the counter starts counting with the loaded data state as a new starting point. As the preset action is controlled by the clock pulse signal, it is called synchronous preset and has nothing to do with the state of ET and EP control terminal.

Mode control voltage ET and EP are used to select and control the working state of the counter and determine whether the counter is in the hold or counting state. For ET and EP control terminals, when one of them is connected to a low level voltage signal and the other is connected to a high level voltage signal, the counter is placed in the hold state which means that it stops counting and the output state remains the same. When ET and EP are connected to the high level voltage signal at the same time, the counter enters the counting state.

2.2.3. Decimal Counter

Decimal counter is just the chip 74ls160 (figure 8). Compared with the chip 74ls161, the effective looping codes of the decimal counter is from 0000 to 1001, which corresponds to ten decimal digits from 0 to 9. Therefore, the six status codes from 1010 to 1111 are invalid states. When the state of the counter enters the invalid state due to interference and other reasons, the state of the counter should be able to enter the effective cycle and automatically restore to the valid counting state. It can also be said that it can start by itself, otherwise it will crash.

In addition, the logic function of the decimal counter is the same as that of the 4-bit binary counter, which also has two important functional terminals. One is synchronous preset terminal, and the other is asynchronous zerosetting ternminal.

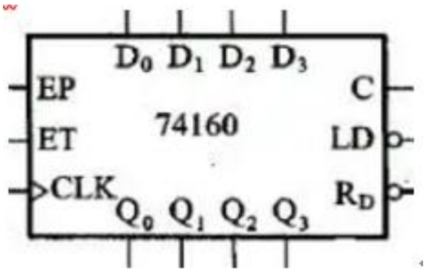

Fig 8. Logic Block Diagram of 74LS160.

2.2.4. Any N-carry Counter

If there are n-carry counter products, it is necessary to build m-carry counter. Obviously, there are two cases where M is less than N and M is greater than N.

For the first case where M is less than N. Since M is less than N, only one piece of the n-carry counter product is needed. So the number of the states of the counter product needed to be shielded equals to N-M. There are two ways to do this.

The first method (figure 9) is the zerosetting, which uses the set circuit to detect a certain target state of the counter. The counter is set zero automatically when the counter count loop outputs the target state that needs to be detected. In this way, the highest count state is, so that the number of shielded states equals to N-M.

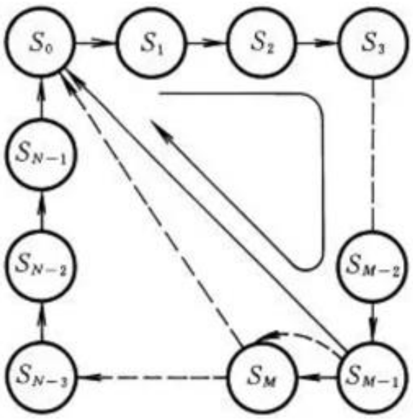

Fig 9. Zerosetting.

The existing counter products are divided into two categories: synchronous zero setting and asynchronous zero setting. If the asynchronous zero setting function is used, one more status must be detected. So it’s needed to check for state S_m. If the reset operation is initiated when only S_{m-1} is detected, the detected state S_{m-1} will have a very short residence time. Therefore the state S_{m-1} will not be counted as a valid count state. For synchronous zero setting, the status S_{m-1} needs to be checked. The zeroing operation is still automatically started when state S_{m-1} is detected, but will not be executed until the next clock effective edge arrives. This causes the state of the counter to jump back to its initial state, thus completing a cycle.

The principle of number setting (figure 10) method is similar to that of zero setting method. After detecting the target state, it automatically jumps to the state of loading data, and enters the counting cycle with the state of loading data as the new starting point. Thus, the number of shielded states equals to N-M. The difference between the two methods is that the former can conveniently preserve the highest state of the counter product, and therefore can take advantage of the carry output signal of the counter itself. The carry signal generated by the external circuit is removed.

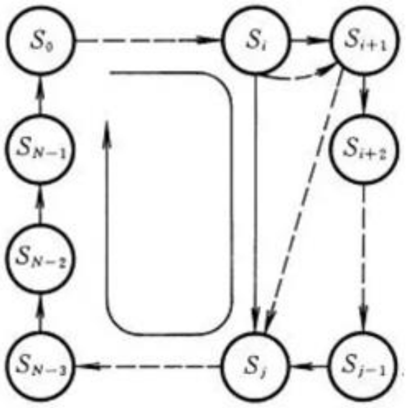

Fig 10. Zerosetting.

If M is greater than N, it can be used to combine a variety of existing base counters, and then through the zero setting method or number setting method to shield the redundant states, so as to achieve the counting requirements. However, it won't be expanded too much here.

3. Future development

With the development of science and technology, the current era has entered the information age, the development of information promotes the development of electronic technology, today, digital electronic technology has become the main force of social and economic development, and the market demand for digital electronic technology will be more and larger. Nowadays, the speed of upgrading scientific and technological information is constantly accelerating, which promotes the speed of industrial upgrading. As a result, the market demand will constantly change, and digital electronic technology needs to constantly develop to meet the needs of the market. In the process of the continuous development of electronic technology, digitalization will become the only way. Besides, electronic products are constantly being updated and replaced, and the speed of replacement is very rapid. Nowadays, large-scale programmable logic devices are widely used in digital electronic technology, which is also an important manifestation of the change. With the development of digital electronic technology, electronic design technology is also constantly changing, on the basis of electronic design automation, electronic design technology will be widely used.

Digital electronics technology has more advantages than analog electronics technology, but this does not mean that analog electronics technology is not useful. In the future, digital electronic technology and analog electronic technology should be integrated to promote the birth of new electronic devices. In the process of development of traditional electronic devices, its performance should be constantly optimized and improved. The fusion of the two is beneficial to improve the performance of traditional electronic devices and produce new electronic devices. Traditional electronic devices have many shortcomings in the process of use, such as loud noise, short life and so on. The fusion of analog electronic technology and digital electronic technology makes up for the shortcomings of traditional electronic devices and improves their performance.

4. Conclusion

Starting from the concept of electronic technology, this paper focuses on the combinatorial logic circuit and sequential logic circuit when the basic logic operation is known. The decoder in combinatorial logic circuit is widely used, so this example is selected for analysis. Starting from the truth table, the function of decoder is analyzed step by step. And explain the decoder actual chip each pin function. Finally, an example is given to solve the logic problem with decoder. Similarly, since counters are widely used and very important in sequential logic circuits, hexadecimal and hexadecimal counters are also analyzed from state transition diagrams. The function of each pin of the two chips is explained. Finally, the core describes how to implement any N base counter. After that, it briefly analyzes the future of digital electronic technology, and explains the universality of its application and the importance of its development.

So in order to adapt to the changes of The Times, it is necessary to deeply learn and understand digital electronic technology. And it can be applied to solve real life problems. Through the purchase of chips, and based on the principle some useful gate circuits can be built to achieve the specific logic functions.

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