

A Review of Design of Digital Clock Based on Verilog HDL

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Abstract. With the development of electronic technology, digital clocks have added many functions that facilitate people's lives, Digital electronic clock is a device that uses digital circuits to realize the digital display of time, minutes, and seconds. This paper mainly discusses how to use Verilog HDL to design a simple digital clock and realize the basic functions such as timing and display in the clock, as well as the platform and tools used. The circuit of the digital clock is divided into three modules, namely the frequency division module, counting module, and decoding display module. And the timing process is through the LED display, and the digital tube displays "hours", "minutes", and "seconds" which are displayed in two digits. The frequency division module divides a 50 MHz input signal to obtain a 1 Hz clock signal, and the counting time module can count and adjust the time of the clock, minutes, and seconds, and then display it on the FPGA development board through the decoding display module. After clock simulation, the system realizes the function of the digital clock and meets the design requirements.

Keywords: Verilog HDL, digital clock, frequency division module, counter module, decode display module, clock simulation.

1. Introduction

Due to the relative lack of timing accuracy of mechanical clocks and only a single timing function, the advent of digital clocks has greatly solved such problems. Not only that, but digital clocks have also added many functions that facilitate people's lives, such as school time, counting, and other functions. Digital electronic clock because of its long-term stability and low energy consumption, has become one of the indispensable necessities in people's lives and is widely used in residential, offices, and other living places. Digital integrated circuit technology in recent years rapid expansion and quartz crystal oscillators are also used in more areas of reason, digital clock timing and display time accuracy compared to the old clock has a qualitative leap. [1] People have to admit that the digitization of clocks and watches can greatly avoid some unnecessary troubles in our production and life, and digitalization has also made the timing function of the original clock form one have more beneficial functions [2].

This paper mainly discusses how to use Verilog HDL to design a simple digital clock and realize the basic functions such as timing and display in the clock, as well as the platform and tools used. The circuit of the digital clock is divided into three modules, namely the frequency division module, counting module, and decoding display module [3] and the timing process is through the LED display, and the digital tube displays "hours", "minutes", and "seconds" which are displayed in two digits. Verilog HDL method can be used to realize the design process of digital circuits. The digital clock cannot only display the time but also complete simple functions such as time checks and alarms [4].

2. Basic application methods and different design analysis

2.1. Circuit theory

A basic digital clock needs to have the timekeeping and display function of time, accurately presenting the current time, including hour, and minute-second information corresponding to the time to the user. The digital electronic clock is actually a counting circuit that counts at standard 1Hz. The minute counter is charged after the second counter is full of 60, the hour counter is charged after the minute counter is 60, and the hour counter is turned to 1 by 24 or 12 regular countings. The output via the decoder is sent to a digital tube display. Over time, the digital clock completes a digital runout every second, which enables the flip of the hour, minute-second signal. Therefore, a simple digital clock can be divided into at least three modules: the divider module; the counter module for minutes, seconds, and hours; display and control module. However, since the starting time of the count cannot be consistent with the standard time, it is necessary to add a calibration circuit to the clock system, as shown in Figure 1 is a block diagram of a multifunctional digital electronic clock commonly found on the market.

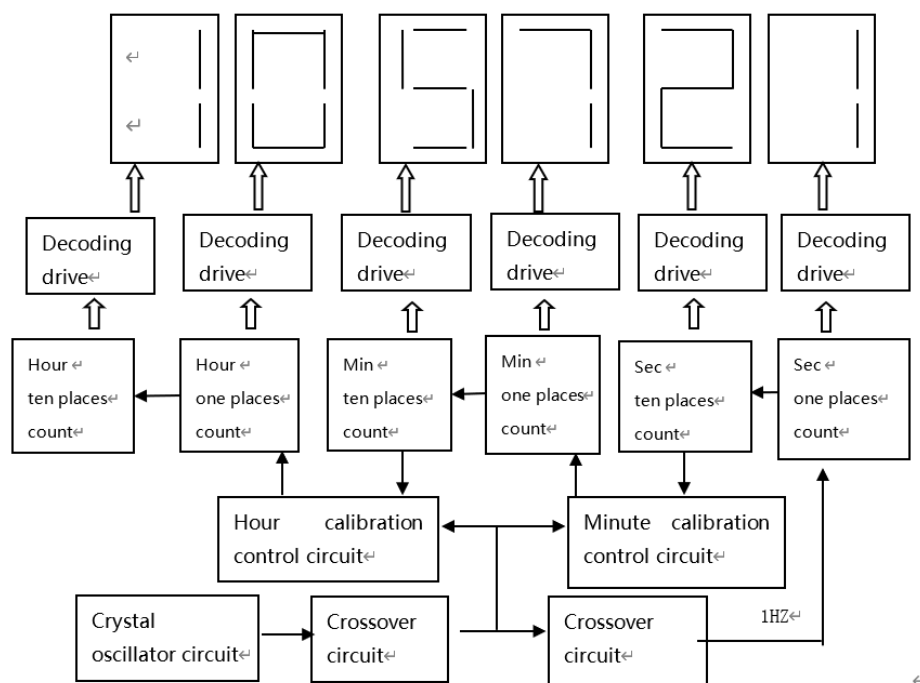


Figure 1. Block diagram of a multifunctional digital electronic clock.

2.2. Introduction to the tool platform

Verilog HDL, the most widely used hardware description language in FPGA design, is simple, efficient, easy to learn, and powerful, and is suitable for RTL level and gate circuit level description. [3]. Compared with other methods, such as the PCB programming method, it avoids the drawbacks of a cumbersome construction process and difficulty in effectively layout lines. Verilog HDL programming language has the characteristics of easy operation and strong visualization. This language cannot only get most devices compatible, generating the design of the clock product, but also appropriately optimizing the circuit resources. When there is a design and use of different modules, it can also flexibly set pulses, and through the relevant equipment achieve simulation.

Quartus II is a very advanced EDA software developed by Altera for CPLD/FPGA. It has two kinds of simulation functions: functional simulation and timing simulation. It not only supports Verilog and other program input functions but also has a digital circuit schematic input function. In addition, Quartus II is well suited to be used in conjunction with other EDA simulation tools because of the interface connecting the three parties. [4].

The process for developing a digital system with Quartus II software is shown in Figure 2.

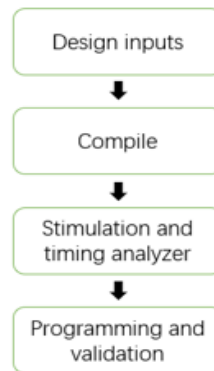


Figure 2. The process for developing a digital system with Quartus II.

ModelSim, a widely used simulation software in the industry, was developed by Mentor Graphics. It can complete the function simulation of the hardware description language code independently, and can also combine the FPGA/CPLD development software to carry out the timing simulation and get the results including the timing of signal transmission. At the same time, the System C and C language can be debugged and simulated and the design process can take many flexible means to complete the design work, most FPGA/CPLD supplier software provides an interface with ModelSim. Fast compilation simulation, cross-platform, and cross-version simulation make it a preferred simulation software for FPGA/ASIC design.

2.3. Analysis of different design methods

2.3.1. Design study of Verilog HDL digital clock circuit

In 2021, Guanlin Li and Baoling Zhang proposed the design process of implementing a digital clock circuit in the Verilog language, so that the circuit automatically implements various functions related to time. The digital clock system designed is divided into four modules, namely the timer module with a frequency of 1 Hz, the time calibration module, the alarm module, and the countdown module, different modes can be converted by the clock's button conversion operation, if the corresponding function is not selected by the user, the expected purpose can be achieved by repeated keystrokes; And when the corresponding button is pressed, its function will be displayed on the screen. The application of the Verilog HDL programming language to the design of digital clock circuits can improve the functionality and practicality of digital clock circuits [3].

2.3.2. FPGA-based digital clock design

In 2022, Huang Mingxia and colleagues designed a digital clock with counting and timing functions, counting in a cycle of 24 hours. By using the Verilog HDL hardware description language to design digital clocks, through a top-down approach in the Quartus II development environment. The design mainly includes three parts: frequency division module, counting and calibration module, and decoding display module; The frequency division module divides a 50 MHz input signal to obtain a 1 Hz clock signal, and the counting time module can count and adjust the time of the clock, minutes, and seconds, and then display it on the FPGA development board through the decoding display module. After the simulation test of each module by Modelsim, the system basically realizes the function of the digital clock and meets the design requirements. The study found that Verilog HDL was independent of specific circuits and could significantly improve design efficiency under the Quartus II development environment [5].

2.3.3. Simple digital electronic clock design

In 2021, Yuxing Li designed a simple digital electronic clock, consisting of a second pulse signal circuit, hours, minutes, seconds counting circuit, and decoding display circuit, with the use of 555 timer generation frequency rate and the 74LS192 chip control minutes and hours [6]. Also, a CD4511 core piece for decoding display, while with a variety of logic gates to achieve different functions. The design was simulated using Proteus.

2.3.4. Digital clock design based on the VHDL

In 2011, Xiaomin Li and Xiyan Tian applied the VHDL language and adopted the top-down design idea to design the digital clock system using the sub-module design method. Then they simulated it under the Quartus II environment and completed the 24 h timing and auxiliary function design, which demonstrated the powerful circuit description ability of the VHDL language and the advanced nature of EDA technology [6].

3. Specific analysis and innovation based on Verilog digital clock

3.1. Detailed analysis of digital clock module

The frequency division module (as shown in Figure 3) is used to obtain the clock frequency required by the group. The input signal of the frequency division module depends on the clock signal provided by the development board. In this design, the crystal frequency selected by the team members is 10 KHz, but the counting period required by the counting module is 1 second, so it is necessary to divide the clock signal from 10 KHz to 1Hz [7]. In addition, in order to make the blinking effect of the dynamic nixie indistinguishable from the human eye, the decoding display module also needs a scanning frequency. The design of this group is to use the fundamental frequency of 10 KHz as the shift scanning frequency of the dynamic nixie tube.



Figure 3. Schematic diagram of the frequency divider.

The flow chart of the frequency divider is shown in Figure4.

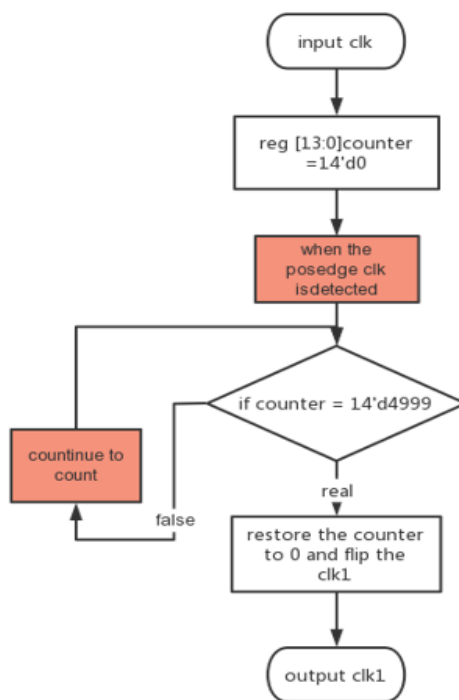


Figure 4. Flow chart of the frequency divider.

As to the counter module, the essence of a clock is composed of several counters with unique bases. The second low and minute low are modular ten counters, the second high and minute high are modular six counters, the time low is modular four counters, and the time high is modular two counters. In order to simplify the design, the team members designed the timing module (as shown

in Figure 5) as a modular 60 counter and a modular 24 counter. "Seconds" and "points" and "when" between independent and interconnected count and rounding, namely, seconds count mode is 60 reset[8], given a carry signal, counter carry signal starts counting, 60, also give a carry signal, hour counter received carry signal began to count, with 24 reset as shown in Figure 6 [9].

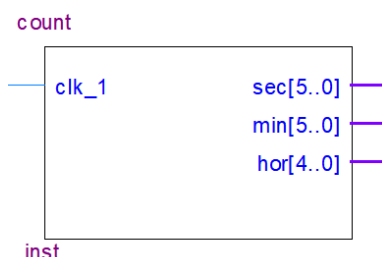


Figure 5. Counter schematic diagram.

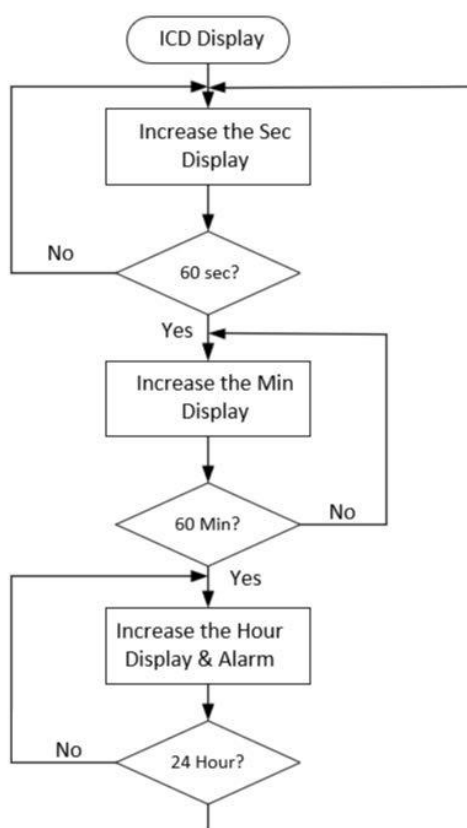


Figure 6. Counter flow chart of this design.

The decode display module (as shown in Figure 8) contains both decode and display functions. The digital clock's seven-segment digital tube is generally composed of eight light-emitting diodes and displays the numbers by dynamic scanning. In the seven-segment digital tube, as shown in figure 7, each segment of light-emitting diodes has a fixed letter to indicate such a combination can indicate 0-9, as well as A, B, C, D, E, F a total of 16 characters, as well as a light-emitting diode, constitutes a decimal point that can be spaced to indicate the number of digits. Therefore, using a combination of multiple light-emitting diodes can represent the common numbers.

The input signals "hor, min, sec" are the binary representation of hours, minutes, and seconds, according to the display principle of the digital tube, it is necessary to convert these three signals into BCD code and separate the ten bits from the individual bits, so that they can be displayed on the corresponding digital tube. Define "led_dis" as the segment selection signal and "led_SEL" as the bit selection signal. "led_SEL" changes the corresponding digital tube when the rising edge of the clock signal "clk" is detected, at which time the register variable temp corresponds to the corresponding second digit, second decimal, minute decimal, minute decimal, hour decimal, hour decimal, which is

too fast to be recognized by the human eye due to the change frequency, thus achieving the effect of the static display. When a change in the register variable temp is detected, disp_code assigns the corresponding segment selection number.

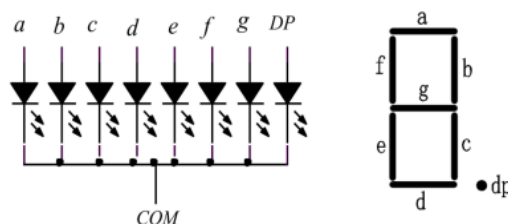


Figure 7. The display schematic diagram of the seven-segment digital.

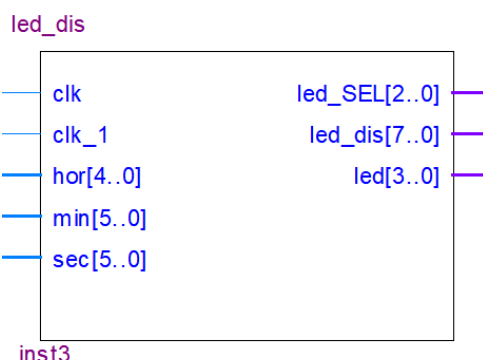


Figure 8. The schematic figure of the display decode module.

3.2. Clock function analysis

This experiment designed a simple digital clock that can achieve hours, minutes, and seconds of timing and display. The counting principle is that when the second count is over 60, a carry to the minute is generated, and when the minute count is over 60, a carry to the hour is generated. These two carry signals relate to the hour, minute, and second. The counting signal comes from the clock signal provided by the development board. The crystal frequency used here is 10 KHz, and the counting period of seconds is 1 second. Therefore, the clock signal needs to be divided into frequencies (10KHz→1Hz). The timing process of "seconds", "minutes" and "hours" all need to be displayed through the LED display.

3.3. Instance Verification

Waveform simulation is an important way to verify the experimental results. Figure 9 shows the functional simulation waveform of the counting module. The waveform shows that when the minute count reaches 59 it reverts to 0 and generates a feed. Figure 10 shows the clock signals input to the top-level module, and the segment and bit selection signals corresponding to each digit output. In addition to this, the digits after the separation of the digits from the tens are shown in the waveform graph, correctly matching the signals sec, min, and hor. Up to this point, this design achieved the function that is expected.

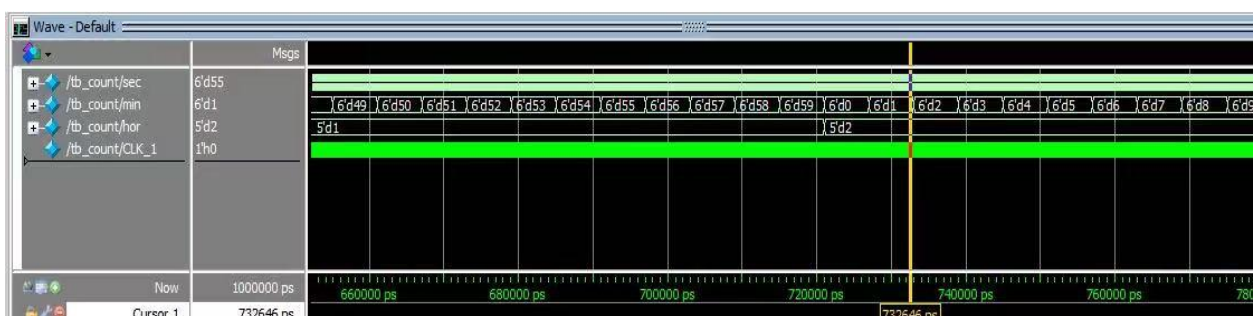


Figure 9. Simulation results of counter module.

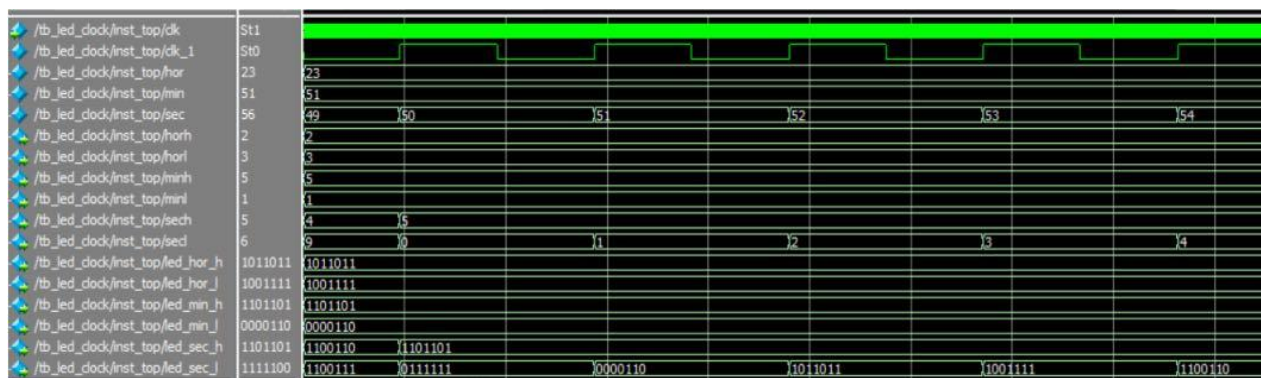


Figure 10. Clock simulation results.

4. Challenges and prospects

4.1. Facing challenge

Through the above expressions, it is of great significance to the development of digital clocks to study digital clocks and increase their functions. However, there are still defects in the current digital clock technology at home and abroad. For example, most of the LED digital clocks used on the market are implemented with full hardware circuits. The circuit is not only complicated in structure, but also has huge power loss. The cost is huge. From the perspective of human health, because electronic clocks are electronic products after all, and electronic products have radiation, the harm of electronic clocks is extremely low. Therefore, our current priority is to study how to simplify complex circuits and reduce manufacturing costs. At the same time, many related problems are actually caused by the indirect number of hardware circuits. The loss of hardware is large. In the future, we will consider reducing the hardware as much as possible, and use other technologies to support its functions after the hardware is reduced, which will also reduce the failure caused by the hardware. Probability. Therefore, in the environment, people need to actively cultivate talents in this area, and digital clocks also need people to actively improve, discover, and create new and better design methods [10].

4.2. Outlook

From the sundial invented in ancient times to the appearance of mechanical clocks and clocks, and then to the development of digital clocks, it marks that people continue to enter a new stage of historical development.

Due to the vigorous development of science and technology, electronic technology has continued to step into new heights of development, digital clocks have been gradually updated, greatly improving the accuracy of timekeeping, and the sun also has some other functions. With the improvement of the level of digitization and people's living standards, the basic functions of digital clocks are far from meeting people's requirements, which promotes the gradual diversification and intelligent development of digital clocks.

Therefore, when human scientific and technological civilization continues to develop toward intelligence, people's requirements for clocks are also constantly improving. The clock has not only been regarded as a tool used to display time, but in many practical applications, it also needs to be able to achieve more other functions. High precision, multi-function, small size, and low power consumption are the trends in the development of modern clocks. Under this trend, the digitization and multi-functionalization of clocks have become the dominant design direction of modern clock production research.

With the continuous improvement and beautification of people's living environment, digital electronic clocks are seen on many occasions. It has become a fashion to use 1cd digital electronic clocks in public places such as major business places, stations, and docks in the city. However, many living areas like cultural industries, family life, industrial office areas, and factories still use some

large-scale electronic mechanical clocks with a small number, single functions, and inaccurate and inconvenient readings. Habit, on the other hand, because most of the various LCD digital electronic clocks on the market are implemented with full hardware circuits, the circuit structure is complex, and the power loss is large. Therefore, it is necessary to improve the digital electronic clock in these aspects to better adapt to people's usage habits, so that the convenience and accuracy of the digital electronic clock can be better popularized and applied. Many related problems are actually caused by the indirect number of hardware circuits. The loss of hardware is large and the cost is also high. In the future, we will consider reducing the cost of hardware as much as possible, reducing hardware, and using other technologies to maintain its functions after hardware reduction. The probability of failure due to hardware will be reduced. Not only that but since there are multiple languages in the world, digital clocks can also be researched and designed in different languages to display time and other intelligent functions [11].

5. Conclusion

Through this experimental design, we have a good grasp of the basic process of using Verilog HDL to design a simple digital clock, the theoretical principles of each module, the clock signals involved in digital timing, and the meaning displayed in each position of the final simulation graph, and learned the basic usage of Verilog. At the same time, in the design process, the frequency division module, the counting module, and the decoding and display module also play an important role. Through these three modules, the timing and display of hours, minutes, and seconds can be realized. During the timing process, two a carry signal, which is carried to "minutes" when the seconds exceed 60, and to "hours" when the minutes exceed 60. Through this experiment, we can master the use of Verilog and the design methods and processes of digital clocks, laying the foundation for subsequent innovation and new functions. The next step of the digital clock should focus on designing new and more convenient functions, and strive to improve people's quality of life in this regard.

Digital clocks are more and more needed in people's lives, but today's digital clocks still lack the diversity of functions and the compactness of appearance, so our research and design of digital clocks are to learn more about the basic knowledge, principles, and design of digital clocks. Process, which is conducive to learning more relevant knowledge in the future, can have a good foundation and more novel ideas, and it is easier to create new functions.

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