High-Performance Monolithic Integration of III-V QD Lasers on Si Substrates

Jun Li*

Department of electronic & Electrical Engineering, University College London, London, UK

* Corresponding Author Email: ucaqlis@ucl.ac.uk

Abstract. With the development of digital processes, the speed and efficiency of information exchange has increased to a great extent. Silicon-based photonics allows for large-scale photonic integration through CMOS manufacturing processes, the advantages of which lie in the low cost, low energy consumption and high quality of such processes. Currently, silicon-based monolithic integrated quantum dot lasers have achieved lifetimes comparable to those of heterogeneous integrated lasers and are even available for commercial applications. The silicon photonic platform also offers low-loss passive devices, as well as high-speed optical modulators and photodetectors. However, device performance suffers due to differences in physical properties between group III-V lasers and substrate materials, an important factor limiting the development of silicon-based monolithic integrated quantum dot lasers. This paper reviews the respective characteristics of silicon-based monolithic and heterogeneous integration. The advantages of monolithically integrated III-V quantum dot lasers over heterogeneous integration are highlighted, as well as the challenges, solutions and recent developments.

Keywords: Quantum-dot laser, photonic integrated circuits, silicon.

1. Introduction

In recent years, with the rapid development of Internet data exchange, optical integrated circuits (PICs) are new devices used to integrate semiconductor lasers, optical multiplexers, optical waveguides, optical detectors, etc. onto a single silicon-based chip [1]. In addition, Silicon makes improvements to the commercial application of optical modules due to its inherent cheapness and complementary metal oxide semiconductor (CMOS) compatibility [1]. However, Si-based lasers have been considered the biggest challenge because Si bulk materials have an indirect band gap and very low radiation efficiency [2]. Although Si Raman and Ge-alloy (GeSi and GeSn) lasers have the potential to integrate devices in the Si platform, their practical applications are limited. In contrast, III-V materials exhibit good optoelectronic properties when used as active components in PICs and have more potential as Si-based platform lasers.

QW lasers have been shown to have good advantages, especially in modulation speed. However, the disadvantage of QW lasers is that their threshold currents are very sensitive to temperature. When the temperature rises, the threshold current drop significantly. In contrast, QD lasers are less sensitive to temperature and still perform better at high temperatures, especially when applying p-type modulation. Deppe et al. achieved fast modulation of more than 30 Gbps in the QD field by using p-type modulation doping [3]. In addition, Sugawara et al. achieved 10 Gbps of temperature-independent operation and 25 Gbps of direct modulation at a QD laser speed of 1.3 μm. Therefore, III-V QD lasers are considered an ideal laser source for silicon-based PICs, and the lack of silicon-based PIC lasers can be solved by directly growing or transferring III-V lasers on Si platforms

External optical feedback (EOF) includes phenomena such as narrowing of linewidth and increased phase noise, all of which have a negative impact on the performance of the device. QDs have proven to be better tolerant compared to QWs when dealing with optical feedback due to their high damping coefficients. Figure 1 shows the RF spectra of the QD and QW lasers. The RF spectra show different intensities at different feedback intensities. Compared to QD, QW appears to have a greater broadening in the optical mode. Also, no anomalies were found in the QDs laser in the RF mode, while strong non-linear vibrations appear in the quantum well laser, indicating that the inner cavity of the quantum well laser is disturbed. The above results demonstrate the higher immunity of QDs compared to QWs in response to optical feedback.

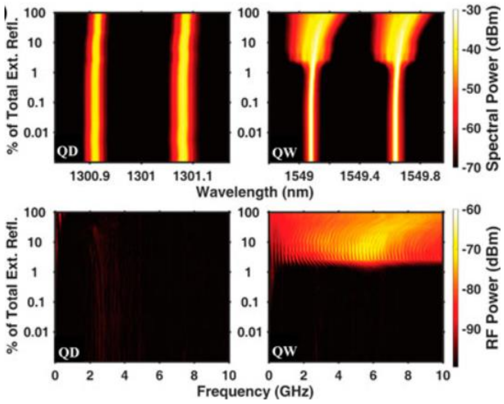

Fig. 1 Optical spectra (Top) and RF spectra (Down) of QW and QD lasers under feedback strength at 3×Ith [1]

2. Monolithic Integration of III-V Lasers on Si Substrates

Compared with the fruitful achievements of silicon-based photonic technology in passive waveguide devices, modulators, and detectors, on-chip silicon-based light sources still lack mature solutions.

The poor fluorescence efficiency of silicon due to its direct forbidden band nature has made it a great challenge for silicon materials to be used to prepare into highly efficient fluorescent devices. Scientists now have a better understanding of the silicon luminescence mechanism, luminescent materials and device structures. Materials such as silicon-based Raman lasers, nano-Si luminescent materials, silicon rare earth doped luminescent materials, and luminescent materials of germanium/storage selenide have been further studied or even achieving excitation over the years, and their luminescent properties have been further improved. However, the performance of these light sources is still a certain gap compared with III-V lasers[3]. Therefore, the current relatively mature silicon photonic on-chip light source program is mainly based on III-V materials, through certain integration means on the silicon photonic chip to achieve the production of III-V material lasers.

Light sources on silicon are divided into two categories based on different integration methods: the first is heterogeneous integration and the second is monolithic integration. The difference between the two is that heterogeneous integration means that the laser or its gain material is indirectly grown and fabricated on silicon, and the integration of this type of light source usually involves the transfer of the laser onto a silicon photonic chip using a specific process. In contrast, monolithic integration uses a more optimised process than heterogeneous integration, avoiding tedious steps such as transferring the laser and growing a specific material directly on silicon as the gain medium for the laser. Heterogeneous integration technology has been refined over the years and is now well established, both in terms of process and product quality. However, the disadvantage is that the steps in this integration method are too cumbersome and costly, which poses certain challenges for large-scale integration. Monolithic integration has been slower to develop than heterogeneous integration, mainly because the light source performance of monolithic integration is not high enough. However, monolithic integration is a simpler and cheaper process step and, more importantly, monolithic integration is more supportive of large-scale optoelectronic integrated circuits and is considered to be the best solution for light sources on silicon photonic chips [4].

2.1. Heterogeneous Integration

The heterogeneous integration technology of semiconductor chips contains mainly the direct mounting technology and the wafer bonding technology of semiconductor chips. The direct assembly technology involves the heterogeneous integration of the light source and the silicon-based optical wafer by soldering a pre-prepared III-V laser to the silicon-based optical wafer via a solder ball and electrically connecting it to the silicon-based optical wafer. A silicon photonic transmitter chip without temperature control was designed by Tanaka et al. using high-precision flip-flop soldering equipment to integrate a semiconductor optical amplifier (SOA) of group Il-V material onto a silicon-on-insulator (SOI) substrate [4]. They aligned it with the waveguide end face to form a heterogeneous integrated laser together with the SOI waveguide, as shown in Figure 2. The use of flip-flops helps make the design of silicon optical devices and SOAs more flexible, and also provides better thermal conductivity for SOAs. However, end-coupling places high demands on the accuracy of flip-flop soldering. Therefore, although the flip-flop soldering technology is more mature and can fully utilize the optical gain characteristics of Kaw-V group materials, the high alignment accuracy requirement leads to a higher process cost.

Wafer bonding is the light source integration technology that is expected to be the highest among the current heterogeneous integration solutions. Using wafer bonding technology, one can integrate the epitaxial layer of III-V material on top of silicon optical devices such as silicon waveguides, and the light generated by III-V material can enter the silicon photonic circuit by means of swift wave coupling, completing the heterogeneous integration of light sources and silicon photonic chips.

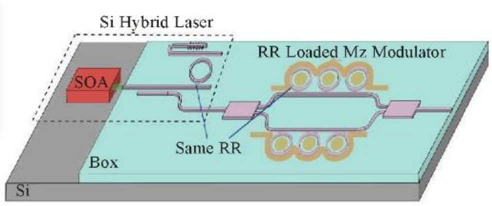

Fig. 2 Conceptual structure of proposed Si transmitter for operation free of temperature control [4]

2.2. Monolithic Integration

Monolithic integration is a method based on the epitaxial III-V type on silicon-based semiconductor heterogeneity. The monolithic integration process, whose greatest advantages over traditional heterogeneous integrated light sources are compressible linewidth and increased integration in parallel with the silicon photonic process, is expected to become the mainstream of future silicon-based photonics.

Heterogeneous epitaxial III-V material on silicon is the most attractive solution for silicon photonic monolithic integrated light sources [5]. Epitaxy of III-V materials directly on silicon is expected to apply the process and technology of native III-V material photonic devices to silicon photonic light sources to obtain excellent performance on-chip light sources. The problem faced by the heterogeneous epitaxy technology is mainly lattice mismatch of Group III-V substances with silicon, which will lead to the formation of defects. Dislocations and anti-phase domains are two typic defects that severely limit the lifetime and performance of III-V lasers. For dislocation defects, a dislocation blocking layer or other buffer layer structure can be added between the substrate and the active region in the growth to reduce the penetration dislocation (TD) density and its penetration depth. The buffer layer does not provide effective filtering for anti-phase domain defects. Epitaxy of III-V materials on patterned silicon substrates using selected growth techniques can effectively limit the impact of antiphase domain defects on the active region.

Monolithic integration of Group III-V compounds on Group IV substrates to form semiconductor materials can be achieved by using molecular beam epitaxy (MBE), and chemical vapor deposition (CVD), etc. [1].

3. Existing Problems and Solutions

3.1. Crystal Defects

Monolithic integration is not perfect. The problem lies mainly in crystal defects arising from dissimilarities when different III-V materials are grown on Si substrates. These defects can evolve into non-radiative composite centers and shunt paths that affect the device's performance. The main challenges of monolithic integration fall into three main categories: anti-phase domain (APD) and anti-phase boundaries (APBs); threaded dislocation; and thermal cracking. The reason for these challenges, as mentioned above, is due to the different physical properties between group III-V and group IV materials. First, the generation of APD is related to the polarity of the material, which can also lead to the generation of substantial amounts of APD. Secondly, the difference in physical properties between the III-V group and the Si substrate can create a lattice mismatch that can lead to the creation of high densities of line dislocations — up to 4% between GaAs and Si substrates, for example [2]. Finally, the misalignment of the coefficient of thermal expansion during epitaxial material cooling can lead to the generation of microcracks.

Nowadays, scientists have applied many methods to reduce the defect density to create monolithically integrated lasers with longer and more stable performance. The most common method of reducing the number of APBs is to use mis-cut silicon substrates that has a slight 4° - 6° offset from the (001) direction [1]. In this case, high-temperature annealing treatment can achieve a single-atom step to a two-atom structural reconstruction on a miscut Si substrate with an offcut angle, thereby suppressing the generation of APB. However, the resulting drawback sacrifices their CMOS compatibility. In the standard CMOS process, the offset angle of the silicon substrate should not exceed 0.5°. At the same time, the use of transition layers such as Ge, GaP and GaAs as well as patterned silicon substrates (V-slot Sid) is expected to lead to APB-free III-V band devices on silicon substrates. In both reactions, metal organic vapour deposition (MOCVD) will necessarily be involved—especially for QD laser growth, making the fabrication procedure more complex while increasing the cost. Meanwhile, these thick buffer layers can correspondingly lead to the formation of thermal cracks and produce a low yield in devices. Strain layer superlattices (SLSs) can prevent TD propagation by lateral bending and are often used as a method to reduce thread dislocation density (TDD) [6]. At the same time, the thermal cyclic heat treatment is able to provide energy for the process, thus accelerating the rate of reduction in threaded dislocation density (TDD). To solve the problem of thermal cracking, reducing the total thickness of the epitaxial layer, such as replacing the epitaxial layer material, is an effective method. Also, reducing the density of the defect by reducing the crack nucleation point will also provide great help. However, in III-V/Si lasers, a thick buffer layer is essential. Apart from that, the engineering of strain profiles, the growth of the selective area, and the method of growth on deeply patterned Si substrates can also be effective in reducing thermal cracks. Table 1 summarises the challenges mentioned above and the solutions commonly used.

Table 1. The current challenges and solutions of III-V type active materials on Si monolithic integration

Challenge	Method
Anti-phase domain (APD) and anti-phase boundaries (APBs)	1. Use a slight 4°–6° offcut angle from the (001) orientation. 2. Use of buffer layers. 3. Use of patterned Si substrate.
Threaded dislocation (TD)	1. Thermal cycle annealing. 2. Use of buffer layers. 3. Use of SLSs as dislocation filter layers (DFLs). 4. Growth of an III-V nucleation layer.
Thermal cracking	1. Reduction of the total thickness of the epitaxial layer. 2. The engineering of strain profiles. 3. Selective area growth (SAG) [3]. 4. Use of deeply patterned Si substrates.

3.2. Thick Buffer Layer

There are great crystal mismatches, thermal expansion and inhomogeneities in the Si and III-V systems, which lead to linear dislocations, thermal cracking, and reversed phase regions. In the past, III-V buffers above 2 microns were mainly used to reduce the concentration of TD and thus effectively suppress the transmission of APB. However, the high III-V semiconductor material is highly susceptible to thermal cracking due to the thickness of the silicon substrate of the III-V semiconductor material being greater than 5 microns [7]. Thermal cracking in silicon-based III-V laser devices can seriously affect the output efficiency of the device. Therefore, reducing the size of the III-V buffer layer is a key part of achieving fully integrated III-V silicon-based. Measures commonly used to reduce the buffer layer include replacing a thicker GaAs buffer layer with a thinner Ge layer, thereby reducing the total buffer layer. The TDD in the film can be reduced by using a heat treatment process at a high temperature so that the measured critical current concentration of the laser at a pulsed operating state is 200 A cm^{-2}, which is comparable to 28.6 A cm^{-2} for each quantum dot [1].

3.3. Slope Efficiency

Direct preparation of quantum dot lasers on microelectronic standard precision (001) Si substrates is critical in order to meet the requirements for compatibility and integration with COMS technology. In order to achieve direct laser growth, there are two important avenues to be addressed. The first objective is to obtain a high precision laser with an error of less than 0.5° on a precision (001) silicon substrate. The second involves on patterned Si substrates [8]. Quantum dot laser devices and AlGaAs melt layers can be prepared using molecular beam epitaxy (MBE) using high precision single crystal silicon (001) as a substrate. However, the molecular beam epitaxy technique is deficient in the epitaxy of lasers on planar precision silicon (001) substrates and needs to be improved. First, the lack of hydrogen atmosphere prevents MBE from performing the hydrogen annealing process, which prevents APD on Si substrates from being suppressed. Second, growing phosphorus-containing materials, such as GaInP layers, is also difficult. Finally, the optically integrated structures suffer from the poor quality of regenerative or selective region growth. Wang et al. combined the advantages of MBE and MOCVD to grow accurate Si (001) templates and GaInP on the melt cladding using MOCVD, and extruded the APD using hot hydrogen annealing with a thinning buffer of GaAs/Si (001) templates, which achieved high slope efficiency.

4. Review of Research Progress

QD has been proven to have superior performance and optimized growth strategies for lasers. High-performance Fabry-Perot (FP) and distributed feedback (DFB) lasers grown on Si platforms have been reported in the literature in the past and have been shown to have excellent performance—even comparable to that of devices grown natively on III-V substrates. Also, mode-locked edge-emitting lasers grown on Si substrate has proven to be a device with development potential. The wavelength range in which FP lasers operate is concentrated in the O-band, due to the use of InAs/GaAs QDd. In fact, C-band operation which is based on the InP is very important as it affects medium/long range communications, but progress on Si for 1.55 μm QD lasers has been difficult to break through due to the hindrance of lattice mismatch. Wang et al. achieved the first monolithically integrated indium phosphide thin-film DFB laser device on a Si substrate at Ghent University, UK, in 2015. In 2016, Wang et al. fabricated silicon-based O-band QD DFB arrays by employing selective area growth techniques to improve on previous preparation techniques. However, these devices are still limited by wavelength, mainly because such lasers are small wavelength coverage. Also, optical pumping can have a negative effect on them. In 2018, for the first time, a monolithically integrated array of electrically pumped InAs/GaAs quantum dot DFB lasers was shown on a silicon substrate, which was jointly fabricated by scientists from the University of London, UK, and Sun Yat-sen University, China. In this work, the array of six devices exhibited a high side-mode suppression ratio

(SMSR) of 50 dB, O-band wavelength coverage of 100nm and a channel spacing of 20nm, meeting the requirements of commercial WDM systems. However, the drawback is that the thicker buffer layer affects the CMOS compatibility of the laser and the growth of thermal crack density while increasing the difficulty of light source deployment [1].

Silicon-based microscale and nanoscale lasers have also gained momentum in recent years due to their potential applications in optoelectronic integrated circuits. So far, scientists have successfully demonstrated monolithic hybrid integration of microring and microdisk lasers on Si. However, the integration of micro/nanoscale lasers with other electronic devices is one of the important issues that need to be addressed [9, 10].

5. Conclusion

This paper reviews the characteristics associated with monolithically integrated III-V QD lasers and heterogeneously integrated lasers based on silicon platforms and highlights the progress made in monolithic integration. Overall, silicon-based edge-emitting lasers have matured sufficiently over the years to meet the needs of silicon photonics for off-chip light sources. Recently, monolithically grown III-V QD lasers on silicon substrates have made great breakthroughs, such as long lifetime, high output power, etc., which indicate that QD lasers are superior to QW lasers. In addition, the single-device performance of monolithic integrated lasers has been accomplished beyond compared to heterogeneous integrated devices and is expected to completely replace heterogeneous integrated devices in the future. However, factors such as crystal defects, relatively thick buffer layers, and difficulty in controlling the slope efficiency make it more difficult to couple light to an insulator-on-silicon waveguide. Although the approach of using lasers as on-chip light sources still has a long way to go, the emergence of silicon-based III-V QD lasers makes III-V/Si integration more practical, it can be believed that in the future, more integrated, better performing, and lower-cost silicon-based optoelectronic integrated chips will emerge and be used in communication, sensing, and other fields.

References

[1] Cao V, Park J-S, Tang M, Zhou T, Seeds A, Chen S and Liu H (2022) Recent Progress of Quantum Dot Lasers Monolithically Integrated on Si Platform. Front. Phys. 10: 839953.

[2] Bin Tian, Zhechao, Philippe Absil, Joris Van Campenhout, et al. Room Temperature O-band DFB Laser Array Directly Grown on (001) Silicon. Nano Lett. 2017, 17, 1, 559–564.

[3] Siming Chen, Mingchu Tang, Qi Jiang, Huiyun Liu et al. InAs/GaAs Quantum-Dot Superluminescent Light-Emitting Diode Monolithically Grown on a Si Substrate. ACS Photonics 2014, 1, 7, 638–642.

[4] Huang Beiju, Zhang Zan, Zhang Zanyun et al. Research progress on silicon-based optoelectronics and microelectronic monolithic integration. Micro- and nanoelectronics and smart manufacturing, 2019, 1(03): 55-67.

[5] Haomiao Wang et al. Silicon photonic transceivers for application in data centers. J. Semicond (2020) 41 101301.

[6] Tournié E, Cerutti L, Rodriguez J-B, Liu H, Wu J, Chen S. Metamorphic III-V Semiconductor Lasers Grown on Silicon. MRS Bull (2016) 41(3): 218–23.

[7] Junjie Yang et al. (2021) All-MBE grown InAs/GaAs quantum dot lasers with thin Ge buffer layer on Si substrates. J. Phys. D: Appl. Phys. 54 035103.

[8] Volz K, Beyer A, Witte W, Ohlmann J, Németh I, Kunert B, et al. GaP-nucleation on Exact Si (001) Substrates for III/V Device Integration. J CrystGrowth (2011) 315(1): 37–47.

[9] Crosnier G, Sanchez D, Bouchoule S, Monnier P, Beaudoin G, Sagnes I, et al. Hybrid Indium Phosphide-On-Silicon Nanolaser Diode. Nat Photon (2017) 11(5): 297–300.

[10] M. Liao et al., "Monolithically Integrated Electrically Pumped Continuous-Wave III-V Quantum Dot Light Sources on Silicon," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 23, no. 6, pp. 1-10, Nov.-Dec. 2017, Art no. 1900910.