A CMOS-Based 4-Bit Absolute-Value Detector for BCI Signal Feature Extraction

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Abstract. In recent years, the integrated circuit industry has developed rapidly. Since the advent of the first computer, the performance of chips has increased exponentially while the size and power consumption have also decreased. Today, a high-performance chip is much smaller than a card. The increase in computing power also means that there are more possibilities in the field of computing and simulation. Many disciplines have also made new breakthroughs due to the improvement of computing power. Brain-computer interfaces and technologies such as rehabilitation medicine and virtual reality based on it are very promising technologies that allow the brain to interact directly with external devices. However, the signals of the human brain are very complex, and the brain-computer interface, as a signal relay station between the human brain and external devices, requires very powerful data processing capabilities. This article will first introduce the brain-computer interface technology and the method of processing the signals in it, and then propose an efficient absolute-value detector circuit design to achieve a very important step in signal processing.

Keywords: Integrated circuit; Brain-computer interface; 4-bit absolute-value detector.

1. Introduction

The term metaverse was coined in 1992 in the science fiction novel Snow Crash. The more recognized source of the concept represented by this term is the 1981 novel True Names, which creatively conceives a virtual world that enters and obtains sensory experiences through brain-computer interfaces [1]. The metaverse I define is a highly realistic virtual world based on mature virtual reality, brain-computer interface, artificial intelligence and other technologies, as described by Sword Art Online, The Matrix, Ready Player One, etc. Human consciousness can be transmitted to it through technological means, experiencing a variety of life, and at the same time, the cost of maintaining a high quality of life does not need to be as expensive as in the real world.

The ethical issues raised by these technologies and the fundamental purpose of some of today's technologies in the name of the metaverse are beyond the scope of this article. But admittedly, today's research has revealed a problem, that is, traditional virtual reality devices cannot input complex motion instructions, nor can people experience high-fidelity sensations such as touch and taste. As a result, traditional devices are no longer up to the task, and brain-computer interfaces are needed to allow the brain to interact directly with the device. With the rapid development of integrated circuit technology, this can process more and more complex brain signals, and the scope and function of brain-computer interfaces are also expanding. This article will first introduce the definition, function, classification and application fields of brain-computer interface technology and give methods for external devices to process brain signals. Then, an efficient absolute-value detector circuit design will be proposed to complete an important step in processing brain signals. Finally, the circuit will be calculated and optimized.

2. Theoretical Basis of BCI

2.1. Defination of BCI

A brain-computer interface (BCI) establishes a direct link between the brain or nervous system of organic life forms and an external device, which could include human or animal brains as well as

brain cell cultures. In simple terms, BCI is the bridge that connects the neural signals in the brains of intelligent organisms with signals from external devices [2]. Taking the movement of the human body as an example, the body feels external environmental stimuli through tactile receptors such as skin, and conducts stimulation to the spinal cord through the peripheral nervous system, and then conducts to sensorimotor related areas of the cerebral cortex through ascending nerve pathways such as the cerebellum for analysis and processing, and then transmits the feedback through the descending pathway to end effectors such as muscles, and then controls arms, hands, wrists, etc. to flex and extend, grasp, use tools, etc. to achieve interaction with the external environment. The significance of BCI is that it can allow more devices to be connected to the human body to carry out more complex operations and obtain more information, no longer limited by the limitations of flesh and blood, or to fill the functional loss caused by the damage of the original organs. This technology can be applied to medical, entertainment, industrial and other fields.

BCI can be roughly divided into three types: invasive, partially invasive, and non-invasive [3]. Invasive BCIs are typically implanted directly into the gray matter of the brain, so high-resolution signals can be directly input and output. However, it is easy to trigger immune rejection and infection, resulting in a decline in signal resolution and even damage to the health of the implanted person. This type of BCI can be used to help blind patients see again, or to help paralyzed patients operate computers. Partially invasive BCIs are generally implanted in the cranial cavity and are located outside the gray matter, and although the signal resolution is not as good as invasive BCIs, it has less impact on the human body. Non-invasive BCIs have the lowest resolution of signals, and it is even difficult to tell which brain region or associated neural unit the signal came from because the signal through the soft or hard tissues of the head is diverged and blurred [4]. However, non-invasive BCI generally only needs to be worn directly or fitted to the head, so there is no damage to the human body at all, and it is still widely accepted. However, regardless of the type of BCI, how the signals from the brain are extracted and processed into signals that can be recognized by the device is critical.

2.2. Processing of BCI signals

The decoding rate is the key to determining BCI availability and robustness. In fact, in the process of signal acquisition, due to interference such as power frequency noise and pseudo-traces, the recorded signal is polluted and has a low signal-to-noise ratio. Therefore, in order to obtain better decoding performance, it is important to perform the necessary preprocessing of the acquired signal. Generally, notch filtering is used to eliminate power frequency interference; Band pass filtering is used to obtain frequency bands of interest. For intrusive BCI, the typical filtering range is between 0.5 and 400Hz, limited by the sampling rate and signal amplitude. For non-invasive BCI, the collected signal is attenuated by the soft and hard tissues of the head, and high-frequency information is difficult to record, so useful information is mainly concentrated in the low frequency band [5].

Then there is the amplification circuit, which amplifies the processed signal for final feature extraction. There are generally three types of amplification circuits. The input signal of the co-emission amplification circuit is input from the base of the transistor and output from the collector. Because the emission is extremely common to ground, so it is named a common-emission amplification circuit. The common-emission amplification circuit is the most widely used transistor amplification circuit. The current and voltage gains of the common-emitted amplification circuit are greater than 1, which is suitable for low-frequency situations. The input signal of the co-collector amplification circuit originates from the triode base and exits through the emitter. This circuit, often referred to as an emitter follower, derives its name from the fact that the collector serves as a shared ground terminal. The emitter follower only has current amplification, no voltage amplification, but has voltage following. It has very low output impedance, very high input impedance, and good frequency characteristics. The input signal of the common-base amplifier circuit is input from the transistor emitter and output from the collector. Because the base pole is common to ground, it is named a common-base amplification circuit. The common-base amplification circuit only has voltage

amplification, no current amplification, but has a current following. It has very low input impedance and good high frequency characteristics.

Finally, the characteristic signal is extracted, and the common characteristic indicators in the time domain include waveform index, pulse index, zero crossing rate, etc. Most feature extraction expressions are inseparable from the Absolute Value Detector. Therefore, an efficient circuit that takes and compares absolute values will improve the efficiency of the feature extraction step and directly affect the performance of BCI. This circuit will be designed using 4-bit as an example and will be implemented by a chip based on CMOS transistors.

3. Design of A 4-Bit Absolute Value Detector

3.1. Design Ideas

For a 4-bit absolute value detector, assuming that the input value is X (4-bit 2's complement code), the value being compared is Y (4-bit 2's complement code) and is positive by default. Since the absolute value comparator needs to output 1 when the result is and output 0 when it is less than, the form of Y-|X| is adopted.

According to the principle of 2's complement code: when Y-|X|, if the 3-bit carry=1, then Y≥|X|, if the 3-bit carry=0, Y<|X|. Therefore, we only need to input the 3-bit carry into the not gate, if the output is 1, then |X|>Y, if the output is 0, |X|≤Y. Then in the absolute value part, taking the opposite number of the absolute value, that is, if the input is a positive number, the opposite number will be output, and if the input is a negative number, it will be the output directly. The summary of the above ideas are shown in the Fig. 1.

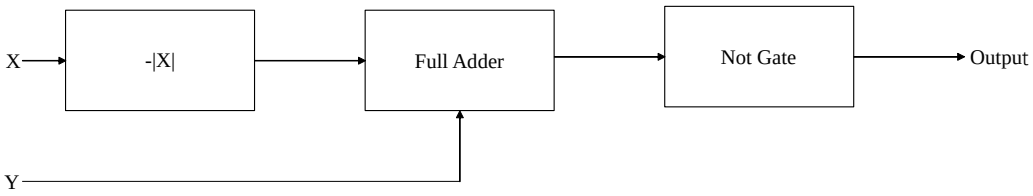


Fig. 1 Sketch of the design idea (Photo/Picture credit: Original)

3.2. Logic Circuit Design

The logic circuit diagram is shown in Fig. 2. This circuit diagram was drawn by Proteus 8 Professional. The seven inputs from top to bottom are the sign bit, 3-bit, 2-bit, 1-bit of X and the 3-bit, 2-bit, 1-bit of Y. 4077 in the figure represents the XNOR gate.

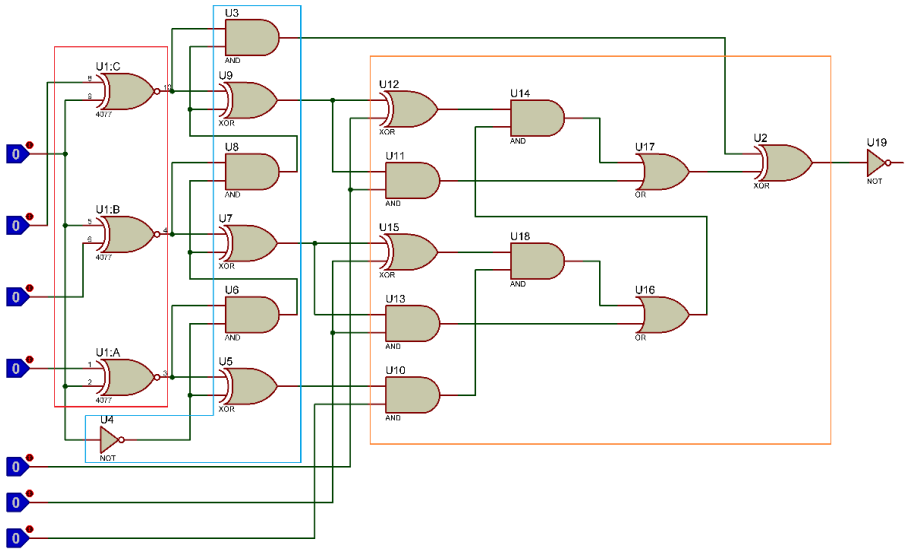


Fig. 2 Logic Circuit Diagram (Photo/Picture credit: Original)

The logic circuit in the red frame detects the sign bit of the input. If the sign bit is 0, it means that the input number is a positive number, then invert 1 to 3 bits and output. If the sign bit is 1, it means that the input number is negative, and 1 to 3 bits are output directly. This step can be represented in Table 1 using a truth table.

Table 1. Truth table

Sign Bit	Input	Output
0	0	1
0	1	0
1	0	0
1	1	1

The logic circuit in the blue frame also detects the sign bit of the input. If the sign bit is 0, the 3-bit number output by the logic circuit in the red frame is added to 1 and output. If the sign bit is 1, add 0 to the 3-bit number output by the logic circuit in the red frame and output it, that is, output it directly.

Regardless of the value of the sign bit, only a 1-bit value needs to be added. This can be understood as the other addend of each bit only comes from the carry of the previous bit. Therefore, an exclusive OR gate is required to output the sum of the standard bits, and an AND gate to output the standard bit for the carry. It is worth noting that the role of the signal bit ends here. 4-bit will be used to output carry from 3-bit.

Under the combined action of these two parts of the logic circuit, the input X will be output as the opposite number of the absolute value of X, that is - |X|. It is worth noting that although the value is still represented by 2's complement code, the 4-bit output of the AND gate numbered U3 is no longer used to represent the sign bit, but a carry from 3-bit. And the sign bit no longer participates in subsequent logic calculations.

The logic circuit in the orange frame adds - |X| to Y bit by bit using incomplete full adders. The comparator section only needs to detect carry from the most significant bit, so a complete full adder does not need to be used. That is, it only needs to input the two addends of this bit and the carry from the previous bit, and output the carry, without outputting the sum.

When considering that the value of the input is 0, it is not possible to detect only a carry from 3-bit. It is worth noting that when the input value of X is 0 (decimal), it can only be represented by 0000 (2's complement code) but not 1000 (2's complement code). Again, the 4-bit of the logic circuit in the orange frame does not indicate positive or negative. According to the principle of 2's complement

code, it is not difficult to conclude that the 4-bit here cannot generate a carry, so only one XOR gate is needed to perform a half-add operation on the values from the U3 AND gate and the U17 OR gate. Of course, don't forget to add a NOT gate at the end.

Here the principle of another comparator should be mentioned: Comparing the most significant bits of the two numbers. If one is greater than the other, we know that number is greater. If they are equal, we will move to the second most significant bit, and so on. Compared with this comparator, the comparator used in this paper requires fewer logic gates and the logic circuit is more concise.

From the overall perspective of the entire logic circuit, no matter whether the input value is positive or negative or 0. All share a set of logic circuits for calculation, which greatly reduces the circuit scale and improves the integration level.

3.3. Simulation

Circuit simulations were performed via Proteus 8 Professional. In Fig. 3, the input is set to 1010 (-6 in decimal) and the compared value is set to 101, and the output value is 1, which meets the requirements.

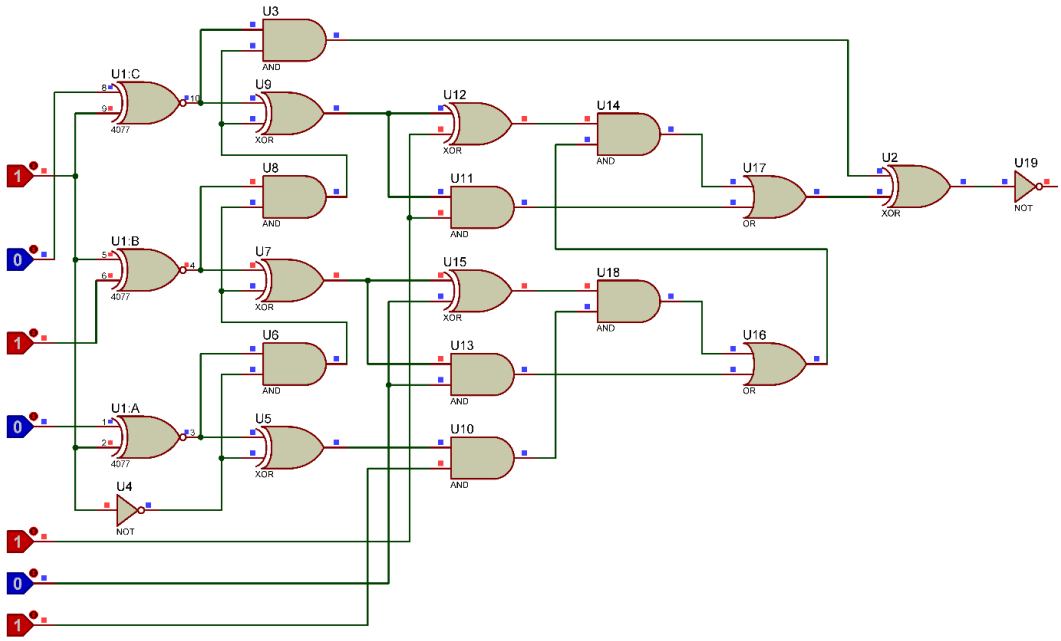


Fig. 3 Simulation of Comparing 1010 with 101 (Photo/Picture credit: Original)

In Fig. 4, the input is set to 0101 and the compared value is set to 111, and the output value is 0, which meets the requirements.

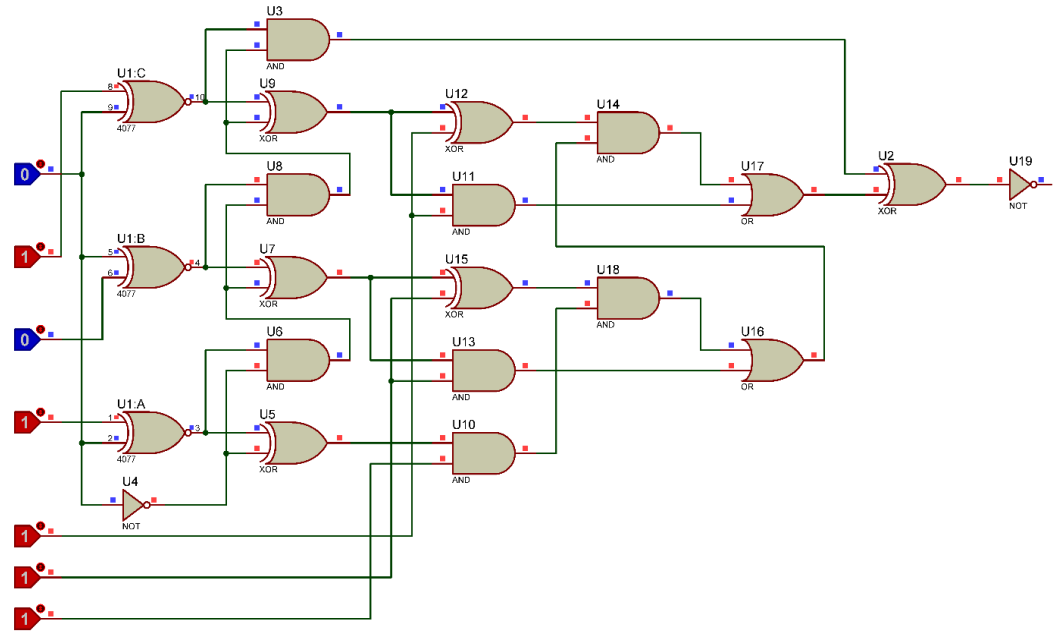


Fig. 4 Simulation of Comparing 0101 with 111 (Photo/Picture credit: Original)

4. Optimization

4.1. Critical Path

Prior to performing the calculation, the critical path, which consists of the highest count of logic gates and the most intricate logic gates, is designated as the path with the greatest delay. In Fig.5, the critical path is indicated by the red arrow, and for simplicity, all the logic gates along this path are sequentially numbered.

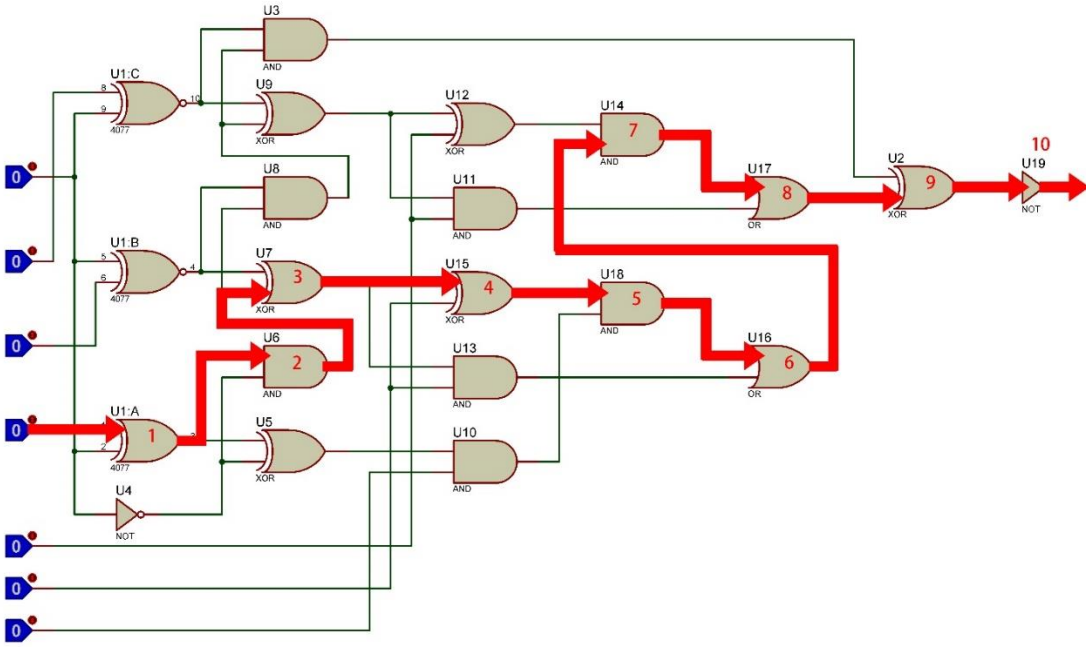


Fig. 5 Critical Path (Photo/Picture credit: Original)

4.2. Delay and Size

Every logic gate within the chip comprises CMOS transistors, making the entire chip CMOS-based. To streamline the calculation process, we will employ logical efforts. The logical effort of a logic gate is quantified as the ratio between its input capacitance and that of an inverter generating an equivalent output current [6]. Following the logical effort principle, this paper encompasses:

$$\begin{cases} G=\prod g_i \\ B=\prod b_i \\ H=\frac{C_{out}}{C_{in}} \\ F=GHB \end{cases} \tag{1}$$

where G is the path logic effort, g is the logical effort, B is the path branch effort, b is the branch effort of a single logic gate, H is the path electrical effort, C_{out} is the output capacitance, C_{in} is the input capacitance, and F is the path logical effort delay [7]. After calculating the value of F, in order to minimize the delay, ideally, the logical effort delay f for each logic gate satisfies the equation:

$$f=\sqrt[n]{F} \tag{2}$$

where n is the number of logic gates on the path [8]. Then, in order to calculate the delay and size factor for each logic gate, the following equation is required:

$$\begin{cases} f_i = g_i h_i \\ D=\sum f_i + \sum p_i \\ s_i = \frac{g_1 + s_1}{g_i} \prod_{j=1}^{i-1} \frac{h_j}{b_j} \end{cases} \tag{3}$$

where h is the electrical effort of a single logic gate, p is the parasitic delay of a single logic gate, D is the path delay, and s is the size factor of a single logic gate [9].

The logical effort and parasitic delay for all logic gates in critical path are listed in Table 2 and the calculation results are listed in Table 3.

Table 2. Logical Effort and Parasitic Delay of Logic Gates ($p_{inv} = 1.0$)

	NOT(INVERTER)	XOR	XNOR	AND	OR
Logical Effort	3	4	4	4/3	5/3
Parasitic Delay	1	4	4	3	3

Table 3. Calculation Results

	1	2	3	4	5	6	7	8	9	10
Logical Effort Delay	2.97	2.97	2.97	2.97	2.97	2.97	2.97	2.97	2.97	2.97
Electrical Effort	0.74	2.23	0.74	0.74	2.23	1.78	2.23	1.78	0.74	2.97
Size Factor	1	1.11	0.83	0.61	1.36	2.42	5.38	9.60	7.12	21.07
Path Delay	61.7									

According to the calculation results and unit conversion, the delay of the critical path can be obtained, that is, the delay of the entire circuit is 15.35 FO4(1V). However, this result is idealized after all, considering that practical applications will have specific restrictions or emphasis on parameters such as delay, power consumption, and size, the equation of the device capacitor charging theory is an important basis for adjusting parameters [10].

$$D \propto \frac{V_{DD}}{(V_{DD}-V_T)^2} \tag{4}$$

5. Conclusion

This article first introduces BCI technology through the metaverse technology that has emerged in recent years. The applications, advantages and disadvantages of different BCI technologies, as well as the techniques for processing BCI signals, are introduced. Then, for the feature extraction part in signal processing, an absolute value comparison circuit is designed, and the basic principle and logic circuit of its operation are explained in detail by taking the 4-bit Absolute-Value Detector circuit based on CMOS transistors as an example. Finally, logical effort was used to optimize the latency and size of the chip. Admittedly, the logical effort method, while well suited for manual calculations, has some limitations: it does not consider input slope, ignores the effects of velocity saturation and lining offset effects, and makes it difficult to analyze circuits with complex branch paths.

For BCI technology, I think it is not just a technology that can be applied in medical and entertainment fields. As BCIs can extract and parse more complex brain signals, perhaps one day we can understand the nature of consciousness. After all, today's artificial intelligence, while already very powerful and capable of abstract creations such as drawing and even writing, is still essentially procedural rather than self-aware. I believe that whether it is a professional scholar or a PC DIYer, it is not difficult to find that the main volume of today's high-performance computers comes from heat dissipation equipment, and the chip itself only occupies a small part of the volume. The process and heating of the chip are one of the factors restricting the development of integrated circuits. The manufacture and use of high-performance chips brings together cutting-edge technologies in many important scientific fields such as semiconductors, electromagnetism, materials science, and computer science, so it is known as the crystallization of human science and technology. It is believed that one day in the future, uploading consciousness to artificial bodies and realizing synthetic evolution will no longer be a dream.

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