A Way to Optimize Delay of Carry-Skip Adders by Using Blocks of Variable Sizes

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Abstract. As one of the most common operational modules in computer processors, the optimization of the propagation delay of adders has attracted extensive attention of researchers. This article proposes a method of optimizing the delay of carry-skip adders by using blocks of variable sizes. By increasing the sizes of the bypass stages gradually and then decreasing it stage by stage, keeping the delay of the first and last stage short, the total propagation delay is optimized. Compared with fixed size carry-skip adders, the delay of variable sizes carry-skip adders has a square root relationship with the number of bits. Thus, when the number of bits is large, the propagation delay is significantly reduced. After calculation, when the number of bits is 16, the propagation delay decreases by 16.67%, and when the number of bits is 256, it decreases by 52.78%. Due to the shorter propagation delay, variable sizes carry-skip adders have faster operation speed and can be applied to improve the performance of computer processors.

Keywords: Carry-skip adders; propagation delay; optimization.

1. Introduction

Addition is one of the most fundamental operations in a computer's arithmetic logic unit (ALU). In a computer processor, the adder, as an important unit circuit, performs a large number of arithmetic functions all the time [1, 2]. Therefore, optimizing the adder is crucial to improving the operation speed and even the overall performance of the processor. Since the adder is often located on the critical path of the circuit, how to shorten its propagation delay by improving the circuit design has always been a concern of researchers. Although a variety of adders with different structures have been reported, optimizing their performance is still a key issue in improving processor performance today [3].

This paper proposes a method to optimize delay of carry-skip adders by using blocks of variable sizes. Based on analyzing the working principle of traditional fixed size carry-skip adders and the expression of propagation delay, an optimized method is to increase the size of the bypass block stage by stage to the intermediate stage, and then reduce the size gradually. This method ensures that as well as the delay of the first and the last stage keeping small, the overall propagation delay and the number of bits have a square root relationship, which is better than a linear relationship. This paper presents the expression of the propagation delay and specific implementation of variable sizes carry-skip adders, and based on three assumptions, the propagation delay under different digits is calculated according to the expression. Compared with fixed size carry-skip adders, when the number of adders increases from 16 to 256, the propagation delay is shortened from 16.67% to 52.78%. The variable sizes carry-skip adders have a shorter propagation delay and can improve the operation speed and optimize the performance of ALU when performing addition or composing other arithmetic function modules, such as subtractors and multipliers.

2. Analysis of the Principle

2.1. Description of the Program

The principle of a traditional fixed size carry-skip adder is shown in Fig. 1. Assume that the adder has a total of N bits and is divided into N/M stages of equal length, each containing M bits.

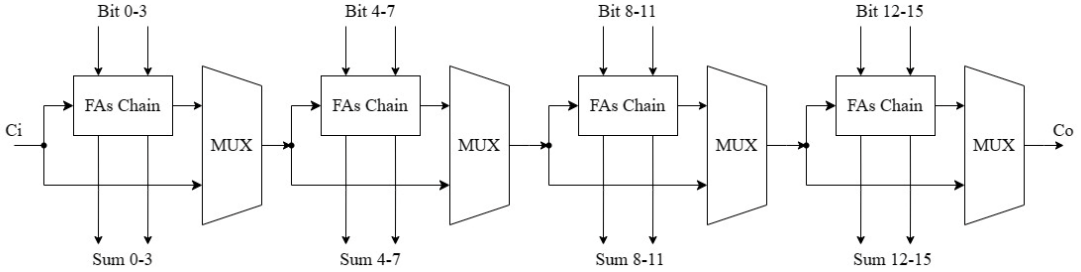


Fig. 1 Fixed size carry-skip adder (N=16, M=4) (Photo/Picture credit: Original)

In the worst case, the carry signal is generated at the first bit, after passing bit by bit through the first block, crossing (N/M-2) bypass stages, and finally is absorbed at the last bit of the last block, where no carry is generated [4]. According to this critical path, the expression of the propagation delay of fixed-size carry-skip adders can be derived [5]:

$$t_p = t_{setup} + Mt_{carry} + \left(\frac{N}{M} - 1\right) t_{skip} + (M-1)t_{carry} + t_{sum} \tag{1}$$

where t_{setup} means the time required to establish a signal at the first stage, t_{carry} means the propagation delay through one bit, t_{skip} means the propagation delay through a multiplexer of a bypass stage, and t_{sum} means the time required for the summation at the last stage. The two input signals to the multiplexer of each stage are respectively the carry chain propagation signal and the carry bypass signal of that stage [6]. The arrival times of these two signals are different, and generally the former has already been stable before the latter arrives. In order to optimize delay, it is necessary to make the arrival times of these two signals as equal as possible, which can be achieved by changing the size of each block [7].

Admittedly, this goal can be achieved by gradually increasing the size of each continuous block, so that the propagation time required for the carry chain signal of the subsequent stage is longer, and more time can be spent waiting for the carry signal generated by the previous stage. However, according to Expression (1), since the carry signal that propagates through the last stage and is absorbed in the last bit is also on the critical path, it is not desirable to make the size of the last block larger [8]. Therefore, a better way to change the sizes of the bypass stages is to gradually increase the size of each block from the first stage to the middle, and then gradually decrease the size of each block to the last stage, that is, make the size of the middle block the largest, while keeping the size of the first and last blocks to a minimum.

2.2. Derivation of the Formula

According to the above method, it is assumed that the improved variable sizes carry-skip adder has a total of N bits and is divided into P stages with different lengths. Besides, the first stage has K bits, and each stage increases by one bit, until the middle stage has the most bits, and then each stage decreases by one bit, so that the last stage also has K bits [9].

When P is an even number, there are two middle stages with the greatest number of bits, which is equal to (K+P/2-1). At this time, the expression of N can be written as:

$$\begin{aligned} N &= K + (K+1) + (K+2) + \cdots + \left(K + \frac{P}{2} - 1\right) + \left(K + \frac{P}{2} - 1\right) + \cdots \\ &\quad + (K+2) + (K+1) + K \\ &= \left[K + \left(K + \frac{P}{2} - 1\right)\right]\frac{P}{2} \\ &= \left(2K + \frac{P}{2} - 1\right)\frac{P}{2} \\ &= \frac{P^2}{4} + \frac{P(2K-1)}{2}, when\ P\ is\ even \end{aligned} \tag{2}$$

When P is an odd number, there is only one middle stage with the greatest number of bits, which is equal to (K+P/2-1/2). At this time, the expression of N can be written as:

$$\begin{aligned} N &= K + (K+1) + (K+2) + \cdots + \left(K + \frac{P-1}{2}\right) + \cdots + (K+2) + (K+1) + K \\ &= \left[K + \left(K + \frac{P}{2} - \frac{1}{2}\right)\right]\frac{P+1}{2} - \left(K + \frac{P-1}{2}\right) \\ &= \left(2K + \frac{P-1}{2}\right)\frac{P+1}{2} - \left(K + \frac{P-1}{2}\right) \\ &= \frac{P}{4}(P+1) + (2K - \frac{1}{2})\frac{P+1}{2} - \left(K + \frac{P-1}{2}\right), when\ P\ is\ odd \end{aligned} \tag{3}$$

When N is much larger than K, the square term of P occupies the main part in the formula. Thus, no matter whether P is even or odd, the relationship between N and P is as follows:

$$N \approx \frac{P^2}{4}, when\ N \gg K \tag{4}$$

or:

$$P \approx 2\sqrt{N}, when\ N \gg K \tag{5}$$

In Expression (1), N/M represents the number of stages. While for variable sizes carry-skip adders, the number of stages is represented by P. In addition, the number of bits of the first and last stage is equal to K instead of M. Hence, by replacing the position of N/M with P and substituting Expression (5), and then replacing the position of M with K, the expression of the propagation delay of variable sizes carry-skip adders can be similarly obtained:

$$t_p = t_{setup} + Kt_{carry} + \left(2\sqrt{N} - 1\right)t_{skip} + (K-1)t_{carry} + t_{sum} \tag{6}$$

2.3. Analysis of the Formula

According to Expression (1), the propagation delay of fixed size carry-skip adders has a linear relationship with the number of bits N, that is, the rate at which the delay changes with the increase of N depends on the slope of this linear relationship. Compared with ripple carry adders which is also in a linear relationship, the slope of carry-skip adders is smaller, which means that when N is large, the delay of carry-skip adders is smaller than that of ripple carry adders. Nevertheless, since the number of bits in each block in fixed size carry-skip adders cannot be too large (otherwise it will lead to an increase in delay), the increase of N increases the delay proportionally, and this effect is still not negligible.

For variable sizes carry-skip adders, according to Expression (6), when N is large, delay is proportional to $\sqrt{N}$. This square root relationship is extremely important because the square root function grows more and more slowly compared to linear growth. This means that even when N increases to a large value, the increase in delay is so small that sometimes this small increase can be ignored, and it is considered that when N is large, the propagation delay is relatively close to a constant. The implement of a variable sizes carry-skip adder is shown in Fig. 2.

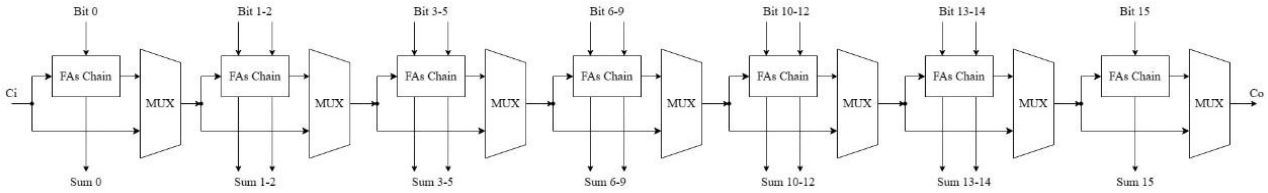


Fig. 2 Variable sizes carry-skip adder (N=16, P=7, K=1) (Photo/Picture credit: Original)

It can be proved that the relationship between the propagation delay and the number of digits is upper bounded by $\log_2 N$, which is achieved in carry look-ahead adders [10]. At this time, the propagation delay will be extremely close to a constant when N is large. The above analysis can be summarized as the following formula:

$$t_p = \begin{cases} O(N), & for\ fixed\ size\ carry - skip\ adders \\ O(\sqrt{N}), & for\ variable\ sizes\ carry - skip\ adders \\ O(\log_2 N), & for\ carry\ look - ahead\ adders \end{cases} \tag{7}$$

3. Calculation and Analysis of Results

3.1. Assumptions for Simplification

In order to compare the delay relationship between fixed size carry-skip adders and variable sizes carry-skip adders under the same N condition, after comparing Expressions (1) and (6), it can be found that due to the difference in the total number of stages (N /M and P) and the first level of digits (M and K), it is impossible to perform direct calculations and draw intuitive conclusions. In order to simplify the mathematical model and highlight the laws, three assumptions need to be made for the subsequent simplification and calculation.

3.1.1 Assuming that $t_{setup} = t_{carry} = t_{skip} = t_{sum} = 1$

From the perspective of circuit implementation, t_{carry} is determined by delay of full adders, and t_{skip} is determined by delay of XOR gates, AND gates and multiplexers. These delays are related to the technology and style of the circuit, so the quantitative relationship between t_{carry} and t_{skip} may vary in different circuits. However, for the sake of calculation, it is very necessary to clarify this quantitative relationship, so it will be useful and convenient to assume that $t_{carry} = t_{skip} = 1$. In additions, t_{setup} and t_{sum} is not necessary for calculation, but assuming that $t_{setup} = t_{sum} = 1$ leads to a more concise mathematical expression.

3.1.2 Assuming that $M = 4$

For fixed size carry-skip adders, the propagation delays of the two input signals of the first-stage multiplexer should be kept as equal as possible, so there is an optimal value for the selection of M, which is determined by the process parameters of circuits. In general, M takes 4.

3.1.3 Assuming that $K = 1$

For variable sizes carry-skip adders, to make Expression (6) true, it must be ensured that $N \gg K$. Therefore, it is safe for the accuracy of the calculation results to suppose that $K = 1$.

3.2. Calculation Results and analysis

Based on the above three assumptions, according to Expressions (1) and (6), the simplified expressions of the propagation delay of fixed size carry-skip adders (t_{pF}) and variable sizes carry-skip adders (t_{pV}) can be obtained:

$$\begin{aligned} t_{pF} &= 1 + 4 + \left(\frac{N}{4} - 1\right) + (4 - 1) + 1 \\ &= \frac{N}{4} + 8 \end{aligned} \tag{8}$$

$$\begin{aligned} t_{pV} &= 1 + 1 + \left(2\sqrt{N} - 1\right) + (1 - 1) + 1 \\ &= 2\sqrt{N} + 2 \end{aligned} \tag{9}$$

Take N equal to 16, 32, 64, 128, 256 respectively, which are the number of bits that computer processors commonly use at present and may use in the future, and then substitute into the expression for calculation. The calculation results are shown in Table 1.

Table 1. Calculation Results

N	t_{pF}	t_{pV}
16	12	10
32	16	13.31
64	24	18
128	40	24.63
256	72	34

The results shows that variable sizes carry-skip adders have a more optimized propagation delay than fixed size carry-skip adders. For $N = 16$, delay is reduced by 16.67%, and for $N = 256$, by 52.78%.

Fig. 3 shows the curves of t_{pF} and t_{pV} as a function of N as N varies from 1 to 32. It is worth noting that when N is small, the actual situation will deviate from the result of the curve because the condition that $N \gg K$ is not satisfied. Nevertheless, it clearly shows that variable sizes carry-skip adders have better propagation delay than fixed size carry-skip adders, and as N gets larger, the delay is reduced more.

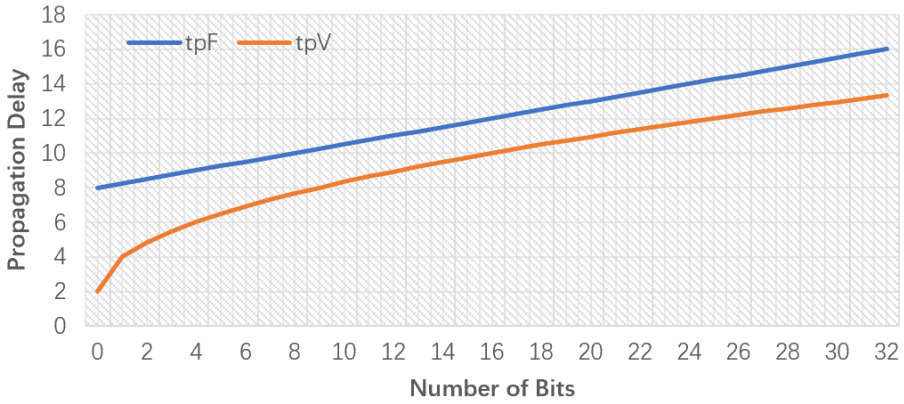


Fig. 3 The curves of t_{pF} and t_{pV} as a function of N (Photo/Picture credit: Original)

4. Conclusion

In the research of this paper, based on the principle of fixed size carry-skip adders and the expression of the propagation delay, in order to optimize delay, the author gives a method of first gradually increasing the size of each block and then gradually reducing the size. Then, the author derives the mathematical expression of the method of using blocks of variable sizes, verifies the feasibility of this method, and obtains the expression of the propagation delay of variable sizes carry-skip adders, as well as the condition for the expression to hold true. Then, the author compares and analyzes the delay expressions of the two kinds of adders and points out that the square root delay relationship of variable sizes carry-skip adders is more optimized than the linear delay relationship of fixed size carry-skip adders. Finally, based on three assumptions, the calculation results verify the correctness of this design. When the number of digits increases from 16 to 256, delay decreases from 16.67% to 52.78 %.

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