A design of fully differential operational amplifier for switched-capacitor application

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Abstract. Switched-capacitor (SC) circuit is used widely in communication and signal processing systems, such as switched-capacitor filter and switched-capacitor integrator. This paper proposes a fully differential operational amplifier for switched-capacitor application. The designed amplifier comprises common mode feedback circuit, auxiliary amplifier and main amplifier using fold cascode structure and its biasing circuit. The supply voltage VDD is 1V and VSS is -1V. After the simulation using TSMC 0.18μm process model, the simulation result shows the proposed amplifier achieve about 100.6dB DC gain, 66 degree phase margin,333 MHz unit gain bandwidth, 3.78V differential output swing, 287V/μs slew rate,122.8 dB DC PSRR, 114 dB DC CMRR, 1.6mW power consumption, the input reference noise is about 6nV/√Hz at 1MHz, the Total Harmonic Distortion of this amplifier is less than about 1.05%.The proposed fully differential operation amplifier meet all the specification, and it can be used in some SC circuit applications.

Keywords: Switched-capacitor circuit, fully differential amplifier, gain boosting, common mode feedback.

1. Introduction

The concept of a switched capacitor (SC) circuit was first proposed in 1972, and now it has been widely used in many electronic fields [1]. In analog integrated circuits, resistance integration is much more difficult and expensive than capacitors, which limits the application of resistors in many areas that require high accuracy and cost. Switched capacitor circuits work by transporting charge with switches and capacitors instead of resistors, thereby avoiding difficult-to-integrate resistors in integrated circuits [2-4]. The SC circuit has many good characteristics such as high precision time constant, good voltage linearity, good temperature characteristic, compatible CMOS process, so it has been widely implemented in many vital parts of analog circuit such as pipeline Analog to Digital Converter (ADC), DC-DC converter, Switched capacitor filter [5-7].

Compared to single-ended output operational amplifiers, the operational amplifier with fully differential structure has stronger anti-jamming ability to noise in circuit and larger output voltage swing, higher linearity, simpler bias circuit, it also can reduce the even harmonic distortion of the circuit [8]. In SC circuit, the operational amplifier with full differential structure can reduce the offset voltage caused by channel charge injection of MOS switches. The drawback of fully differential operational amplifier is that it needs extra common-mode feedback (CMFB) circuit due to output voltage error caused by mismatch of current source. The fully differential operational amplifier is used in the switched capacitor circuit to form the switched capacitor amplifier. The SC amplifier always is used in active filters, ADC, and many other analog systems.

The structure of this paper is organized as follows. Section II introduces the design of proposed fully differential amplifier, including the introduce of gain boosting technology, the structure of proposed amplifier circuit, the design of auxiliary amplifier and common-mode feedback circuit and bias circuit, some circuit performance analysis. Section III shows the simulation results of proposed fully differential amplifier. Section V is the conclusion of this paper.

2. Circuit implementation

2.1. Gain boosting technology

Figure. 1 shows the schematic of a simple cascode which adopts gain boosting technology. The M1 is input transistor, M2 is cascode device, M1 and M2 form main cascode amplifier. The Aux is auxiliary amplifier, it drives the gate of M2 and forces the source voltage of M2 equal to reference voltage. If the drain voltage of M2 increases, then the source voltage of M2 tend to increase. As a result, the output voltage of auxiliary will drop, which make the current of M2 decrease, then the source voltage will tend to keep. When the gain of auxiliary is large enough, the source voltage of M2 will be clamped to reference voltage.

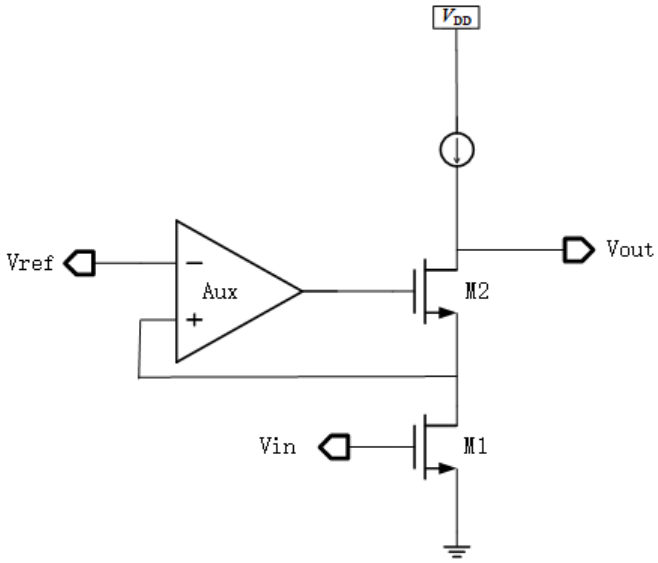


Figure 1. Schematic of the cascode amplifier using gain boosting technology
(Photo/Picture credit: Original)

The DC gain of simple cascode amplifier is given by:

$$A_v = g_{m1}r_{o1}(g_{m2}r_{o2} + 1) \approx g_{m1}g_{m2}r_{o1}r_{o2} \tag{1}$$

The DC gain of cascode amplifier using gain boosting technology is given by:

$$A_v = g_{m1}r_{o1}(g_{m2}r_{o2}(A + 1) + 1) + g_{m1}r_{o2} \approx Ag_{m1}g_{m2}r_{o1}r_{o2} \tag{2}$$

The A stands for the voltage gain of auxiliary amplifier. Comparing (1) and (2), the transconductance of M2 increase to about A times, and the voltage gain of cascode amplifier have same increase.

The drawback of this technology is that the auxiliary amplifier takes pole-zero doublet, increasing the setup time of main amplifier. In order to make main amplifier work steadily, the unity-gain bandwidth of auxiliary amplifier ω_{aux1} should be less than the non-main pole frequency of main amplifier ω_{p2}, and greater than β times the unity-gain bandwidth of main amplifier ω_{p1}. β stands for feedback factor [9]. The following inequality expresses this relationship.

$$\beta\omega_1 < \omega_{aux1} < \omega_{p2} \tag{3}$$

2.2. Fully differential amplifier

Figure.2 shows the structure of the proposed fully differential amplifier. The component includes four auxiliary amplifiers, two CMFB components.

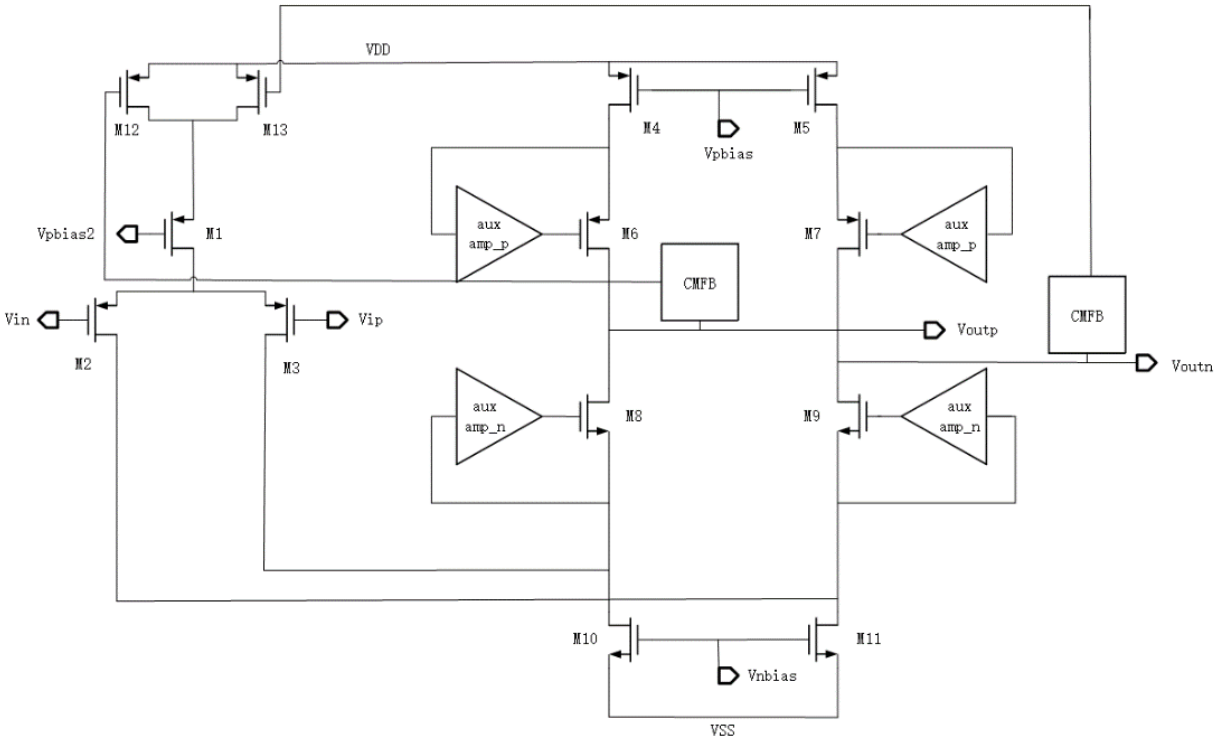


Figure 2. Schematic of proposed fully differential amplifier (Photo/Picture credit: Original)

The proposed fully differential amplifier adopts a folded cascode structure and gain boosting technology. Compared to telescopic cascode structure, the folded cascode structure has larger output voltage swing and wider input common-mode range, which is important for the application in switched capacitor circuits. The fold cascode structure has smaller voltage gain than telescopic cascode structure, so proposed amplifier use gain boosting technology, which uses four auxiliary amplifiers to help main amplifier improve voltage gain.

If NMOS is selected as input transistor, the amplifier will have a higher gain bandwidth product, but the non-main pole frequency will be very low. If PMOS is selected as input transistor, the amplifier will have smaller gain bandwidth product as well as it need wider transistors and larger biasing current to achieve same slew rate as NMOS, but PMOS input transistor make amplifier have higher frequency non-main pole, which can achieve larger phase margin and lower noise. As a result, this design chooses PMOS transistor as input transistor.

From the schematic of proposed fully differential amplifier, input transistor M2 and M3 form the differential pair, and M1 provides tail current for them. M4, M5, M6, M7 form cascode current source load, improving the output impedance.M10, M11 are also current source, all the current from this circuit flow them. The common-mode feedback circuit drive M12 and M13 depend on the change of output voltage. The sum of the current of M12 and M13 will adjust the current flow the tail current source M1. If the sum of Voutn and Voutp increase, then the sum of current flow the M12 and M13 will drop, which make the current flow the tail current source M1 decrease and the current flow M4, M5, M6, M7, M8, M9 increase. As a result, the sum of Voutn and Voutp will drop, which keeps common mode level unchanged.

The output resistor of main amplifier can be expressed by:

$$R_{out} \approx A_n g_{m8} r_{o8} (r_{o3} \| r_{o10}) \| A_p g_{m6} r_{o6} r_{o4} \tag{4}$$

A_n and A_p stand for the gain of auxiliary amplifier.

The voltage gain of main amplifier can be expressed by:

$$A_V = G_m R_{out} \approx g_{m3} A_n g_{m8} r_{o8} (r_{o3} \| r_{o10}) \| A_p g_{m6} r_{o6} r_{o4} \tag{5}$$

The main pole of main amplifier is given by:

$$P_1 = \frac{1}{R_{out}C_L} \tag{6}$$

The C_L is the sum of the load capacitor and the transistor parasitic capacitor in the output.
The unit-gain bandwidth product of main amplifier is described by:

$$GBW = A_V P_1 = \frac{A_V}{R_{out}C_L} = \frac{g_{m3}}{C_L} \tag{7}$$

From (7), the larger unite-gain bandwidth is decided by g_{m3}, the greater this transconductance, the boarder the unit-gain bandwidth. The single-ended output swing voltage of main amplifier is decided by:

$$V_{DD} - (V_{OD8} + V_{OD10} + |V_{OD6}| + |V_{OD4}|) \tag{8}$$

The V_{OD} is the overdrive voltage of transistor.
The single-ended slew rate is decided by:

$$SR = \frac{I_{SS}}{2C_L} \tag{9}$$

From (9), large tail current can achieve large slew rate, but it also will increase power consumption.
The common mode rejection ratio (CMRR) of main amplifier can be described by:

$$A_{V,CMRR} = \frac{A_V}{A_{V,CM}} \tag{10}$$

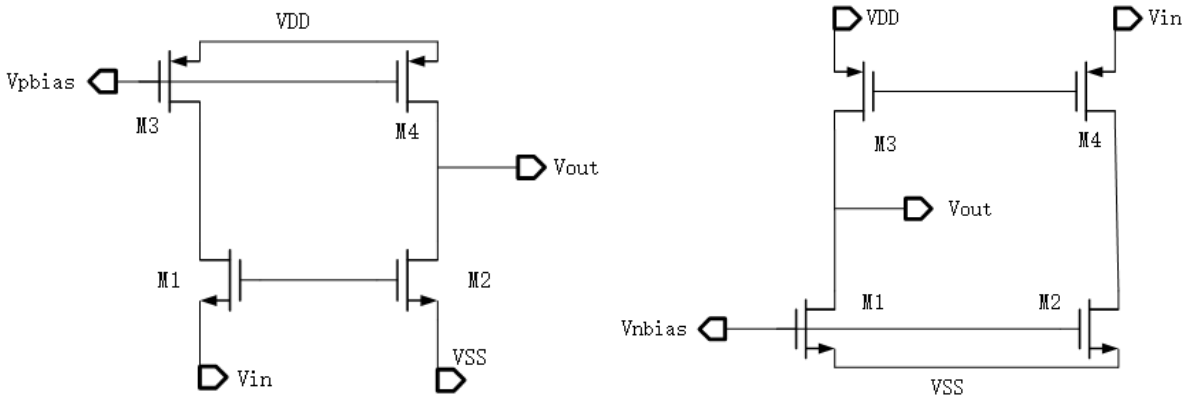
The power supply rejection ratio (PSRR) of main amplifier can be described by:

$$A_{V,PSRR} = \frac{A_V}{A_{V,Vdd}} \tag{11}$$

From (10), (11), large voltage gain A_V can improve CMRR and PSRR.

2.3. Auxiliary amplifier

Figure.3 shows the schematic of auxiliary amplifier in this design. If a simple common source amplifier is used directly as the auxiliary amplifier, the gate-source voltage of input transistor will limit the output voltage swing of main amplifier. In order to solve this issue, in Figure. 3(1), a source follower M1 as the first stage to avoid this situation. In second stage, M2 as a simple common source amplifier to provide gain. M3 and M4 provide bias current for M1 and M2 respectively. The bias voltage of auxiliary Vpbias and Vnbias is same as the bias voltage of main amplifier, which save some area and power consumption.



(1) Auxiliary amplifier for NMOS (2) Auxiliary amplifier for PMOS

Figure 3. Auxiliary amplifier schematic (Photo/Picture credit: Original)

2.4. Common mode feedback circuit

Common-mode feedback circuit can be divided into switched-capacitor common-mode feedback and continuous time common-mode feedback. Switched-capacitor common-mode feedback have no influence on the output voltage swing of main amplifier, high linearity, but it introduces more noise and load. So, this design adopts continuous time common-mode feedback.

Figure.4 shows the common-mode feedback circuit in this design. In this design, to achieve as large as possible output voltage swing, the common-mode voltage is chosen to 0V, so there is no reference voltage in the schematic of CMFB. The structure of proposed CMFB is that two source followers are cascaded. Input transistor in first stage is NMOS and that is PMOS in second stage, M1 and M3 provide bias current for M2 and M4 respectively. Comparing to single source follower, this structure follows the output voltage closer.

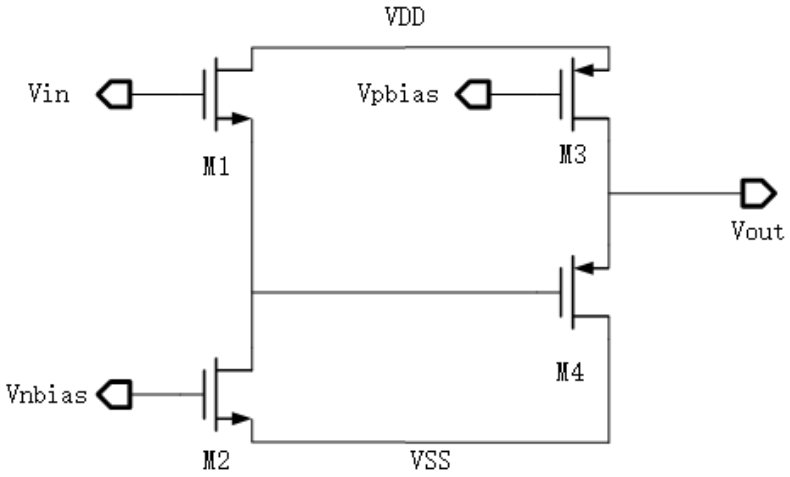


Figure 4. Common-mode feedback schematic (Photo/Picture credit: Original)

2.5. Bias circuit

The bias circuit adopt width swing cascode structure [10]. All the bias voltage are generated by a reference current source.M2 and M6 work in linear region and the result transistors work in active region. The size of all the transistors need to match the transistors in amplifier circuit except M2 and M5. The width of M2 is the same width as M1 and the width of M5 is same as M6. To make sure M4 and M8 work in active region and get proper bias voltage, the length of M2 and M5 need to be carefully determined (Fig 5).

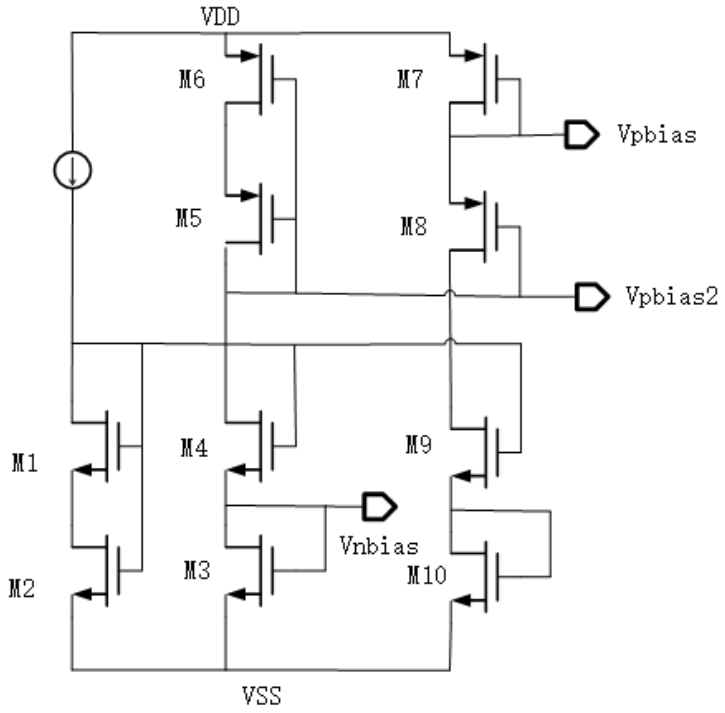


Figure 5. bias circuit schematic (Photo/Picture credit: Original)

3. Simulation Result

This design is based on TSMC 0.18μm CMOS process, and simulation tool is Cadence spectre. The supply voltage VDD is 1V and VSS is -1V, the load capacitor is 2pF, and all the corner is FF.

Figure.6 shows the AC gain & phase simulation result, from which the DC gain is 100.573dB, phase margin is about 66.029 deg, and the unit-gain bandwidth is 333.268MHz.

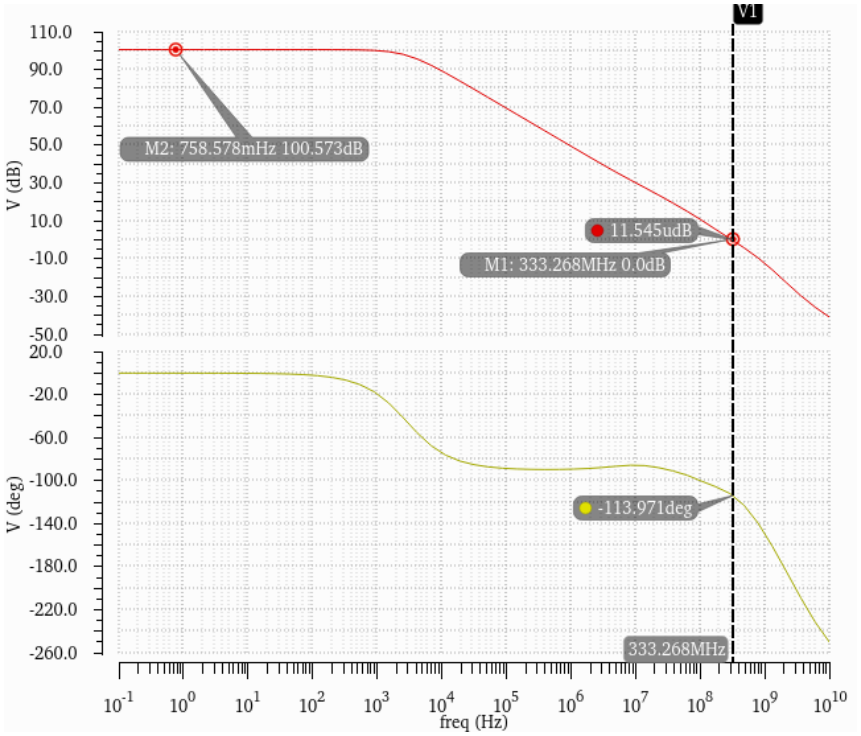


Figure 6. fully differential amplifier AC gain & phase simulation result (Photo/Picture credit: Original)

Figure.7 shows the simulation result for test differential output voltage swing. When output voltage is from -1.89148V to 1.89147V, the curve is linear. So, the full differential output swing of proposed differential amplifier is about 3.78V.

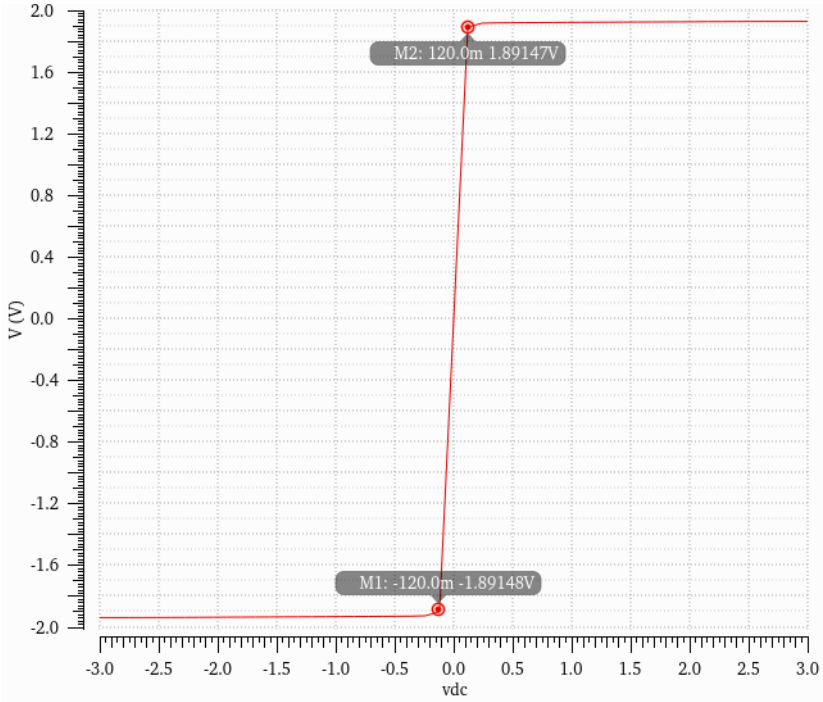


Figure 7. differential output voltage swing of proposed amplifier simulation result (Photo/Picture credit: Original)

Figure.8 shows the simulation result for test differential slew rate. A stand for 10% stable high-level voltage, and B stands for 90% stable high-level voltage. The differential slew rate of proposed amplifier is about 287.13V/μs.

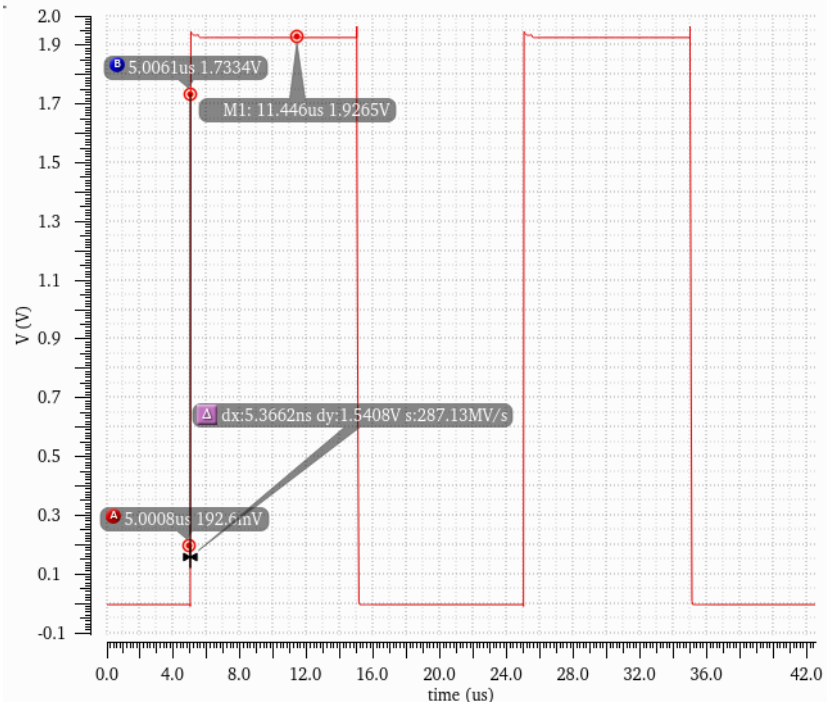


Figure 8. differential slew rate simulation result (Photo/Picture credit: Original)

Figure.9 shows the simulation result of common mode rejection ratio (CMRR). It indicates the CMRR of proposed amplifier is about 114.7dB at low frequency.

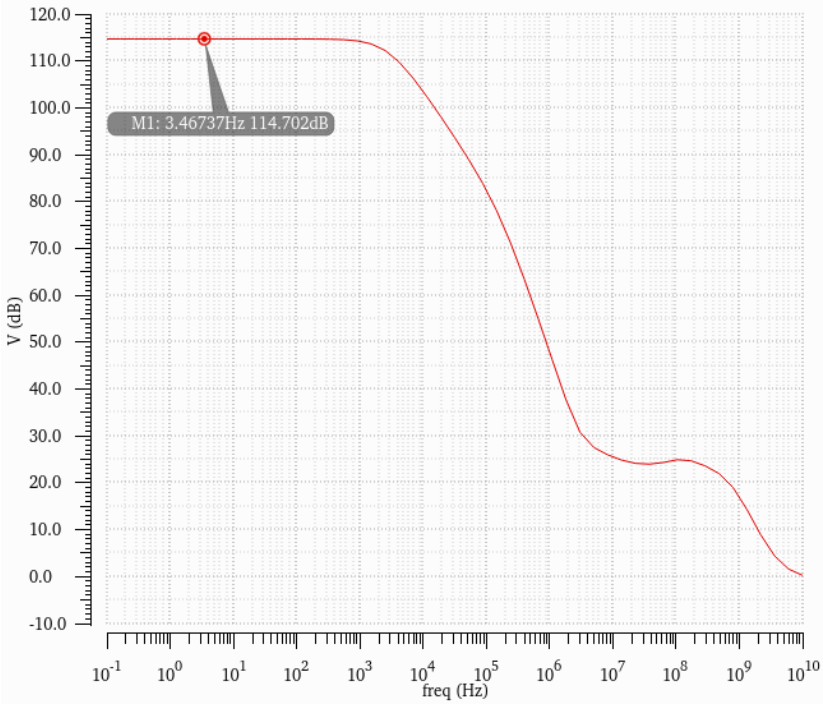


Figure 9. common mode rejection ratio simulation result (Photo/Picture credit: Original)

Figure.10 shows the simulation result of power supply rejection ratio (PSRR). It indicates the PSRR of proposed amplifier is about 122.85 dB at low frequency.

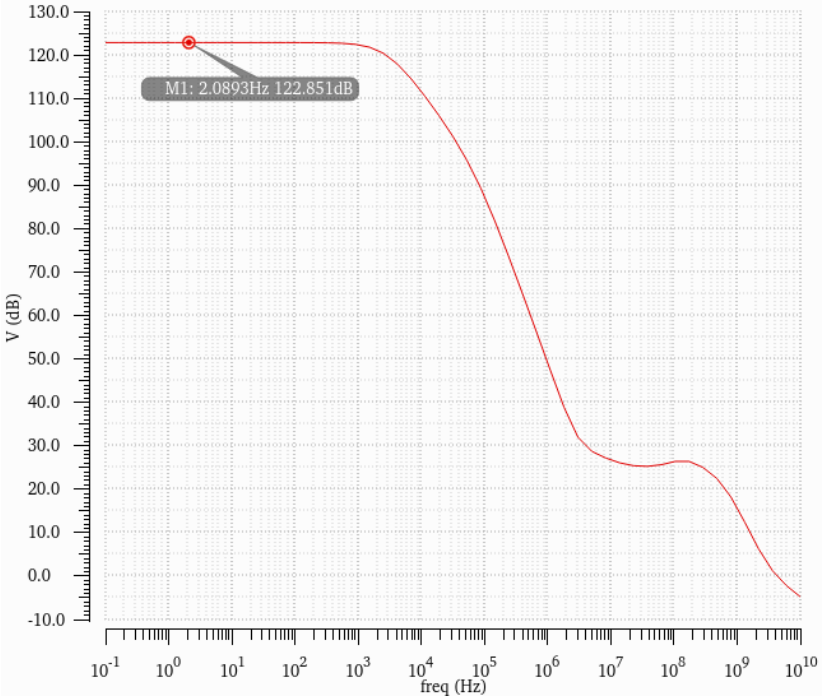


Figure 10. power supply rejection ratio simulation result (Photo/Picture credit: Original)

Figure.11 shows the simulation result of input reference noise. It indicates the input reference noise of proposed amplifier is about 6.2 nV/$\sqrt{Hz}$ at1MHz.

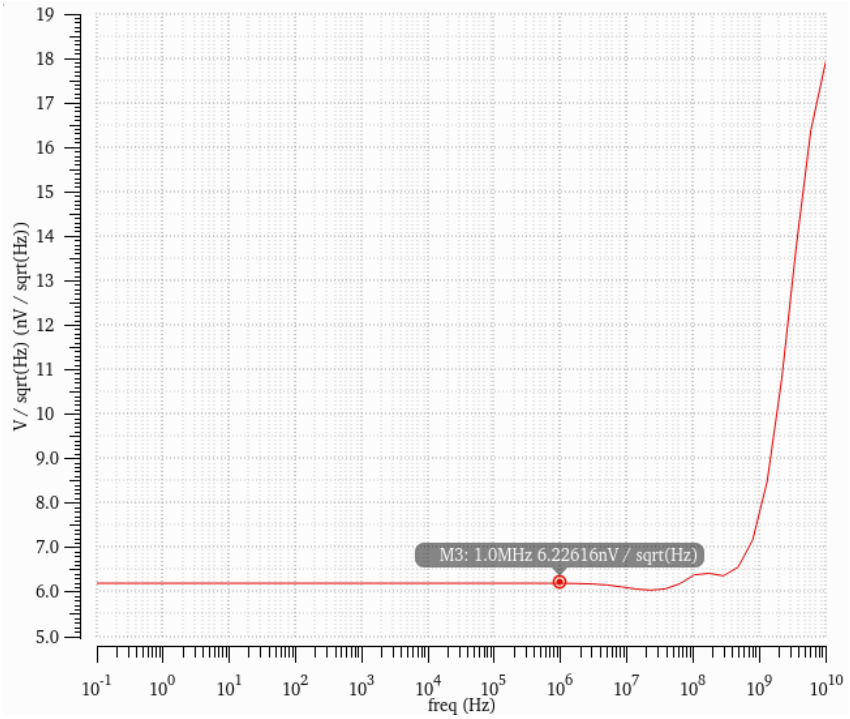


Figure 11. Input reference noise simulation result (Photo/Picture credit: Original)

Table 1 summarize all the specifications and simulation results of proposed amplifier. All the parameters meet the specification.

Table 1. The Parameter summary of proposed fully differential amplifier

Parameters	Specifications	Simulation results
Supply Voltage	+/- 1.0 V	+/- 1.0 V
Power Consumption	≤ 2.0 mW	1.6mW
DC gain	≥ 80 dB	100.572 dB
Slew Rate	≥ 80 V/μs	287.13V/μs
Phase Margin	≥ 60 deg	66.029 deg
Unit-gain bandwidth	≥250MHz	333MHz
CMRR	≥ 80 dB	114.702 dB
PSRR	≥ 80 dB at dc	122.85 dB at dc
Differential Output Swing	≥ +/- 1.2 V	+/- 1.89 V
Total Harmonic Distortion	≤3%	1.05%
Equivalent Input Noise	≤ 10nV/$\sqrt{Hz}$ at 1MHz	6.2nV/$\sqrt{Hz}$ at 1MHz

4. Conclusion

This paper designs a fully differential amplifier for switched-capacitor application, such as switched-capacitor filter and pipeline analog-to-digital converter. The proposed amplifier was used in TSMC 0.18μm CMOS technology and it can work with supply voltage VDD at 1V and VSS at -1V, its common mode level is 0V. The proposed amplifier adopts fold cascode structure and gain boosting technology, which make it have higher gain and larger output swing. The structure of auxiliary amplifier is very simple, it is a source follower cascades a common source amplifier, but it is effective and saves power consumption. The CMFB circuit is that two source followers are cascaded, it can adjust the current flow tail current source according to output voltage. The simulation results show the proposed amplifier meet all the specification.

With the development of advanced manufacturing processes, the reduction of transistor length and low supply voltage brings great challenges to the design of amplifiers due to the decrease in intrinsic gain. How to scale op amps as the manufacturing process advances is a direction of future development.

References

[1] Fried D L. Analog sample-data filters. IEEE Journal of Solid-State Circuits, 1972, 7 (4): 302 - 304.

[2] Dong-Ying Y, Shih-Hao K, Yong-Long S, et al. An Improved 48-to-12V Series-Parallel Resonant Switched-Capacitor Converter for Data Center Applications, 2021 IEEE International Future Energy Electronics Conference (IFEEC). IEEE, 2021: 1 - 6.

[3] Taghizadeh H, Cross A M, Whitehouse R, et al. Switched capacitor DC-DC converters for HVDC applications. 2015.

[4] Singh D, Sandeep N. A Switched-Capacitor-Based Multi-Source Multilevel Inverter for High-Frequency AC Applications, 2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT). IEEE, 2022: 1 - 6.

[5] Allen P E, Dobkin R, Holberg D R. CMOS analog circuit design. Elsevier, 2011.

[6] Wakaumi H. A Switched-Capacitor Low-Pass Filter with Multiple-Channel Double-DSB OP Amplifiers, 2021 International Conference on Electronics, Information, and Communication (ICEIC). IEEE, 2021: 1 - 4.

[7] Ghoshal P, Sen S K. Realization of a 1.5 bits/stage pipeline ADC using switched capacitor technique, 2016 International Conference on Intelligent Control Power and Instrumentation (ICICPI). IEEE, 2016: 65 - 66.

[8] Razavi B. Design of analog CMOS integrated circuits. Tsinghua University Press Limited, 2005.

[9] Berntsen O, Wulff C, Ytterdal T. High speed, high gain OTA in a digital 90nm CMOS technology, 2005 NORCHIP. IEEE, 2005: 129 - 132.

[10] Abo A M. Design for reliability of low-voltage, switched-capacitor circuits. University of California, Berkeley, 1999.