Trade-offs Between Delay and Energy in 4-Bit Absolute Value Detector and its application analysis

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Abstract. With the rapid advancements in digital signal processing and communication technology, the utilization of digital detectors has become prevalent across numerous domains. Among these detectors, absolute value detectors hold particular significance. This article primarily delves into the delicate balance between latency and energy consumption within the realm of 4-bit absolute value detectors. To commence, we provide an exhaustive exposition of the fundamental design and operational principles underpinning absolute value detectors. Subsequently, we embark on a comprehensive comparison of various optimization approaches, with a special focus on their efficacy concerning energy consumption and latency. The research endeavors have unveiled that the detector's optimal aspect ratio, as well as the choice of novel materials like graphene and silicon germanium, can wield a substantial influence over its performance. As its peer into the horizon, it is evident that the continuous evolution of new materials and cutting-edge technologies promises further enhancements in the performance of 4-bit absolute value detectors.

Keywords: Absolute value detectors; optimization; latency; energy consumption; new materials.

1. Introduction

With the rapid development of digital signal processing and communication technology, digital detectors are widely used in many fields. Among them, the absolute value detector is particularly critical because it plays a central role in signal processing, image analysis, and various communication systems [1]. As technology evolves, how to find the balance between latency and energy, especially in the field of microelectronics and embedded systems, has become an urgent problem to be solved. Because in these systems, energy efficiency and processing speed are critical performance indicators.

This paper will focus on the trade-off between latency and energy in 4-Bit absolute value detectors. Firstly, the basic design and working principle of the absolute value detector are introduced in detail. Next, different design approaches are compared, paying particular attention to their performance in terms of energy consumption and latency. Finally, the most efficient design method among them is adopted, aiming at finding an optimal balance point between these two key performance indicators. The significance of this paper is to provide new design strategies for high-performance and fast digital systems.

2. Absolute value detector principle and circuit

2.1. Basic Principle

An absolute value detector is a circuit or mathematical operation that calculates the absolute value of a given input signal regardless of its polarity (positive or negative). The absolute value of a number is its distance on the number line from zero, which is always a positive number or zero. In mathematical notation, the absolute value of a number “x” is represented as |x|. The principle of an absolute value detector depends on the application and field of use.

In the context of analog signals, absolute value detectors are typically implemented using precision rectifiers and op amps. A precision rectifier is a circuit that rectifies an input signal and amplifies it with unity gain. This effectively converts the negative part of the input signal to its positive

counterpart, allowing the absolute value to be calculated. The output of the precision rectifier is the absolute value of the input signal.

In digital signal processing, the absolute value of a digital signal can be calculated using different methods, such as subtracting the signal from zero if the input is negative and leaving it unchanged if the input is positive. Additionally, bitwise operations can be used to manipulate the sign bit. The exact method depends on the hardware or programming language used. The structure of a basic absolute value detector is shown in the figure 1 below.

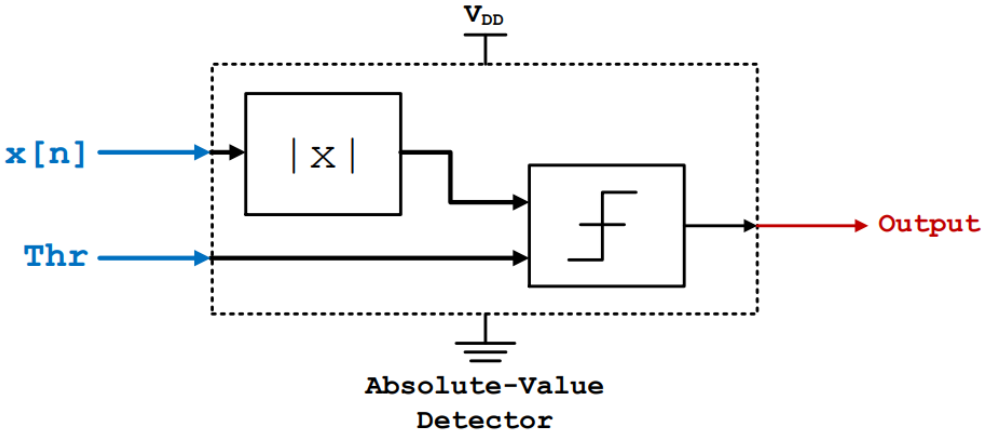


Fig 1. Structure of a basic absolute value detector (Photo/Picture credit: Original).

It can be seen from the structure diagram that the absolute value detector is mainly composed of the following two parts: Absolute value calculation part and threshold comparison part. The goal of absolute value calculation part is to calculate the absolute value of the input signal. It converts the negative part of the input signal to its positive counterpart. In threshold comparison part, the calculated absolute value signal will be compared with the preset threshold. If the absolute value signal is greater than the threshold, the output will be a high logic value "1"; otherwise, the output will be a low logic value "0" [2].

2.2. Principle of 4-bit absolute value detector

A 4-bit absolute value detector is a circuit or logic component used to determine the absolute value of a 4-bit binary number. In other words, it evaluates the positive value of the input regardless of whether the input is positive or negative. The rationale behind this detector involves analyzing the sign bit of the input number and performing appropriate operations to generate the absolute value.

A 4-bit absolute value detector functions based on the principles of two's complement binary number representation. Typically, for 4-bit input binary numbers, the most significant bit (MSB) serves as an indicator of the number's sign. A 0 in the MSB denotes a positive number, whereas a 1 indicates a negative one. When the MSB is 0, showing that the input is positive, the absolute value remains unchanged from the input. However, for negative numbers where the MSB is 1, the process of determining the absolute value involves a few more steps. First, acknowledging the MSB of 1 indicates that the number is negative. Next, the bits of the number are inverted. For instance, a bit sequence of 0010 would become 1101. Finally, 1 is added to the inverted value, turning 1101 to 1110, which, in this example, corresponds to the decimal value of 3 [3]. This resulting sequence then represents the absolute value of the original negative input.

2.3. Circuit Analysis

2.3.1. Circuit Topology

The entire absolute value detector circuit is showed in figure 2. It is composed of three parts, the left part is composed of XOR gate and half adder, which is used to obtain the amplitude of the signal. In the middle, there are two multiplexers, and the right part is a comparator, which is compared with the set threshold. The circuit style is static CMOS.

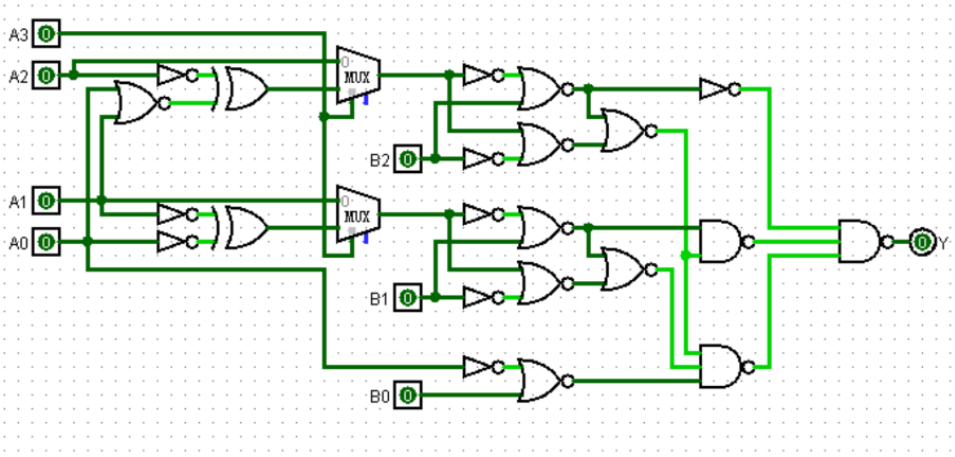


Fig 2. Circuit Diagram of 4-bit absolute value detector (Photo/Picture credit: Original).

2.3.2. MUX

In a 4-bit absolute value detector, the purpose of the multiplexer is to select one of the two input signals as the output. In the context of an absolute value detector, a multiplexer is used to compare the absolute value to a threshold and then determine the logic state ("1" or "0") of the output. The following figure 3 is the MUX in this design.

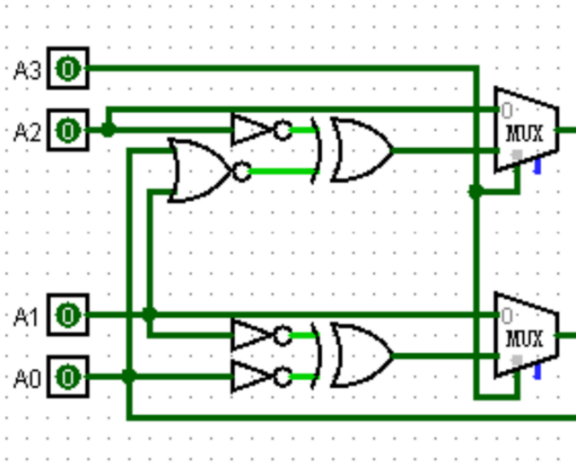


Fig 3. MUX (Photo/Picture credit: Original).

From the graph, if the A3 is 0 which means the value is positive, and the multiplexer will output A2A1A0, and if the A3 is 1 which means the value is negative, and the multiplexer will output S2S1S0.

2.3.3. Half adder

A half adder is an essential component in digital circuitry that functions to add two individual input bits, yielding two output bits. One output bit signifies the sum while the other indicates the carry. Within the context of a 4-bit absolute value detector, the half adder can be instrumental in calculating the sum of the absolute value signals. For instance, when dealing with the absolute value signal, A, and a threshold, B: if A is greater than or equal to B, the difference is found by subtracting A from B, resulting in (A - B). Conversely, when A is less than B, the difference is determined by subtracting B from A, giving (B - A). In both situations, the half adder plays a crucial role in computing the difference, generating a result bit and, if necessary, a carry bit.

2.3.4. Comparator

A comparator is a circuit component that compares the magnitude relationship of two inputs and produces a corresponding output signal indicating which input is greater than, less than, or equal to the other input. In a 4-bit absolute value detector, a comparator may be used to compare the sum (or

difference) of the absolute value signal to a preset threshold. If the sum of the absolute value signals is greater than the threshold value, the comparator will output a signal indicating that the absolute value signal is greater than the threshold value. If the sum of the absolute value signals is less than or equal to the threshold value, the comparator outputs a signal indicating that the absolute value signal is less than or equal to the threshold value [4].

3. Calculation and Optimization

3.1. Analysis of Logical Effort and Parasitic Effort

3.1.1. Analysis of Logical Effort

Logic delay analysis is a critical step in ensuring that circuits meet performance requirements while minimizing delays. First, select the appropriate logic gates to meet the design requirements. In this project, the aim is to increase the latency to 50% of the lowest latency, which is 1.5 times. Using the logic delay metric to calculate the delay of different logic gates to ensure that the selection of logic gates will meet this goal. Next, by cascading logic gates, optimize latency. Increasing the number of logic gates cascaded may reduce the overall delay, but also at the expense of greater power consumption. Here, weighs the relationship between delay and power consumption, and choose the appropriate number of cascades to minimize power consumption while meeting the delay requirement.

3.1.2. Parasitic Effort

Parasitic effort analysis considers effects such as parasitic capacitance and parasitic resistance in the circuit to optimize circuit performance and power consumption. Especially parasitic capacitance. These parasitic capacitances increase propagation delay and increase power consumption. With proper physical layout and line design, by reducing the effects of parasitic capacitance and thus optimize circuit performance. In addition, power consumption can be reduced by considering the effect of parasitic resistance on power consumption. Through optimization of supply voltage and power management strategies, power consumption can be reduced while maintaining performance.

3.2. Path Effort and Input Capacitance Calculation

3.2.1. Path effort calculation

Path effort calculations are designed to assess the propagation delay within a logic path, an indicator of a circuit's logic complexity. One way to gauge this is through the “logical effort,” which stands for the ratio of a specific logic gate's delay to that of a standard gate. This ratio effectively offers a metric to determine the intricacy of the logic path. To compute the path effort, one would begin by determining the total delay of the path, taking into account the selected logic gates and any cascade optimizations. Next, by selecting a standard logic gate as a reference, its delay is computed. Subsequently, the logic effort is ascertained by dividing the path's total delay by the delay of this reference gate [5]. It's noteworthy that a higher path effort signifies a more substantial quantity and complexity of logic gates in the path, which consequently leads to increased propagation delay.

3.2.2. Critical path analysis

The critical path is the path with the longest propagation delay in the circuit, which determines the maximum response time of the entire circuit which is shown in figure 4.

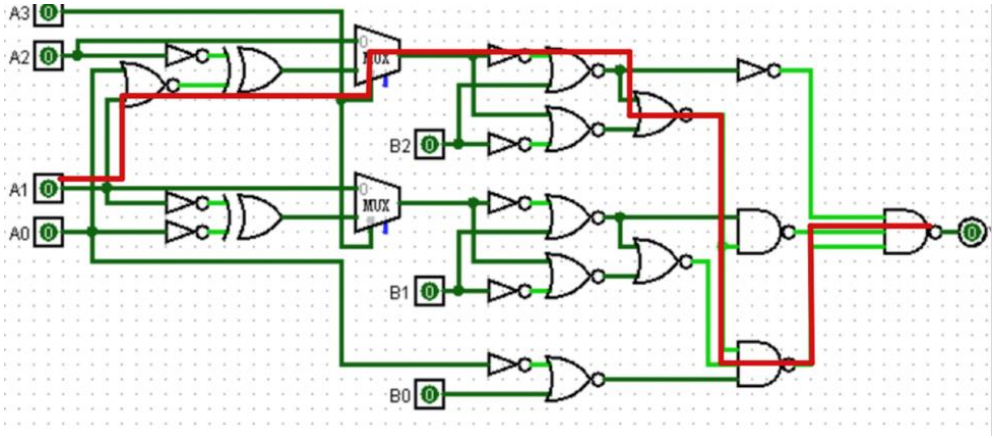


Fig 4. Critical path of the circuit (Photo/Picture credit: Original).

The red line marked in the figure is the critical path of this design. Assume that there is an inverter chain at each input as Cin, and assume that the output load is 32Cin load. Finally, the schematic of critical path circuit is showed above.

3.2.3. Critical path delay calculation

From figure 5, an inverter is used as an input load before the input port, and its capacitance is Cin. A capacitive load with a capacitance 32 times the input capacitance is connected after the output port.

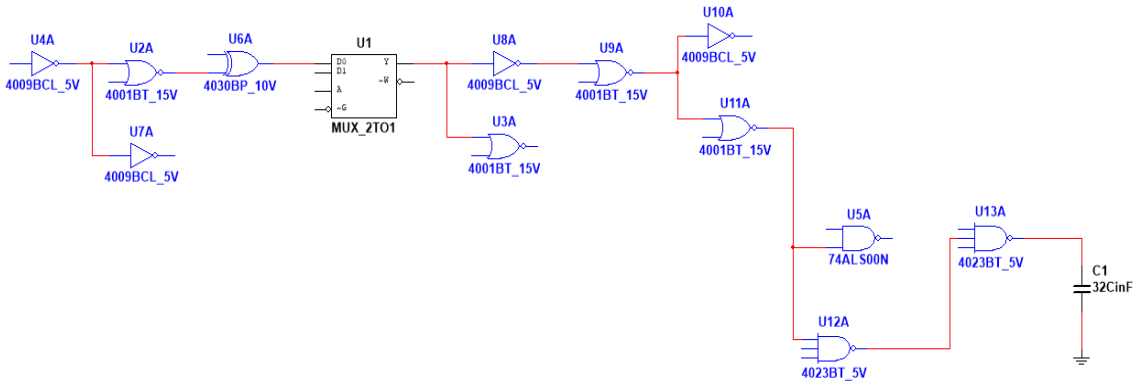


Fig 5. Critical path circuit schematic (Photo/Picture credit: Original).

Based on this configuration, the entire critical path is divided into 9 stages, and the output load reaches 32 times the input load. Also, when calculating latency, the 3 branches in the critical path need to be considered. All NAND and NOR gates in the system are designed in complementary CMOS. For an inverter of unit size, its P-channel transistor width (Wp) is 650nm, its N-channel transistor width (Wn) is 430nm, and the lengths of both P-channel and N-channel transistors (Lp and Ln) are 100nm.

$$g = \frac{R_{gate} \times C_{in,gate}}{R_{Inv} \times C_{in,Inv}} \tag{1}$$

$$h = \frac{C_{out}}{C_{in,gate}} \tag{2}$$

$$p = \frac{C_{par,gate}}{C_{par,Inv}} \tag{3}$$

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}} \tag{4}$$

These are required equations; with these equations the table 1 can be obtained below [6].

Table 1. Logic effort and parasitic effort for each gate.

Gate	Logic effort (g)	Parasitic effort (p)
Not	1	1
Nand2	1.398	2
Nor2	1.602	2
Nand3	1.296	3
Xor2 with MUX	8	5.398

3.2.4. Input Capacitance Calculation

The input capacitance calculation is intended to evaluate the load capability and response time of the circuit. The input capacitance is mainly composed of capacitive elements and line capacitance in the circuit, which has an important impact on signal transmission speed and power consumption. In this project the input capacitance needs to be calculated.

Input capacitance can generally be divided into static capacitance and dynamic capacitance. Static capacitance comes from the input capacitance of the logic gate, while dynamic capacitance depends on how often the signal changes [7]. In this project static capacitance is a critical point.

To compute the input capacitance, one would begin by estimating the logic gate's input capacitance based on its design. This estimation can be derived from the physical attributes and parameters of the logic gates. Furthermore, when the circuit incorporates cascaded logic gates, it's crucial to factor in the input capacitance of these cascaded gates to obtain an accurate total input capacitance. After calculation, the data of input capacitance is shown in the table 2 below.

Table 2. Logic effort and parasitic effort for each gate.

Stages	C_{in}
1	0.9995
2	2.0056
3	4.0789
4	13.2952
5	2.0814
6	6.7827
7	8.4958
8	9.7199
9	17.6362

3.3. Sizing and Vdd Optimization

Usually, based on previous calculations, the minimum delay can be obtained for the circuit design. However, the final decision is to make a compromise in reducing overall energy consumption by sacrificing latency. The maximum latency which can be accepted is 1.5 times the current minimum latency. In this case, assuming that the delay is proportional to the supply voltage Vdd, which can be expressed by equation (5). Note that the maximum supply voltage is 1.

$$Delay = \frac{k \times V_{dd}}{(V_{dd} - V_T)^2} \tag{5}$$

Then substitute the calculated values in to get the minimum voltage value.

$$Delay_{\min} = \frac{k \times 1}{(1-0.2)^2} \tag{6}$$

$$1.5Delay_{\min} = \frac{k \times V_{dd,\min}}{(V_{dd,\min} - V_T)^2} \tag{7}$$

By solving equations (6) and (7), a minimum voltage of 0.7751V can be obtained.

3.4. Latency and energy consumption trade-off analysis

The final optimization method is do both sizing and Vdd optimization. When try to do sizing only and Vdd only, but the effect is worse than using these two methods together. Although the critical path delay will increase by 50%, from 60.9 to 91.35, the reduction in energy is the highest when the two methods are used together, reducing by 78%.

4. Applications and Outlook

4.1. Applications

The 4-bit absolute value detector is a versatile component with potential applications spanning a range of fields, due to its capability to swiftly determine the absolute value of a 4-bit binary input. One notable area of application is signal processing. These detectors can play a crucial role in digital signal processing avenues such as audio and image processing [8]. For instance, when integrated into an audio processor, it serves to measure the amplitude of an audio signal, thereby facilitating processes like noise cancellation and audio enhancement. Similarly, in the realm of image processing, the detector proves instrumental for tasks like edge detection and feature extraction, making it a valuable tool for computer vision applications.

Another significant field of application for the 4-bit absolute value detector is in communication systems. Here, the detector assists in assessing signal quality and detecting errors. By computing the absolute value of signal variations, it becomes possible to pinpoint amplitude distortions or phase shifts. This, in turn, bolsters the reliability and integrity of data transmission [9].

4.2. Outlook

The advent of 4-bit absolute value detectors ushers in a realm of intriguing possibilities for both academic research and real-world applications. One such avenue worth exploring is the creation of high-precision variants of these detectors. By expanding beyond the 4-bit range and increasing bit width, researchers could harness higher precision, catering to applications demanding meticulous calculations.

Moreover, in an era emphasizing energy-efficient computing, there's potential in tailoring these detectors for low-power implementations. Such energy-conscious designs would be aptly suited for integration into battery-powered devices, IoT sensors, and other systems where power conservation is paramount [10]. In tandem with this, considering the foundational role absolute value computations hold in numerous machine learning algorithms, there's an opportunity to delve into integrating these detectors within hardware accelerators for neural networks. This could potentially expedite model training and inference processes while also enhancing energy efficiency.

5. Conclusion

By designing and testing the 4-Bit absolute value detector, choosing the most suitable optimization method is obviously the optimal solution that can affect its delay and energy consumption. But in addition, it is possible that the aspect ratio of the detector also largely affects its latency and energy consumption. An aspect ratio that is too wide or too narrow may result in suboptimal performance. Additionally, material choice can also have a significant impact on latency. By adopting new materials with high conductivity and low energy consumption, such as Graphene, Silicon Germanium, etc., it may be possible to significantly reduce the delay of absolute value detectors. Looking forward to the future, with the continuous development of new materials and technologies, the performance of the 4-Bit absolute value detector can be further optimized, making it more widely used in the fields of digital signal processing and communication.

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