Consumption Analysis and Optimization Strategies for Four-Bit Absolute-Value Detectors

Haokang Jin *

Detroit Green Technology Institute, Hubei University of Technology, Wuhan, 430000, Hubei, China

* Corresponding Author Email: 2111621108@hbut.edu.cn

Abstract. As embedded systems, communication systems, and neurology research continue to advance, the demand for high-performance components in digital circuits has risen. Simultaneously, there is a growing need for low-energy consumption. In this paper, Four-Bit Absolute-Value Detectors, as crucial components in digital circuits, have garnered significant attention for their role in achieving energy efficiency. This paper embarks on a comprehensive exploration, commencing with the fundamentals of circuit theory, circuit topologies, and circuit styles. Through extensive calculations and comparative studies, this paper conduct a thorough analysis of the factors influencing energy consumption in these circuits. The study reveals that various parameters have a substantial impact on energy consumption. To mitigate this, the author proposes multiple strategies, including gate size optimization, supply voltage optimization, and the selection of appropriate circuit styles. The significance of this study lies in providing foundational insights into the energy optimization of Four-Bit Absolute-Value Detectors. By investigating the interplay between gate sizes, supply voltage, path length, capacitance load, and circuit topology, this paper offer a holistic perspective on energy-efficient design.

Keywords: Four-Bit Absolute-Value Detector, Digital circuits, Energy Consumption, Energy Optimization

1. Introduction

In today's digital age, the demand for efficient and power-conscious electronic devices has become paramount. Absolute value detectors, as crucial components of digital circuits, play a pivotal role in various applications ranging from signal processing to communication systems [1]. With the increasing integration of electronic components in everyday life, the need for energy-efficient designs has gained significant importance. As a result, exploring strategies to optimize the energy consumption of such detectors has emerged as a vital research endeavor [2]. This paper delves into the realm of energy analysis and optimization for four-bit absolute value detectors, addressing the pressing need for sustainable and high-performance electronic systems.

This paper is focused on the analysis of energy consumption and energy optimization strategies for four-bit absolute value detectors. This paper will commence by delving into the operational principles of these detectors. Through a comprehensive review of existing four-bit absolute value detectors, this paper will conduct comparative analyses, dissecting circuit architectures and parameters such as logic gate sizes to illustrate how energy is consumed within these detectors. Subsequently, this paper will delve into exploring energy consumption using energy calculation formulas and circuit structures, elucidating calculation principles and preliminary optimization approaches. Through practical examples, this paper will provide tangible insights into energy consumption characteristics. Concluding this section, this paper will outline a holistic approach and direction for optimizing detector energy consumption and offer a summary and conclusion.

The content of this paper will provide fundamental insights into energy optimization for detectors, offering foundational concepts and references for future optimization strategies.

2. Basic Theory Analysis

2.1. Principle of the detector

The Four-Bit Absolute-Value Detector, as a vital component in digital circuitry, holds substantial importance in terms of energy consumption and optimization. Modern implementations of the Four-Bit Absolute-Value Detector are typically constructed using CMOS and Pass-Transistor Logic (PTL) circuits. These implementations comprise various combinational logic gates and gate devices [3]. Primarily, the detector can be divided into two main sections: the absolute value determination and the comparator, each presenting distinct energy consumption aspects.

The conventional Four-Bit Absolute-Value Detector commonly consists of two components. The first part pertains to the absolute value determination [4]. This segment employs devices such as full adders and half adders to ascertain the absolute value of the input. The energy consumption in this phase predominantly stems from logic gate transitions, logic gate currents, and transmission line capacitance. The switching and dynamic power resulting from logic gate transitions become prominent at higher frequencies, particularly during complex operations. Logic gate currents also contribute to energy consumption, especially when logic gates are active. Although the energy impact of transmission line capacitance is relatively minor, its significance becomes pronounced under conditions of frequent signal transmission and substantial voltage fluctuations.

The second part is the comparator section, typically composed of multiple logic gate circuits [5]. Here, energy considerations are closely linked to logic gate sizing and supply voltage. Increasing logic gate sizes may raise switching power, yet it can expedite transitions and consequently lower dynamic power. Lowering supply voltage reduces switching power but concurrently affects circuit performance.

In terms of optimization strategies for the detector, several avenues can be explored. In logic gate circuits, selecting low-power logic styles, rational logic gate size choices, and appropriate supply voltage settings can mitigate switching power [6]. Concerning transmission line capacitance, adopting low-power driving techniques, reducing signal frequencies, and addressing transmission line capacitance-induced energy consumption should be considered.

Thus, the energy consumption of the Four-Bit Absolute-Value Detector is primarily influenced by logic gate transitions, logic gate currents, and transmission line capacitance. By tailoring strategies to the different sections through prudent logic gate sizing, voltage selection, and transmission line optimizations, effective energy reduction can be achieved.

The Four-Bit Absolute-Value Detector functions as a crucial element within digital circuitry to determine the absolute value of a 4-bit binary input. The operational process involves two distinct sections: the absolute value determination and the comparator. In the absolute value determination section, the input value's absolute magnitude is ascertained. This is accomplished by analyzing the most significant bit (MSB) of the input. If the MSB is '0', indicating a positive number, the input value is directly passed through to the output. Conversely, if the MSB is '1', signifying a negative number, the input is inverted using the two's complement method, followed by an addition of '1'. This process ensures the extraction of the absolute value through a series of logical operations involving full adders, half adders, and combinational logic gate circuits.

The comparator section operates by utilizing multiple logic gate circuits to determine the relative magnitudes of two absolute values. The absolute values of two inputs are fed into the comparator, which subsequently assesses their sizes. The comparator outputs a comparison result that indicates which of the two absolute values is larger. Based on the principles, it can derive the truth tables for the absolute value determination segment as well as obtain the truth tables, shown as Table 1.

Table 1. True table of the AVD.

Carry in (four bits)	Carry out (four bits)
0000	0000
0001	0001
0010	0010
0011	0011
0100	0100
0101	0101
0110	0110
0111	0111
1000	1000
1001	0110
1010	0101
1011	0100
1100	0011
1101	0010
1110	0001
1111	0000

And according to the principle of comparator, this paper can get its logical function:

$$(A > B) = A_3\overline{B_3} + X_3A_2\overline{B_2} + X_3X_2A_1\overline{B_1} + X_3X_2X_1A_0\overline{B_0}, where X_i = A_iB_i + \overline{A_i}\,\overline{B_i} \tag{1}$$

2.2. Structural analysis of current four-bit absolute-value detectors

2.2.1. Energy and Related Parameters of Two Absolute Value Detectors:

The V_{DD}^{opt} is optimal voltage for the V_{DD} in the range of 0v -1v. This voltage also satisfies the requirements that the maximum delay is 1.5 minimum delays. As the following formula shown, this paper calculate the V_{DD}^{opt} by using t_p:

The optimal voltage range for the V_{DD} falls between 0 volts and 1 volt, meeting the condition of ensuring that the maximum delay is no more than 1.5 times the minimum delay. As demonstrated in the following formula, this paper compute the V_{DD}^{opt} utilizing t_p:

$$t_p = \frac{CV_{DD}}{K'(V_{DD} - V_T)^2}, K' = \frac{W}{L}K. \tag{2}$$

According to the situation that the maximum delay is 1.5 minimum delays, it preset $V_{th} = 0.2V$:

$$D \propto \frac{V_{DD}}{(V_{DD} - V_T)^2}. \qquad V_{DD}^{opt} = 0.7758. \tag{3}$$

It can obtain the total circuit energy consumption for various supply voltages (Vdd) scenarios Energy consumption when $V_{DD} = 1v$

$$E = C_l V_{DD}^2 = 32.00 \tag{4}$$

Where E is all energy consumption of critical path; C_l is capative load of each logic gate.

The overall energy coumsumption of the circuit

$$E = C_l V_{DD}^2 = 19.26 \tag{5}$$

Additionally, it is essential to take into consideration the logic gate sizes for each stage of this circuit. It get the sizing of the circuit path gates from the Table 2.

Table 2. Circuit Path Gates Sizings.

$C_{inu1}=1.27$	$C_{inu2}=2.05$	$C_{inu3}=4.13$
$C_{inu4}=2.78$	$C_{inu5}=1.87$	$C_{inu6}=3.02$
$C_{inu7}=6.09$	$C_{inu7}=9.83$	$C_{in}9=19.83$

The energy associated with this design pertains to the total energy consumption along the specified critical path. This energy is derived from V_{DD} based on a prescribed probability distribution. To determine the optimal V_{DD}, one must compute it based on the relationship between minimizing energy and delay. The correlation between delay and V_{DD} is as follows:

$$Delay=\frac{Q}{I_D}\propto\frac{C\times V_{DD}}{\beta\times(V_{DD}-V_T)^2} \tag{6}$$

Where Q is the total amount of electric charge; I_D is current; C is capacitance; β is geometric transconductance parameter, where V_T=0.2 V, and for a given device β and C are constants. Given that the 1.5x minimum delay is the maximum delay, the

$$V_{DD}^{opt}=0.78v \tag{7}$$

Where V_{DD}^{opt} is optimized V_{DD}. And it can also get the following related parameters from the Table.3.

Table 3. Minimum energy consumption of each stage.

Stages	1	2	3	4	5
g	1.6	2.6	3.2	2.2	1.8
p	2	10.1	4	4	3
Size	1	2.5	3.83	4.77	8.66
$C_l(C)$	8.5	37.51	25.81	34.67	45.18
$\alpha_{0\to1}$	3/16	1/4	1/4	7/64	903/4096
$E_{\min,delay}$	2.55C	15C	10.32C	6.07C	15.94C
$E_{1.5delay}$	1.55C	9.13C	6.28C	3.69C	9.70C

2.2.2. Comparisons between detectors

To compare the two detectors, this paper get the following data from the table 4.

Table 4. Basic parameters of the two detectors3.

	Five-Stage Four-Bit Absolute Value Detector	Nine-Stage Four-Bit Absolute Value Detector
Logic Gate Sizes	8.5, 37.51, 25.81, 34.67, 45.18	1.2, 2.05, 4.13, 2.78, 1.87, 3.02, 6.09, 9.83, 19.83
Path Stages	5	9
Supply Voltage	$V_{DD}=0.78$	$V_{DD}=0.78$

By incorporating logic gate sizes, capacitance load, and supply voltage into the energy calculation formula, this paper can compute the energy consumption of the two detectors [7]. This comprehensive approach enables us to compare the energy consumption of the two circuits effectively. Furthermore, recognizing that path stages significantly impact energy consumption, this paper understand that an increase in stages leads to a higher number of logic gates involved in the charge-discharge process,

ultimately resulting in elevated energy consumption. Moving to the impact of logic gate sizes, the five-stage circuit features relatively larger logic gate sizes, which may contribute to higher energy consumption per stage. Although larger logic gates exhibit faster switching speeds, they can concurrently lead to increased switching power consumption. Conversely, in the nine-stage circuit, smaller logic gate sizes might correspond to lower energy consumption per stage. However, smaller gates may exhibit slower switching speeds, subsequently causing higher dynamic power consumption. Considering the effect of path levels, the five-stage circuit presents fewer path stages, implying a decreased number of logic gates on the critical path. Consequently, this configuration might lead to reduced switching and dynamic power consumption. In contrast, the nine-stage circuit incorporates more path stages, involving a higher count of logic gates on the critical path, thereby potentially increasing switching and dynamic power consumption. In terms of the influence of supply voltage, both circuits share the same supply voltage of 0.78. Consequently, the energy consumption discrepancy is primarily influenced by capacitance load and logic gate sizes under identical supply voltage conditions. To optimize energy consumption, several strategies can be applied. For the five-stage circuit, potential optimizations involve opting for smaller logic gate sizes to mitigate switching power consumption or selecting a lower supply voltage to minimize dynamic power consumption. Meanwhile, optimizing the nine-stage circuit necessitates striking a balance in logic gate sizes to avoid excessively small sizes that could compromise performance. Adjusting the supply voltage could also be explored.

In conclusion, effective energy optimization strategies should account for logic gate sizes, path stages, and supply voltage collectively to strike the optimal balance between energy consumption and performance. Varied circuit structures and requirements will likely require tailored optimization approaches to achieve the best results.

3. Energy Optimization

3.1. Energy Consumption Calculation and Optimization

When calculating the energy consumption of digital circuits, two primary types of energy consumption are typically considered: static power (static current consumption) and dynamic power [8]. These two forms of power can be calculated using distinct equations and are optimized during the design process.

Static Power: This arises from the energy consumption generated by current flowing through channels while the circuit is in a steady-state condition. Static power is often linked to the magnitude of logic gate currents. It is commonly calculated using the following formula:

$$\begin{aligned} Energy/transiton &= C_L \cdot V_{dd}^2 \\ Power &= Energy/transition \cdot f = f \cdot C_L \cdot V_{dd}^2 \end{aligned} \tag{8}$$

Where Capacitive Load C_L : Capacitance is an element that stores charge and can switch between charging and discharging states. In digital circuits, capacitance primarily arises from logic gate circuits and transmission lines, among others. Larger capacitance implies a greater requirement for energy to charge and discharge; And Supply Voltage V_{DD} : This is the voltage supplied to the circuit, usually maintained at a constant value. Increasing the supply voltage enhances the energy of the charges, consequently leading to higher power and energy consumption; Energy E: Energy represents the amount of energy consumed by the capacitive load Cl during the process of charging and discharging. The unit of energy is typically joules.

Based on the aforementioned equations, this paper can derive initial strategies for energy savings. To begin, one pivotal approach involves the reduction of the supply voltage (Vdd). This action directly correlates with a decrease in energy consumption, given the quadratic relationship between energy and voltage. However, it's crucial to acknowledge that diminishing the voltage might introduce

trade-offs, potentially affecting circuit performance by increasing delay and sensitivity to noise. Striking a balance between voltage reduction and performance optimization is paramount.

Illustrating the relationship between supply voltage and delay can provide a visual grasp of this quadratic interplay. This insightful figure1. further accentuates the importance of this parameter [9].

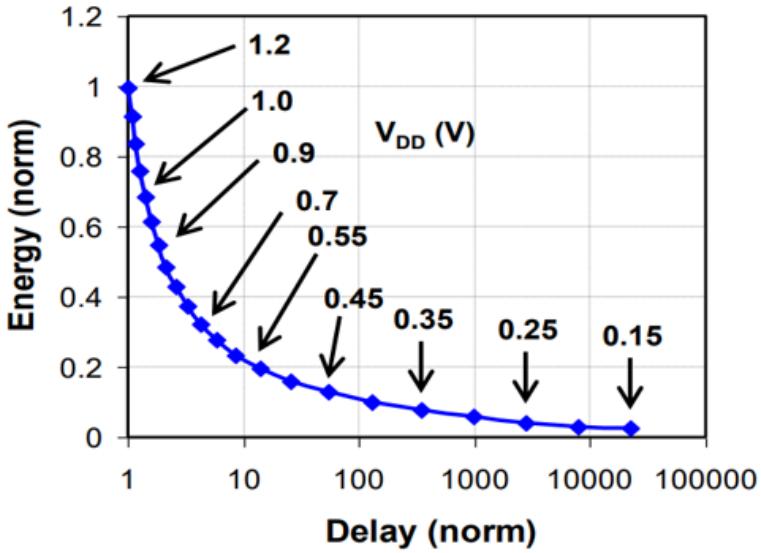


Fig 1. The relationship of energy with supply voltage and delay [9].

Another effective avenue is the reduction of the effective circuit capacitance (C_l). By optimizing the circuit topology, load capacitance can be minimized. Strategies encompassing fewer logic gate stages, streamlined logic paths, and similar measures contribute to the mitigation of load capacitance.

Moreover, the adoption of low-power logic styles like Pass-Transistor Logic (PTL) or Comparator Logic merits consideration. These styles inherently possess lower static and dynamic power characteristics, ensuring a notable reduction in energy consumption.

Given that the energy consumed per CMOS circuit switching event is $C_l \times V_{DD}^2$, it possesses a crucial property where its efficiency improves quadratically when the high transition voltage level is decreased. This paper can define an effective capacitance, denoted as Ceffective, encompassing the transition activity, which equals $\alpha_{0\to1} C_l$, resulting in an average transition energy of $C_{effective} \times V_{DD}^2$. It is evident that after minimizing the high transition level to its maximum extent, the subsequent step involves reducing Ceffective. This can be achieved through a combination of factors, including logic function selection, logic style, circuit topology, data statistics, and operation sequencing. Furthermore, optimization can be approached from both static and dynamic perspectives. Static optimization entails adjusting transition probabilities in relation to Boolean operations, while dynamic optimization accounts for the impact of transient "glitching" transitions that may occur before the logic settles into its static state [10]. This holistic approach not only recognizes the vital role of energy optimization but also encompasses a comprehensive understanding of the interplay between parameters and their impact on energy efficiency.

3.2. Example Sum

Assume designing a four-bit absolute-value detector circuit with a capacitive load C_l composed of logic gates and transmission lines. Let's assume the total capacitance is 50 femtofarads (fF) for the sake of this example.

Capacitive Load Optimization: By selecting smaller logic gate sizes and using low-power logic styles like pass-transistor logic (PTL), this paper can reduce the capacitance. Suppose this paper initially use standard CMOS logic gates, and their average gate capacitance is around 10 fF. By switching to PTL with an average capacitance of 6 fF, this paper reduce the overall capacitance by 4 fF.

Supply Voltage Adjustment: Let's say the original supply voltage V_{DD} is 1.2 volts. Lowering it to 1.0 volts can result in substantial energy savings. The energy consumed during charging or discharging a capacitance Cl from voltage V1 to voltage V2 is given by

$$E = \frac{1}{2}C(V_2^2 - V_1^2) \tag{9}$$

For our example, with initial V_{DD} of 1.2V and reduced V_{DD} of 1.0V, the energy reduction would be approximately. The energy reduction achieved by lowering V_{DD} is approximately

$$\begin{aligned} E_{initial} &= \frac{1}{2}\times 50\times 10^{-15}\times(1.2^2 - 0^2) \approx 3.6\times 10^{-15}\ joules \\ E_{optimized} &= \frac{1}{2}\times 50\times 10^{-15}\times(1.0^2 - 0^2) \approx 2.5\times 10^{-15}\ joules \end{aligned} \tag{10}$$

In summary, optimizing the four-bit absolute-value detector involves reducing the capacitance by switching to PTL and adjusting the supply voltage. These optimizations can collectively lead to a significant energy reduction, such as from $3.6\times 10^{-15}\ joules$ to $2.5\times 10^{-15}\ joules$ in this example.

3.3. The Overall Approach.

Optimizing energy consumption in four-bit absolute-value detectors is a multifaceted task that demands a comprehensive approach. The key considerations involve logic gate sizing, supply voltage, path length, and capacitance load reduction. By striking a balance between these factors, a holistic energy optimization strategy can be formulated [11].

To achieve energy efficiency, several strategies can be employed. One vital aspect is Logic Gate Sizing, where optimizing gate sizes involves finding the right trade-off between switch power and dynamic power. Smaller gate sizes decrease switch power but may raise dynamic power due to quicker switching, while larger gate sizes can mitigate dynamic power at the cost of increased switch power.Another key consideration is Supply Voltage Selection. Adjusting the supply voltage (Vdd) has a significant impact on energy consumption. Lowering Vdd reduces both dynamic and static power, leading to overall energy savings. However, this decision should be carefully balanced with performance requirements, as lower supply voltage might affect operational speed [12]. Furthermore, Path Length Optimization is crucial. The number of levels in a circuit's path directly influences energy consumption. Shortening critical paths accelerates switching and diminishes energy usage. Achieving the right equilibrium between path length, gate sizes, and energy consumption is paramount for optimization.Capacitance Load Reduction is equally important. Minimizing capacitance load can significantly enhance energy efficiency. Techniques such as low-power driving and signal frequency reduction contribute to lowering overall load and result in substantial energy savings.Lastly, Topology Optimization offers potential for further reduction. Exploring diverse circuit topologies and arrangements can provide insights into novel ways of reducing energy consumption. The consideration of layered or parallel structures aligned with specific application needs can yield innovative energy-efficient solutions [13].

Optimizing energy consumption in four-bit absolute-value detectors requires a synergistic approach that takes into account logic gate sizing, supply voltage, path length, and capacitance load. The interplay of these factors is intricate, necessitating a systematic analysis for efficient energy-conscious design.

4. Conclusion

In summary, in Chapter 2, our analysis of detector principles, circuit topology, and circuit styles reveals that altering the number of gate stages and subsequently adjusting logic gate sizes can effectively reduce energy consumption. Similarly, modifying the load capacitance also demonstrates

a notable reduction in energy consumption. Moving on to Chapter 3, through comparative calculations using various detector parameters, it becomes evident that the supply voltage (V_{DD}) can significantly impact energy consumption. This leads us to the conclusion that lowering the supply voltage can effectively mitigate energy consumption. The synthesis of our findings across these chapters underscores a multifaceted approach to optimizing the energy efficiency of detectors. By strategically addressing gate stages, logic gate sizes, load capacitance, and supply voltage, a holistic energy reduction strategy can be formulated. These findings not only contribute foundational insights for energy optimization in detectors but also provide a conceptual framework for shaping future optimization strategies.

Looking towards the future, the realm of detector energy optimization holds immense potential for innovation and advancement. Exploring alternative materials like Gallium Nitride (GaN) could offer a promising avenue. GaN's unique electrical properties could lead to enhanced performance, reduced leakage currents, and ultimately lower energy consumption. Additionally, Adjusting the W/L ratio and implementing techniques like adaptive voltage scaling promise efficient operations. These advancements will shape energy-efficient detectors, aligning with the growing demand for sustainable technologies. The future of detector energy optimization lies in a fusion of novel materials, advanced transistor designs, adaptive voltage scaling, and innovative circuit paradigms. These forward-thinking approaches hold the potential to pave the way for highly efficient detectors that align with the increasing demand for energy-conscious technologies.

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