Adiabatic Power Management Techniques for Metal Oxide Silicon Field Effect Transistors in Digital Logic Circuits

Qiansong Luo *

Department of Engineering, University of Auckland, Auckland, 1010, New Zealand

* Corresponding Author Email: qluo764@aucklanduni.ac.nz

Abstract. Metal Oxide Silicon Field Effect Transistors are foundational components in electronics, mainly digital logic circuits. Effective power management in MOSFET-based logic circuits becomes more crucial as technology expands to sub-100-nanometer nodes. Four optimization techniques to reduce power losses during switching transitions are carefully examined in this article. With the first method, QSSERL, no additional timing control clocks are required, which results in significant energy savings, especially in high-frequency applications. In the second method, DFAL, split-level sinusoidal power clocks are used instead of diodes, significantly lowering voltage differentials and power dissipation. Building on DFAL, IDFAL employs control transistors to reduce leakage power, significantly lowering power dissipation and facilitating charge recovery. Lastly, FSOA, inspired by natural species' collective behaviour, enhances key components within MOSFET-based circuits. This paper examines numerous adiabatic logic topics. Developing energy-efficient MOSFET-based logic circuits is essential for improving electronics and satisfying the growing demand for energy-conscious technologies.

Keywords: MOSFET; power lose; adiabatic logic; high-frequency application.

1. Introduction

Metal Oxide Silicon Field Effect Transistors (MOSFETs) are integral electronic components, enabling voltage manipulation and signal amplification across diverse applications. Comprising source, gate, and drain terminals, MOSFETs form the bedrock of digital logic circuits. As technology advances, scaling down to sub-100-nanometer nodes, effective power dissipation management in MOSFET-based logic circuits is increasingly imperative [1].

This review thoroughly investigates MOSFET-based logic circuits, motivated by the pressing imperative to minimize power losses during switching transitions. This paper meticulously examines four distinctive optimization methodologies, each characterized by its unique approach: QSSERL represents a paradigm shift in MOSFET-based logic design, obviating the necessity for additional timing control clocks. This innovation effectively surmounts the challenges associated with multiphase clocking, notably manifesting substantial energy savings, particularly in high-frequency scenarios. DFAL, like static CMOS logic, eliminates diodes from both the charging and discharging paths. It introduces split-level sinusoidal power clocks, thereby ameliorating voltage differentials between electrodes. This deliberate slowing of load capacitance charging and discharging profoundly diminishes power dissipation. IDFAL, building upon the foundation laid by DFAL, IDFAL incorporates control transistors to curtail leakage power, significantly mitigating power dissipation and facilitating charge recovery. FSOA presents an innovative optimization methodology inspired by the collective behaviour of natural species. When applied to MOSFET-based circuits, it engenders performance enhancements in critical components such as comparators and operational amplifiers. This comprehensive exploration promises to unveil insights into state-of-the-art approaches for crafting power-efficient MOSFET-based logic circuits. These methodologies are of paramount significance in advancing energy-conscious electronics within the contemporary technological landscape, where the optimization of power consumption remains a pivotal challenge.

2. CMOS Background

2.1. Function logic

The full name of MOSFET is Metal Oxide Silicon Field Effect Transistors, a type of electronic device used to switch or amplify voltages in circuits. The terminals of MOSFET are named as source, gate, drain, and body. In general, the body and source connect, thus MOSFET usually a three-terminal device. The structure of MOSFET is typically represented as in figure 1 [2].

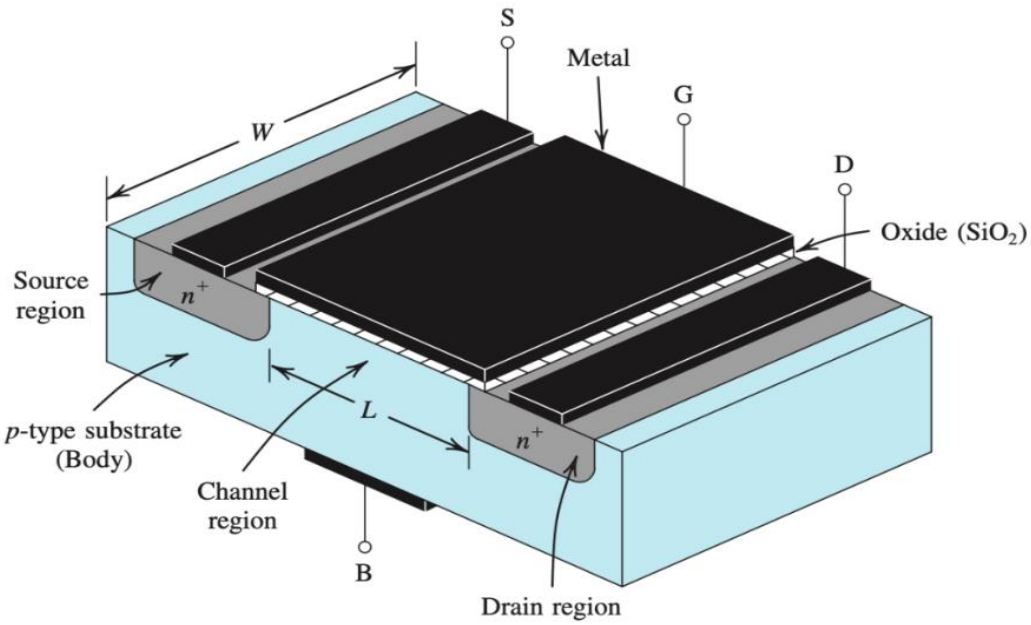


Fig 1. Structure of N-type MOSFET [2].

The Fig.1 shows an N-type MOSFET has two n+ regions at the source and drain with a p-type region in between, and there are lots of electrons in n+ regions and free space in the p-type region. There are metals that conduct electrons between the voltage supplies to those junctions, and there is also an oxide layer between the metal and p-type region [3]. At rest, no current can flow out of the MOSFET. When positive voltage applies to the gate, since the holes present beneath the oxide layer have the same polarity with the gate terminal, holes experience repulsive force and move downwards, thus creating a channel between the source and drain. When an external voltage source is applied, electrons can freely flow forward through channel. Fig.2 shows the symbol of two main types of MOSFET.

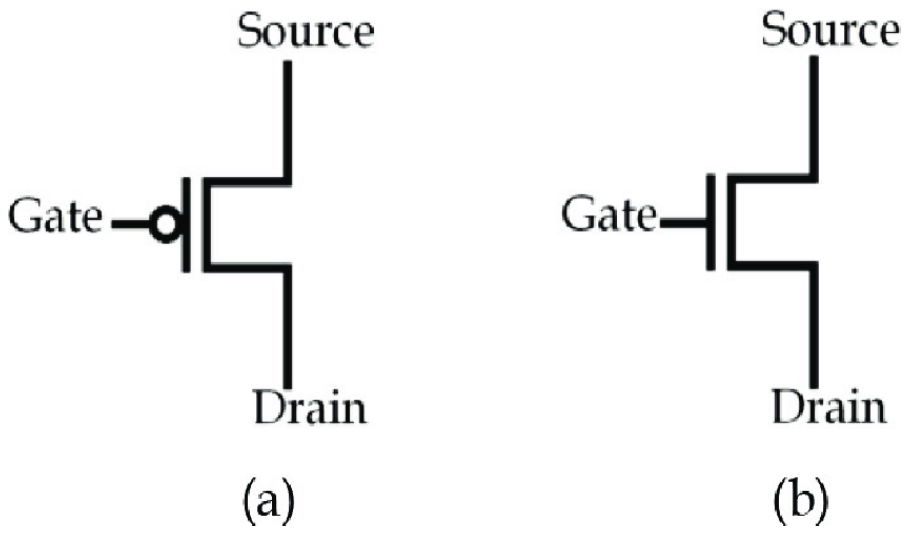


Fig 2. Symbol of (a)N-type and (b)P-type MOSFET (Photo/Picture credit: Original).

2.2. Intern structure

In logic circuit design, the most commonly used logic gate is the inverter. Fig.3 shows the static CMOS logic inverter

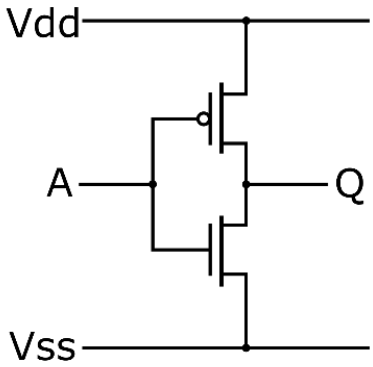


Fig 3. Structure of static CMOS logic inverter (Photo/Picture credit: Original).

The Static CMOS logic inverter is a fundamental building block in digital integrated circuits, used to invert the logic level of an input signal, producing the complementary output signal. The inverter consists of a PMOS transistor and an NMOS transistor connected in series between the power supply and ground.

When the input signal is high, the PMOS transistor turned on, creating a conductive path between the voltage supply and the output. At the same time, the NMOS is off, preventing any current flow to the ground. As a result, the output is pulled up to the supply voltage, representing a logic high.

Conversely, when the input signal is low, the PMOS turned off, cutting off the path to the voltage supply. Simultaneously, the NMOS transistor is on, creating a conductive path to the ground. This allows the output to be pulled down to the ground, representing a logic low [4].

The essential advantage of the Static CMOS logic inverter is its ability to provide both strong logic high and low outputs, ensuring a robust and reliable operation. Additionally, it offers a high noise margin, making it less susceptible to noise interference [5].

2.3. Heat dissipation

However, the operation of the Static CMOS logic inverter is not entirely efficient, leading to heat dissipation. This is primarily due to the fact that during the switching transitions, both the PMOS and NMOS transistors are momentarily conducting simultaneously. This results in a brief period where both transistors are partially on, creating a direct path between the power supply and the ground. Consequently, a significant amount of current flows through the transistors, causing power dissipation and generating heat.

When technology nodes are typically above 100 nm, dynamic power dissipation makes up the majority of the total power dissipation. However, the current electronic industry is focused on nodes with a technology scale below 100 nm. Therefore, in below 100 nm technological nodes, static or leaky power dissipation is essential to the overall power dissipation.

Dynamic dissipation occurs when the circuit change logic level, which caused by load capacitance charging and discharging [6]. When logic circuit pull up, load capacitor's voltage charing toV_{DD}. And power dissipation is:

$$E = \frac{1}{2} C_L V_{DD}^2 \tag{1}$$

Where: C_L is load capacitance of CMOS inverter, V_{DD}^2 is source voltage

Then apply a circuit clock frequency f_{clk} and activity factor α, now the power dissipation can be written as:

$$P_{dynamic_{loss}} = \alpha f_{clk} C_L V_{DD}^2 \tag{2}$$

This formula accounts for the power consumed during the charging and discharging of the load capacitance during switching transitions.

For the 100-nm process that is common in today's integrated circuits, the typical parameters are as follows:

$$C_L = 500\ \text{fF},\ V_{DD} = 1\text{V},\ \alpha = 0.25 \tag{3}$$

So one typical COMS converter, the power dissipation is

$$P_{dynamic_loss} = 0.125\ pW/Hz \tag{4}$$

3. Literatures of adiabatic logic

3.1. Quasi-Static Single-phase Energy Recovery Logic (QSSERL)

In the optimal adiabatic logic circuit, a new type of QSSERL is proposed in [7]. There does not exist an extra time control clock in this new logic. For two-phase 2N-2N2D, inserting data buffers is necessary to ensure that signals coming from various clock phases are synced, which results in additional power and space consumption. Compared to that, QSSERL can overcome the problems through its single voltage source [8]. The Schematic of QSSERL inverter is shown in figure 4.

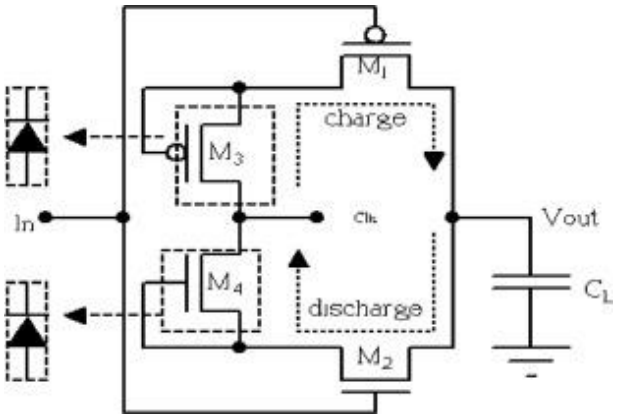


Fig 4. Schematic of QSSERL inverter (Photo/Picture credit: Original).

As can be seen, unless the input changes, the output remains in its current this could happen every clock cycle or not—depends on capacitor charging or discharging.

QSSERL only requires one charging and discharging period as opposed to the two required by the normal design. As a result, QSSERL will use less power. Due to this, QSSERL exhibits low energy dissipation when circuit at high frequencies, saves about 27% of the energy when frequency is 32 MHz compared to static inverter [8].

3.2. Enhanced Diode-free Logic (DFAL)

Another optimization for the adiabatic logic to reduce power dissipation is the Proposed Diode Free Adiabatic Logic. The circuit with no diode in either the charging or discharging path contains a pair of sinusoidal voltage supply V_{pc} and$\overline{V_{pc}}$. By making one clock in phase and the other clock inverted, the voltage difference between the electrodes is minimized since the voltage level of Vpc 1.5 times higher the voltage of$\overline{V_{pc}}$. Thus, the reduction of power dissipation resulted.

The diode for discharging is replaced by an nMOS transistor (M3), controlled by the power clock Vpc to turn on and off. Mainly, the threshold voltage drop (nonadiabatic loss) at the (MOS) diodes causes the majority of power dissipation in the discharging path. However, in suggested circuit Fig.5, the pull-up energy loss of M3 is to blame. Compared to the heat dissipation when voltage drop in diode, the previous one has much better behavier. Additionally, M3 can also recycle electricity from the output stage, allowing further more recovery of energy losses. Compared to the diode-based adiabatic circuits, the power dissipation is reduced significantly [9].

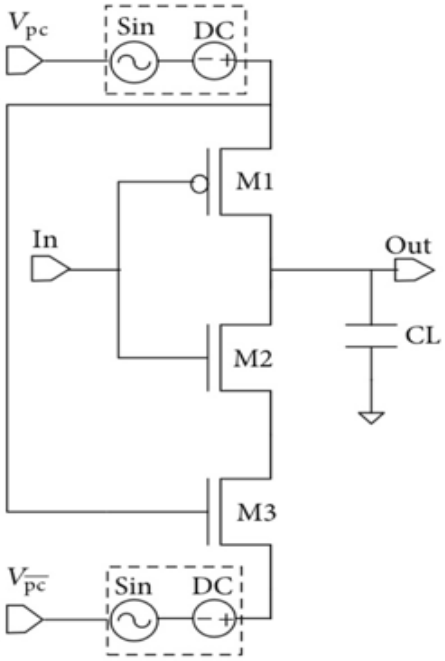


Fig 5. Schematic of DFAL inverter (Photo/Picture credit: Original).

All DFAL-based logic circuits an energy savings of over 50% at 50MHz. The bigger integral DFAL circuit, which at 50 MHz, saves over 53% more energy than CMOS multipliers. The proposed DFAL circuit is favorable in high density and high frequency VLSI applications and would be particularly effective in lowering the charging energy of analog to digital converters such as liquid crystal TV or computer displays.

3.3. Improved Diode-free Adiabatic Logic (IDFAL)

In the improvement of DFAL, the enhanced diode-free adiabatic logic proposed in this research. The logic called IDFAL creatively used a pair of sinusoidal power source which are out of phase, and in different DC level. The peak current flowing through transistors can be decreased with the help of the split-level power supply, reducing power usage. Control transistors are also included in the circuit to limit leakage power. The schematic of IDFAL inverter is shown in figure 6.

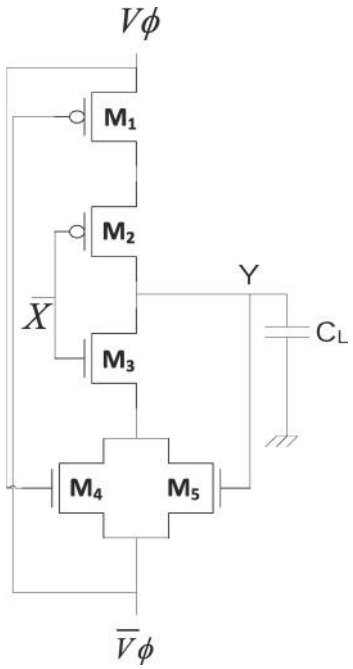


Fig 6. Schematic of IDFAL inverter (Photo/Picture credit: Original).

There is a 180° of phase difference exists between the two power clocks $\overline{V_{\emptyset}}$ and$V_{\emptyset}$. The peak-to-peak voltage of each power clock is set to half ofV_{dd}. The voltage between the current-carrying electrodes might be lowered in the circuit using these two power clocks, minimizing power usage.

IDFAL (Improved Dual Floating-Gate Adiabatic Logic) incorporates two control transistors to minimize the floating state of the output node. This design feature helps reduce leakage current and leakage power. Additionally, the use of complementary split-level power clocks further contributes to the reduction of power consumption [10]. Simulation results demonstrate that IDFAL achieves significant power savings, with an average power reduction of 95% compared to CMOS technology in the below 100nm HP_PTM process. IDFAL outperforms other logic families such as DFAL [8], CCAL, 2PASCL, 2PADCL, ADCL, and QSER in terms of power optimization and savings.

3.4. Fish Swarm Optimization Algorithm (FSOA)

This study introduces a novel optimization methodology named FSOA, which draws inspiration from the collective behaviour and swarming principles observed in natural species. The FSOA is applied to optimize the design of a two-stage comparator and a folded cascade operational trans-conductance amplifier (FCOTA) in the context of Complementary Metal Oxide Semiconductor (CMOS) circuits. The underlying concept of FSOA is to mimic the behaviour patterns of fish in their natural habitat, including activities like preying, migration, and local optimization by individual fish to achieve global search capabilities [11].

By applying individual movement operator (S_I^{t+1}), food operator (W_I^{t+1}) and non/instinctive collective movement operator ($\vec{S}_i^{t+1}$) as follows:

$$S_i^{t+1} = S_i^t + rand \times W_{ind} \tag{5}$$

$$W_i^{t+1} = W_i^t + \frac{\Delta di}{\max(\Delta d)} \tag{6}$$

$$\vec{R}^t = \frac{\sum_{i=1}^{N} \vec{\Delta S}_i \Delta d_i}{\sum_{i=1}^{N} \Delta d_i} \tag{7}$$

$$\vec{S}_i^{t+1} = \vec{S}_i^t + \vec{R}^t \tag{8}$$

The transistor-level circuit simulations were conducted using μm level technology for the CMOS two-stage comparator and folded cascode operational trans-conductance amplifier (OTA). The simulation results obtained through the application of FSOA demonstrate significant improvements in the performance of the optimized circuits. The FSOA algorithm effectively determines the optimized parameters, such as MOS transistor series-parallel connection and bias voltage, resulting in reduced MOS transistor area, lower power dissipation, and improved gain, phase margin, and unity-gain bandwidth (UGB) compared to previously reported methodologies.

4. Conclusion

In conclusion, this review has undertaken a comprehensive exploration of MOSFET-based logic circuits, addressing the critical imperative of minimizing power losses during switching transitions. We meticulously scrutinized four distinct optimization methodologies, each offering a unique approach to enhance power efficiency in MOSFET-based logic circuits. For future research directions, we recommend further exploration and refinement of these optimization methodologies, as well as their integration into practical circuit designs. Additionally, investigating their applicability in emerging technologies and exploring novel optimization algorithms could pave the way for even more efficient and sustainable electronic systems. Ultimately, the pursuit of energy-efficient MOSFET-based logic circuits remains crucial in advancing the field of electronics and meeting the growing demands for energy-conscious technologies.

References

[1] Ferain I, Colinge C A, Colinge J P. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. Nature, 2011, 479(7373): 310-316.

[2] Natori K. Ballistic metal-oxide-semiconductor field effect transistor. Journal of applied Physics, 1994, 76(8): 4879-4890.

[3] Sedra A, Smith K C, Carusone T C, et al. Microelectronic circuits 8th edition. Chapter, 2020, 14: 1235-1236.

[4] Veendrick H. Bits on chips. Springer, 2018.

[5] Sharroush S M. Analysis of the subthreshold CMOS logic inverter. Ain Shams Engineering Journal, 2018, 9(4): 1001-1017.

[6] Fanet H. Ultra-low power electronics and adiabatic solutions. John Wiley & Sons, 2016.

[7] Li S, Zhou F, Chen C, et al. Quasi-static energy recovery logic with single power-clock supply. 2007 IEEE International Symposium on Circuits and Systems. IEEE, 2007: 2124-2127.

[8] Kramer A, Denker J S, Avery S C, et al. Adiabatic computing with the 2N-2N2D logic family. Proceedings of 1994 IEEE Symposium on VLSI Circuits. IEEE, 1994: 25-26.

[9] Upadhyay S, Mishra R A, Nagaria R K, et al. DFAL: diode-free adiabatic logic circuits. International Scholarly Research Notices, 2013, 2013.

[10] Vanlalchaka R H, Maity R, Maity N P. Energy-Efficient circuits with improved diode free adiabatic logic design methodology. Ain Shams Engineering Journal, 2023, 14(8): 102049.

[11] Maji K B, Kar R, Mandal D, et al. Optimal design of low power high gain and high speed CMOS circuits using fish swarm optimization algorithm. International Journal of Machine Learning and Cybernetics, 2018, 9: 771-786.