Circuit design and energy optimization strategy for a four-bit absolute value detector

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Abstract. The demands placed on the quality of products and services within the realm of electronic technology have reached unprecedented heights. The utilization of electronic decoders has thus become incredibly extensive to meet these evolving needs. Among the integral components of electronic decoders, the absolute value detector holds a significant position. In our pursuit to enhance the efficiency of electronic decoders, this paper have identified substantial room for improvement within the currently prevalent absolute value detector designs. This paper introduces a novel absolute value detector design scheme that promises remarkable advancements. It is worth noting that the performance of this newly proposed absolute value detector far surpasses that of the traditional counterparts. Through rigorous calculations and testing, our absolute value detector exhibits an impressive performance profile, boasting a delay of $34.13FO_{4\ (1V)}$ and an energy consumption of $184.832E_{u\ (1V)}$. These results undoubtedly hold the potential to catalyze innovation in digital decoder technology, offering fresh insights into how we can elevate the overall quality of digital decoders. This contribution paves the way for product enhancements and serves as a valuable resource for those striving to stay at the forefront of electronic technology advancements in our fast-paced information-driven society.

Keywords: Digital decoder; Absolute-value detector; Comparator; Digital gate.

1. Introduction

In recent years, digital decoders have become an increasingly important tool in modern society [1]. With the rapid development of technology and the widespread use of digital data, the need for efficient and accurate methods of encoding and decoding has grown significantly [2]. As a result, digital decoders have found applications in a wide range of fields, including communication systems [3], cryptography, and data compression. And in a digital decoder, the absolute value detector is a central part [4, 5]. And the authors found that the present absolute value detector has a large room for optimization in terms of design.

Therefore, in this thesis, the authors propose a new absolute value detector design, which employs a subtractor to realize the function of a comparator that is subtracting the input from the number of comparisons, and then determining the size relationship by the first place of the result. Meanwhile, in the full adder part of the subtractor the authors believe that it can be simplified and only need a half adder and a gate circuit to realize the function. The final calculation shows that the absolute value detector designed by the author's exhibits good data performance in terms of both delay and energy. The design of the digital decoder product line provides new perspectives for upgrading and improving the products. In turn, it helps to improve the whole industry.

2. Digital decoder

2.1. Defination of digital decoder

A digital decoder is an electronic device that converts binary data, which is represented by a series of ones and zeros, into a specific set of instructions or actions [6]. It is used in various applications such as computer systems, communication systems, and control systems. The decoder takes in a binary input and outputs a specific signal or command based on the input code [7]. The most widely used of these is the ASCII decoder.

An ASCII decoder is an electronic device or software that converts binary data (ones and zeros) into text characters using the American Standard Code for Information Interchange (ASCII) standard. The ASCII standard assigns unique binary codes to each character, ranging from 0 to 127.Here's how an ASCII decoder works: When a decoder receives a stream of binary data as input. It uses a look-up table or algorithm to map each binary value to its corresponding ASCII character. The look-up table contains a list of all 128 ASCII characters, along with their corresponding binary codes. Once the binary value has been mapped to its corresponding ASCII character, the decoder retrieves the character from the look-up table or generates it dynamically based on the binary value. Finally, the decoder outputs the retrieved or generated ASCII character as text. For example, if it has the following binary sequence: 11010110 [8]. Using the ASCII chart shown in figure 1 below, it can be seen that this binary sequence corresponds to the letter "h".

Character	ASCII
a	97
b	98
c	99
d	100
e	101
f	102
g	103
h	104
i	105
j	106
k	107
l	108
m	109

Character	ASCII
n	110
o	111
p	112
q	113
r	114
s	115
t	116
u	117
v	118
w	119
x	120
y	121
z	122

Character	ASCII
A	65
B	66
C	67
D	68
E	69
F	70
G	71
H	72
I	73
J	74
K	75
L	76
M	77

Character	ASCII
N	78
O	79
P	80
Q	81
R	82
S	83
T	84
U	85
V	86
W	87
X	88
Y	89
Z	90

Character	ASCII
0	48
1	49
2	50
3	51
4	52
5	53
6	54
7	55
8	56
9	57

Fig 1. ASCII chart [9].

There are also many different types of digital decoders, including linear feedback shift register (LFSR) - a type of digital decoder that uses a linear sequence of bits to generate a pseudo random number. Maximum length sequence (MLS) decoder - a type of digital decoder that generates a maximum length sequence of ones and zeros. In summary, a digital decoder is an essential component in many modern technologies, and it plays a vital role in converting binary data into meaningful information.

2.2. Work flow of digital decoder

A digital decoder works by processing a binary input signal and generating a specific output signal based on the input code. The workflow of a digital decoder is divided into the following steps as shown in figure 2.

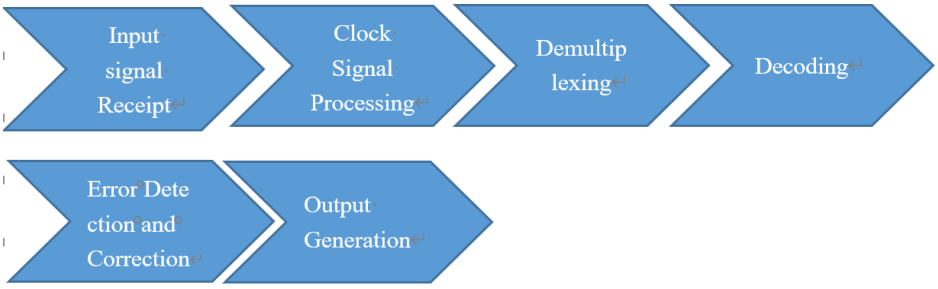


Fig 2. Workflow of a digital decoder.

Input Signal Receipt: The digital decoder receives the binary input signal that needs to be decoded. This signal can come from a variety of sources, such as a communication channel, a storage device, or another digital system [10]. Clock Signal Processing: The clock signal is processed to synchronize the decoding process with the input signal. This ensures that the decoder accurately captures the binary data and minimizes errors. Demultiplexing: In some cases, multiple signals may need to be decoded simultaneously. Therefore, demultiplexing is done to separate the input signal into individual channels for parallel decoding. Decoding: The actual decoding process involves applying logic operations to the input signal using combinational logic circuits or sequential logic circuits. These operations depend on the coding scheme used and the desired output. For example, if the input signal

is encoded using a Hamming code, the decoder would use a Hamming distance calculator to determine the error and correct it. Error Detection and Correction: After decoding, error detection and correction techniques like cyclic redundancy check (CRC), parity bit checking, etc., are applied to detect and fix errors that might have occurred during transmission or storage. Output Generation: Finally, the decoded output is generated based on the corrected input signal [11]. Depending on the application, this output could be a digital signal, analog signal, text message, and image, audio.

3. Absolute-value detector

3.1. Definition of absolute-value detector

The absolute value detector (AVD) is a powerful technique used in various fields such as signal processing, image analysis, and machine learning. Its primary function is to detect and extract features from signals or images that have both positive and negative values. The AVD serves multiple purposes, including anomaly detection, feature extraction, and noise reduction. It can be implemented using hardware, software, or a combination of both. Depending on the application, the choice of AVD type will vary, and each has its own set of advantages and limitations. For instance, hardware-based AVDs offer fast processing speeds but may be limited in terms of flexibility, whereas software-based AVDs provide greater customization options but may be slower. When selecting an AVD, it's essential to consider factors such as the type of data, desired output, and computational resources. Overall, the AVD is a valuable tool for identifying patterns, trends, and anomalies in data, making it an indispensable component in many modern technologies.

3.2. Initial design

In terms of circuit design, the author encountered the problem of how to use MOS tubes to represent absolute value 0/1 shunt processing. The author’s initial solution was to represent a positive number when the highest bit is 0, set the negative output to 0, and then combine the number output from the positive output with the negative output to realize an output similar to a tri-state gate. Similarly when the highest bit is 1, it indicates a negative number. This enables absolute value 0/1 shunt processing. Based on this line of thinking, the authors completed the initial circuit design through a simple and brutal way shown in figure 3.

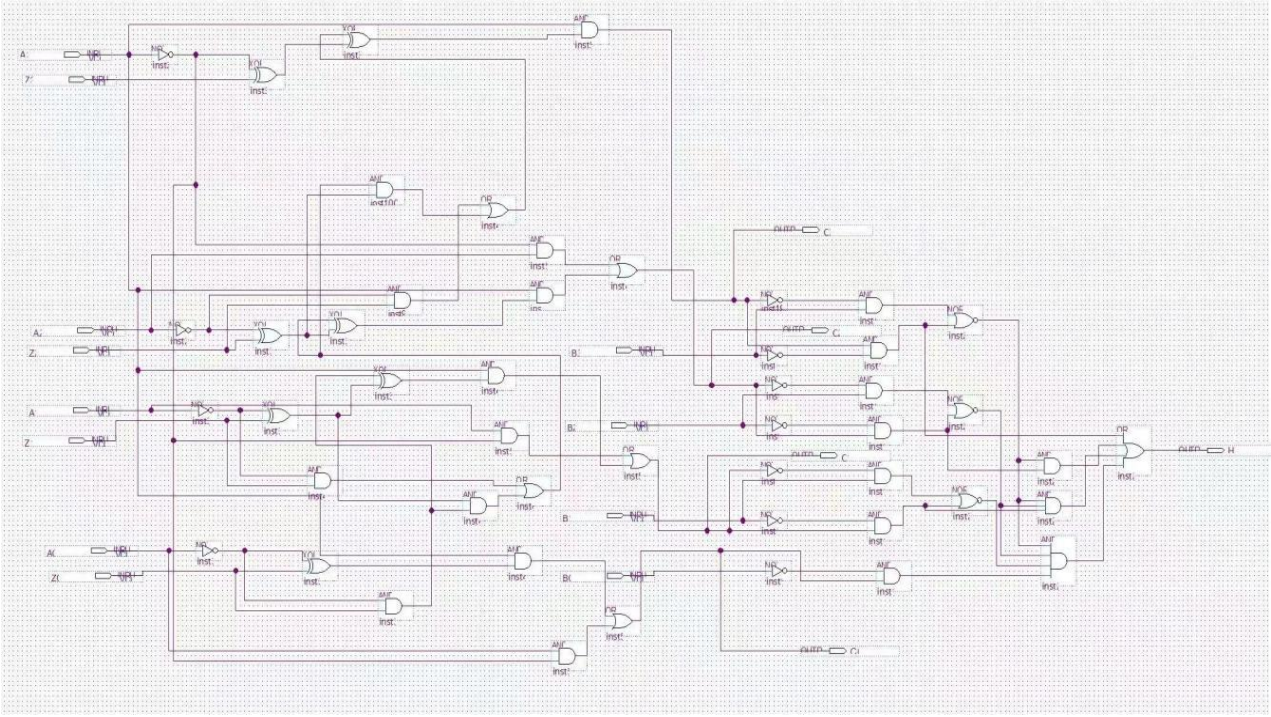


Fig 3. Initial design.

3.3. Advanced design

After this, we thought of a more optimized scheme. In the second scheme, we implement the comparator by means of a subtractor, which subtracts the input X from the comparator number Y. The working principle is shown in figure 4.

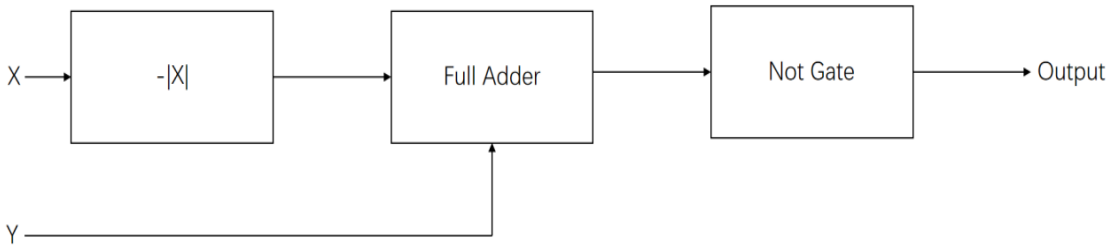


Fig 4. Working principle.

The first bit of the result is four bits. In the case of a three-bit number subtraction, the first bit of the result is four bits. When the first bit of the result is 1, it means that X is greater than or equal to Y. When the first bit of the result is 0, it means that X is less than Y. To achieve the requirement that to output 1 when X is greater than Y, and 0 when X is less than or equal to Y, it is possible to do the opposite, by allowing Y to be subtracted from X, and determining the size relationship based on the first bit of the result. In addition, the full adder portion of the subtractor can be simplified, requiring only a half adder and a gate circuit. Also, it should be noted that when taking absolute values, negative numbers need to be converted to negative absolute values. Through the truth table can be determined, when the first one is 1, the next three digits remain unchanged; when the first one is 0, you need to invert the next three digits and add 1, which is the process of taking the complement. Both methods were simulated and successfully achieved the goal while the second option has lower delay. Based on this line of thinking, the authors completed an improved circuit diagram.

In the first section, the author use XNOR gate to negate binary code of positive numbers while binary code of negative numbers is directly being output. Then there is an incomplete adder since one addition is the standard while other addition come from the carry of the previous digit. The addition of the lowest bit is the inverse of highest bit. The role of signal bit A [4] is to judge positive and negative that is over. The adder part is shown in figure 5.

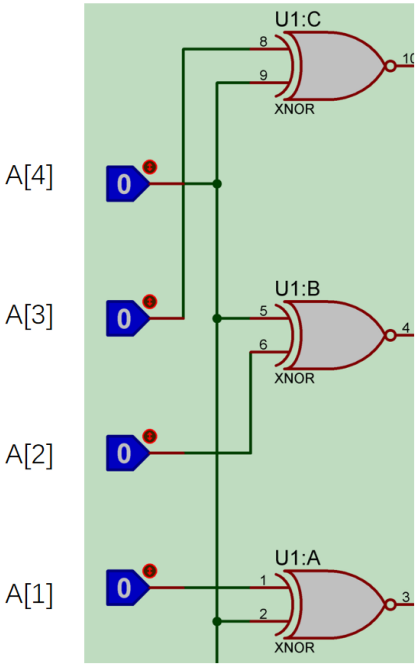


Fig 5. Adder part.

And the first place after that will not be present positive or negative. The advantage of this module is that all positive and negative input will be output through this module, eliminating the need to shunt the signal. And the comparator part is a full adder that only output carry combining the two modules gives us this circuit diagram which is shown in figure 6.

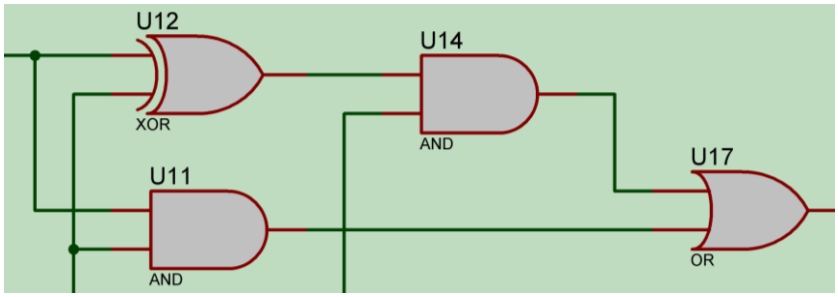


Fig 6. Comparator part.

With the top 4 inputs are input value. The first one is signal, and the bottom 3 are threshold which is positive by default. The advantage of this whole design is it tremendously save the number of logic gates and is optimized according to the function. Improved circuit is shown in figure 7.

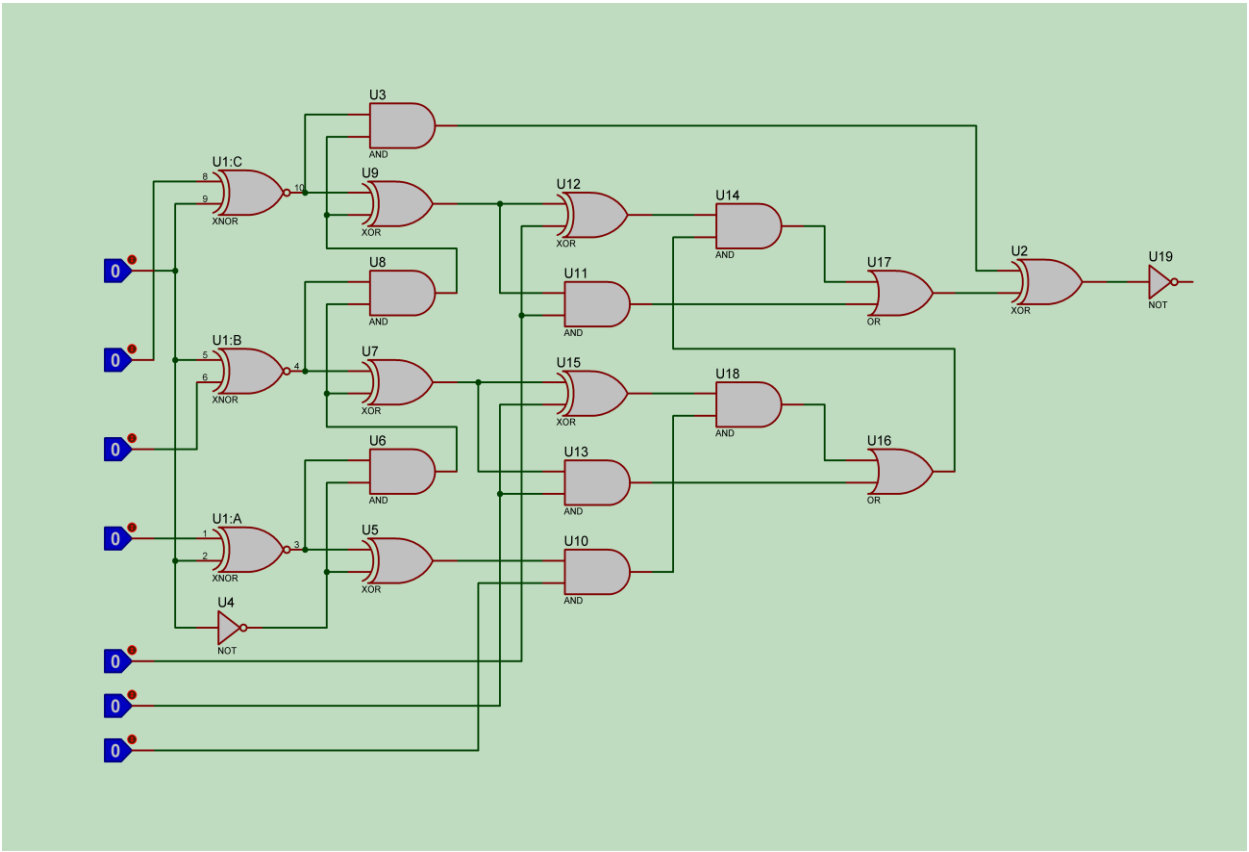


Fig 7. Improved circuit.

3.4. Critical path analysis

To calculate the delay of this circuit, the authors identified the critical path of it, i.e., the one that covers the most electronic components. The critical path is consisting of 2 inverters, 3 AND gate, 1 OR gate and 4XOR gate, it has 4 branches which is shown in figure 8.

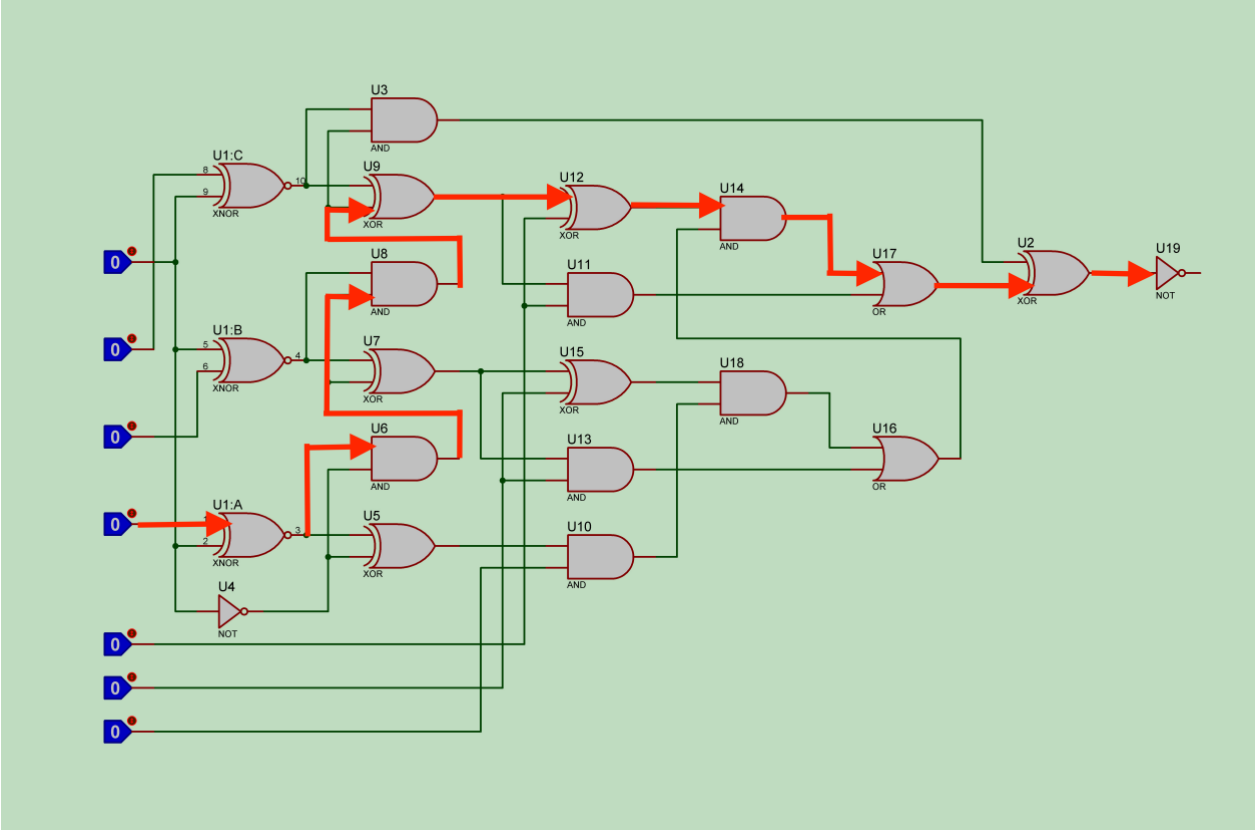


Fig 8. Critical path.

To calculate the logical effort and parasitic effort of critical path, the author divides the whole circuit into several components and calculate each one individually. After finding reference inverter of each logic gate, the author uses the formula to derive specific value.

$$\text{Logical effort (g)} \quad g = \frac{R_{gate} \cdot C_{in,gate}}{R_{INV} \cdot C_{in,INV}} \tag{1}$$

$$\text{Parasitic effort (p)} \quad p = \frac{C_{par,gate}}{C_{apr,INV}} \tag{2}$$

The logical effort and parasitic effort of different gate is shown in figure 9.

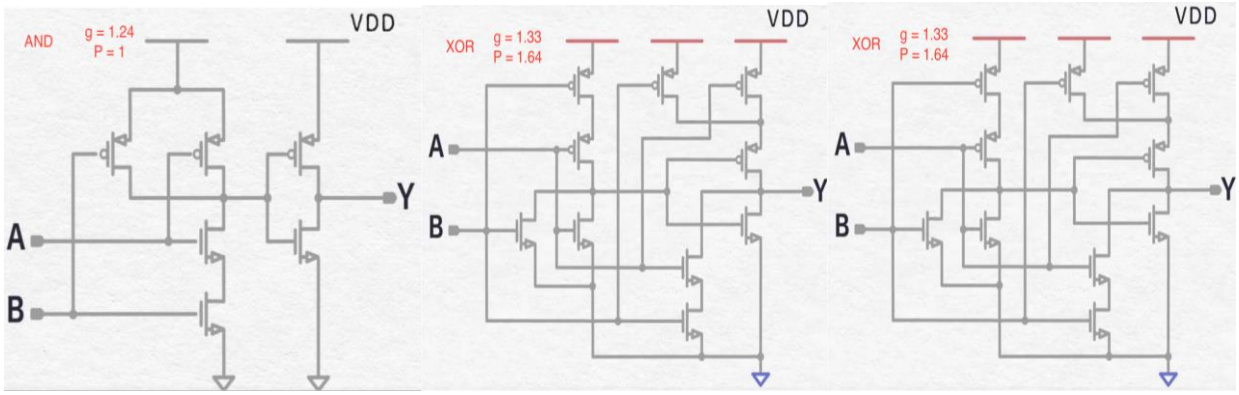


Fig 8. The logical effort and parasitic effort.

After that, the author calculated the parameters of the entire critical path. G is derived by multiplying the logical effort of ten logical gates

$$G=1.33\times1\times1.24\times1.24\times1.33\times1.33\times1.24\times1.43\times1.33\times1=8.5 \tag{3}$$

Cl = 32 and the input buffer equals to 2, so the electrical fan-out H can be calculated by the formula.

$$\text{Electrical fan-out (h)}\ h = \frac{C_{out}}{C_{in,gate}} \tag{4}$$

$$H=32/2=16 \tag{5}$$

There are 4 branches and each branch is two. So the author simply times them up and got B. B=16. According to the formula, the author also finds path effort F

$$F=G*H*B \tag{6}$$

$$F=8.5*16*16=2183.68 \tag{7}$$

Rounding this value up to the tenth power, the author got the value of path effort of optimum stage of every gates, f = 2.157. After that, the author derived the minimum delay of the circuit by using 10 times minimum delay of each stage adding the parasitic delay D. Dmin= 34.13. Finally, the author derived the V_{dd} through the formula

$$T= k \times \frac{V_{dd}}{(V_{dd} - V_T)^2} \tag{8}$$

$$V_{DD}=0.76 \tag{9}$$

The result given by excel is shown in figure 9.

Critical path (gama=1)											
H=32/2=16	Stage	1	2	3	4	5	6	7	8	9	10
	Cin	2	1	1	1	1	1	1	1	1	1
	g	1.33	1	1.24	1.24	1.33	1.33	1.24	1.43	1.33	1
	b	1	1	2	2	2	2	1	1	1	1
	p	1.64	1	1	1	1.64	1.64	1	1	1.64	1
	K=21.169										
	F:path effort:2183.68										
	f:2.157										
	VDD:0.76										
	mini delay:34.13										
	τopt(1.5*mini delay):34.13=51.20										

Fig 9. Critical path analysis.

3.5. Energy-delay model

In the energy section, this paper first calculates the delay corresponding to the maximum energy can achieve by equation.

$$E = CL * Vdd\text{^}2 \tag{10}$$

It end up with a maximum power consumption of 320. That is the first point. After sizing the circuit, it take the delay value of 34.1 derived from Logic effort and bring it into equation to get the corresponding V_{dd} value, and then it bring this value into equation to get the energy value of 306, and it can see that this is the second point, which corresponds to the state that has decreased in the energy value and increased in the delay value.

$$t= k \times \frac{V_{dd}}{(V_{dd} - V_T)^2} \tag{11}$$

Based on this, this paper multiplies the delay value after sizing by 1.5 to get the delay value of the optimized circuit and bring it into to calculate the minimum required energy value of 184.8.

After the whole process, we find that lower delays are always accompanied by higher power consumption. Moreover, the optimized circuit saves a huge amount of power compared to the circuit with Vdd equal to 1, and the optimized circuit is more significant in reducing energy consumption compared to sizing circuit up to 135. The result is shown in figure 10.

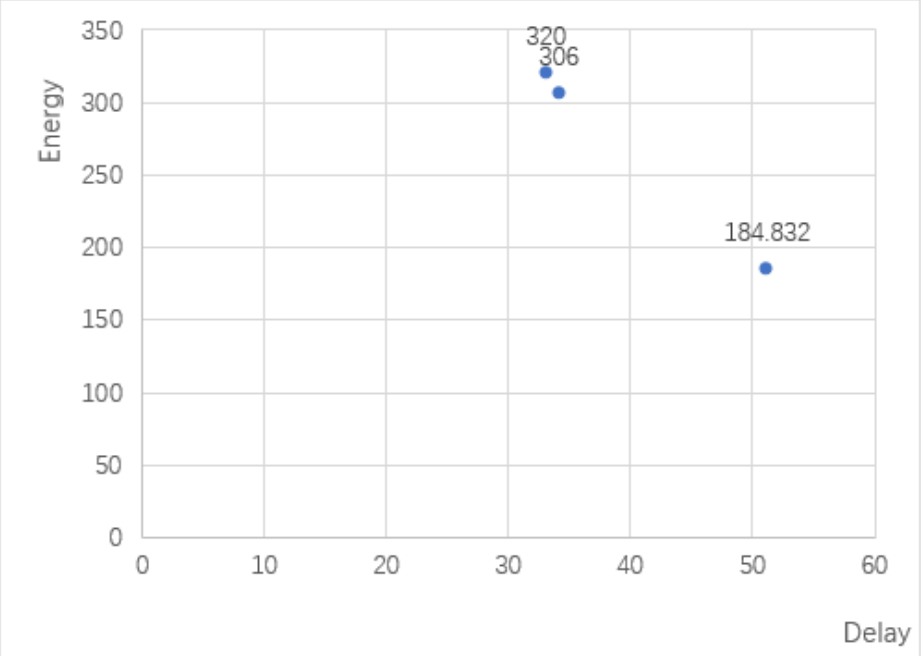


Fig 10. Relationship between Energy and delay.

4. Conclusion

In conclusion, through a comprehensive process of design and optimization, we have successfully developed an absolute value detector that excels in terms of both energy efficiency and latency. This achievement holds great promise for revitalizing the landscape of digital decoders, offering not only enhanced performance but also innovative avenues for exploration. Nonetheless, it believe that there remains ample room for further refinement in absolute value detector design. This includes the potential for optimizing the detector's fundamental characteristics by adjusting parameters such as the W/L ratio. Additionally, exploring alternative materials, such as gallium nitride, presents an enticing opportunity. Gallium nitride's broader band gap and lower on-resistance, in contrast to conventional semiconductor silicon, hold the potential to significantly elevate the absolute value detector's performance. As it look to the future, these avenues of optimization and innovation continue to beckon, propelling digital decoder technology to new horizons of excellence.

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