Enhancing Surface Electromyography (sEMG) Signal Processing through a Four-bit Absolute Value Comparator

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Abstract. This paper delves into the realm of Surface Electromyography (sEMG) signal processing, presenting a comprehensive exploration of its theoretical underpinnings and the application of a four-bit absolute value comparator. The journey commences with an introduction to the subject matter, followed by an in-depth analysis of the theoretical basis of sEMG signals, encompassing their definition and waveform characteristics, as well as the processing flow. The focal point of this study is the utilization of a four-bit absolute value comparator in enhancing sEMG signal processing. Moving forward, the paper delves into the intricacies of logic circuit design, elucidating the architecture of both adder and comparator circuits pivotal in this context. Circuit optimization strategies are subsequently unveiled, addressing critical path considerations, gate sizing, and VDD optimization to bolster efficiency. In summation, this research advances our understanding of sEMG signal processing and introduces a novel four-bit absolute value comparator, which holds promise in elevating the precision and reliability of sEMG data analysis.

Keywords: Surface Electromyography; sEMG Signal Processing; four-bit Absolute Value Comparator; Logic Circuit Design.

1. Introduction

Surface electromyography signal (sEMG) constitutes a crucial component of the arsenal for monitoring the intricate dynamics of the neuromuscular system. This signal, characterized as a one-dimensional time series, is meticulously captured through electrodes placed on the muscle surface. The fluctuations within sEMG are intricately tied to several key factors: the extent of motor unit involvement in the muscular activity, the nuanced patterns of motor unit activation, and the prevailing metabolic state. As a real-time indicator, sEMG proficiently mirrors the current state of muscle activity and functional capacity without inflicting any harm [1].

The invaluable utility of sEMG transcends various domains of scientific inquiry and practical application. In the realm of clinical medicine, it emerges as a potent diagnostic tool for unveiling the mysteries of neuromuscular diseases. In the field of ergonomics, it enables a granular analysis of muscular engagement during tasks, particularly within the meat industry. Rehabilitation medicine benefits from sEMG as it aids in the meticulous evaluation of muscle function, assisting healthcare professionals in tailoring interventions effectively [2]. Sports science turns to sEMG to gauge the onset of fatigue, helping athletes optimize their training regimens. Moreover, sEMG's analytical prowess extends to the domain of sports technology, where it lends insight into the rationality of equipment and techniques employed. Lastly, sEMG offers predictive capabilities regarding muscle fiber type, further enhancing our understanding of human physiology [3].

In the intricate process of sEMG signal processing, two critical steps demand attention: noise elimination and eigenvalue determination. This paper introduces a meticulously designed four-bit absolute value comparator to address these challenges, underscoring its significance in refining the precision and reliability of sEMG data analysis.

2. Theoretical basis of s EMG signal

The generation of EMG is the external response to the central system instructions. In the process of body movement, EMG is often accompanied by skeletal muscle generation, and the comprehensive

characterization of the signal reflects the current state of nerve and muscle movement. In the general research process, there are two main ways to collect the electromyography signal. One is to obtain the electromyography signal by inserting the needle electrode into the muscle, which has the advantage of small interference and easy identification, but it will cause invasive damage to the human body. The other method is to obtain the electromyogram signal on the surface of the human skin through electrodes or other sensors, namely surface electromyogram signal (sEMG). This method is relatively easy to collect signals, friendly to the human body, and is more commonly used. Therefore, the sEMG signal collected from the surface of skin is mainly studied in this paper.

2.1. Definition and waveform characteristics of s EMG signal

Surface electromyography is one of the three major physiological electrical signals in human body (EMG, EEG, ECG), which comes from the potential changes of the central nervous system when responding to external stimuli. Under the innervation of nerves, the polarization reaction on the surface of the cell membrane leads to the variation of the membrane potential, and then the superposition and propagation of the potential on the muscle fiber, thus generating detectable physiological electrical signals on the surface of the skin [4]. As an external comprehensive representation of the potential activity of human muscle cells, it can reflect the characteristics of the current physiological state and consciousness state of the human body, such as muscle fiber strength, muscle state, human psychological activity, and brain movement intention and so on.

Electromyography (EMG), as we know, is a relatively weak electrical signal, meanwhile, skin and tissue have attenuation effect on EMG, so the sEMG signal recorded on the skin surface is weaker than that recorded by the needle electrode and is more susceptible to interference. A lot of studies and experiments show that the amplitude of surface EMG signal is random and can represent the quasi-Gaussian distribution function, the amplitude is microvolt level, the peak-to-peak value is between 0~6mV, and the variance is between 0~1.5mV. The effective energy of the signal is in the frequency range of 0-500Hz. The original surface electromyogram is shown in Figure 1 [5].

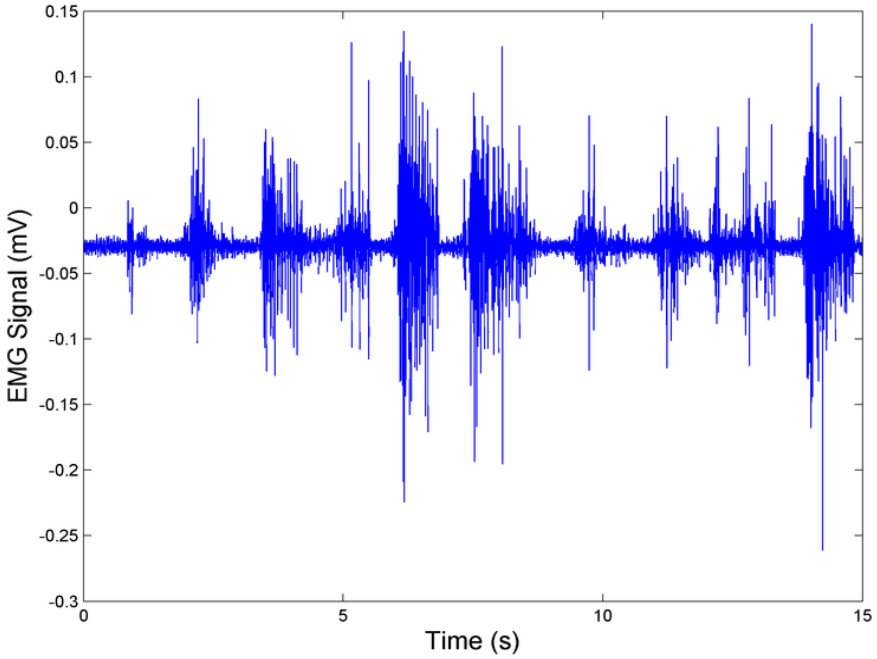


Figure 1. Unprocessed s EMG signal diagram [5]

2.2. sEMG signal processing flow

The sEMG signal processing process mainly includes two steps: noise elimination and feature extraction. Among them, the sEMG signal noise elimination is to eliminate the weak sEMG signal

affected by human factors such as skin, body hair and experimental environment factors. The common denoising methods are usually applied in time domain, frequency domain and time frequency domain. The wavelet transform method is widely used in denoising, which has the characteristics of low computational complexity and easy implementation. In order to have a higher signal-to-noise ratio, the adaptive threshold is usually used to denoise the sEMG signal [6]. In addition, by decomposing the maximum value of the wavelet mode and reconstructing the wavelet coefficient, the method can obtain better noise elimination effect.

After the sEMG signal is denoised, the characteristic values of sEMG signal need to be extracted to obtain the information which can be used for muscle activity and functional state research. The feature extraction of sEMG signal can calculate the mean value, root mean square, zero crossing number and other eigenvalues of signal in time domain after signal filtering and other preprocessing. S EMG signals can also be converted into frequency domain signals through Fourier analysis, so as to analyze the frequency and energy characteristics of sEMG signals, and extract the median frequency, average frequency and peak frequency of s EMG signals. This method is usually relatively stable. In addition, there are also improved optimization schemes based on time domain or frequency domain feature analysis, such as feature extraction, time scale method, recursive quantization analysis method and Choi-Williams distribution, which comprehensively use time domain and frequency domain analysis methods [7].

2.3. Application of four-bit absolute value comparator in s EMG signal processing

Through the above introduction of s EMG signal processing flow, we can find that the four-bit absolute value comparator has a wide application in the process of sEMG signal filtering and denoising, the absolute value comparator can remove noise or false signals below the set threshold, thereby improving the quality of sEMG signal [8].

In addition, after the feature value extraction of sEMG signal is completed, it is often necessary to associate each feature value with specific muscle activity and functional state. The absolute value comparator can compare the feature value of sEMG signal with the threshold value corresponding to specific muscle conditions, so as to identify specific muscle characteristics and states.

3. Logic circuit design

In order to meet the above functions of the absolute value comparator applied to sEMG signals, the four-bit absolute value comparator designed in this paper will take two input signals, one is the characteristic value x [n] of the sEMG signal, and the other is the given threshold value Thr of the corresponding feature. The resulting logic circuit will first obtain the amplitude (absolute value |x|) of the binary signal x [n], and then compare it with the given threshold (Thr). If the characteristic value of the sEMG signal is greater than the given threshold, the output will be "1" (high logical value); Otherwise, the final output is "0" (low logical value). The schematic diagram of its logic function is shown in Figure 2.

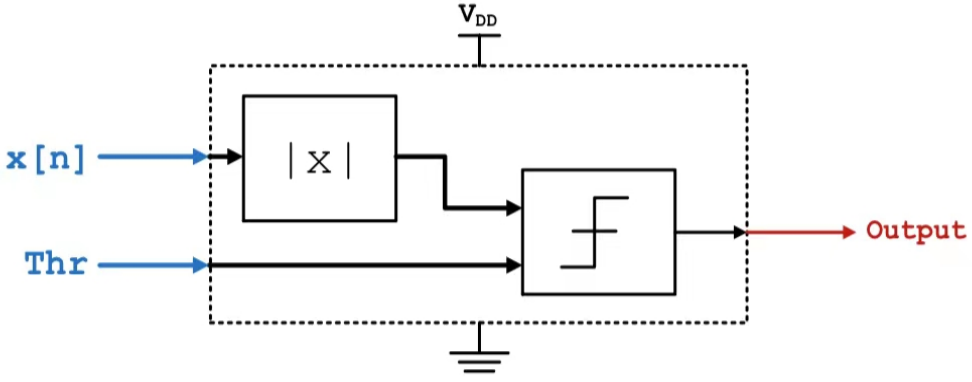


Figure 2. The schematic diagram of its logic function (Photo/Picture credit: Original).

In order to realize such logic function, the four-bit absolute value comparator designed in this paper will be composed of two logic circuits: an adder and a comparator.

3.1. Adder circuit

In this part of the circuit, the input of the circuit is the four-bit binary characteristic value of the sEMG signal A3, A2, A1, A0, A3 here is the sign bit, and the numerical bits A2, A1, and A0 are arranged from high to low. The sign bit A3 here represents the positive and negative of the input binary eigenvalue signal. When it is 0, it means the input signal is a positive signal, and when it is 1, it is a negative signal.

The output of the circuit should be B2, B1, B0, and the output does not contain sign bits, representing the absolute value of the input signal x [n], that is, the amplitude of the signal. Through the elaboration of the functions of this part of the logic circuit. Analyzing and can find that when A3=0, B2=A2; B1=A1; B0=A0; and when A3=1, B2=A2 ⊕ (A0+A1); B1=A1 ⊕ A0; B0=A0 [9].

Considering the cases of A3=1 and A3=0, this paper designed the logic circuit schematic diagram and logic gate circuit diagram, as shown in Figure 3.

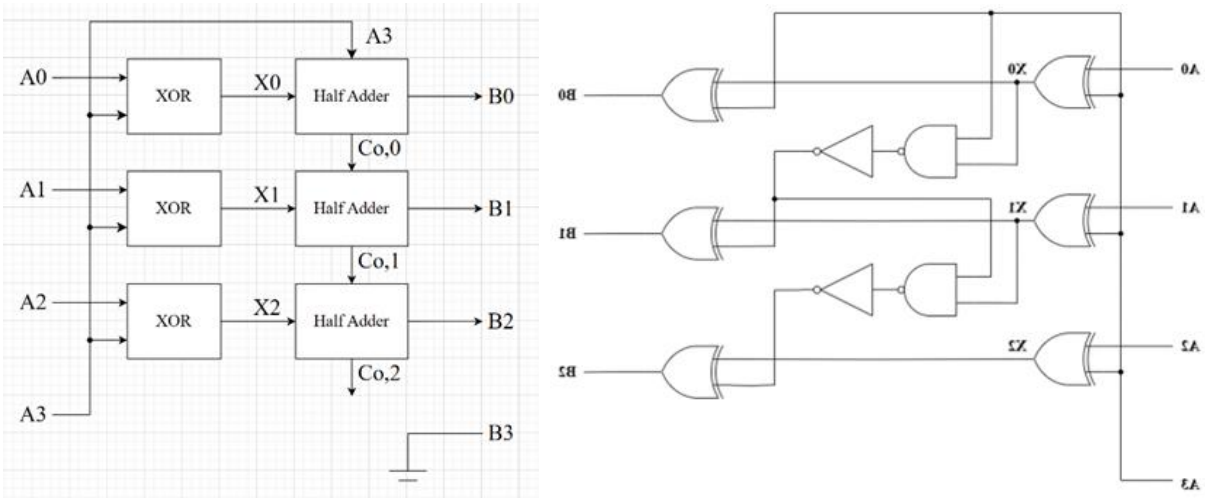


Figure 3. Logic circuit schematic diagram and logic gate circuit diagram (Photo/Picture credit: Original).

3.2. Comparator circuit

In this part of the circuit structure, we will undergo the sEMG signal characteristic value of amplitude and the comparison between the given threshold, namely comparing B2, B1, B0 ($|x|$) with C2, C1, C0 (Thr). If $|x|$ > Thr, Output=1, Otherwise, Output=0. For convenience, let's define

$$Y_i = B_i C_i + \overline{B_i}\,\overline{C_i} = \overline{B_i \overline{C_i} + \overline{B_i} C_i} \tag{1}$$

Therefore

$$\begin{aligned} Output &= B_2\overline{C_2} + Y_2 B_1 \overline{C_1} + Y_2 Y_1 B_0 \overline{C_0} \\ &= \overline{\overline{B_2} + C_2} + \overline{\overline{Y_2 B_1} + C_1} + \overline{\overline{Y_2 Y_1} + B_0 \overline{C_0}} \end{aligned} \tag{2}$$

By designing the circuit with this logic expression, the circuit diagram of the comparator circuit can be obtained step by step, as shown in Figure 4.

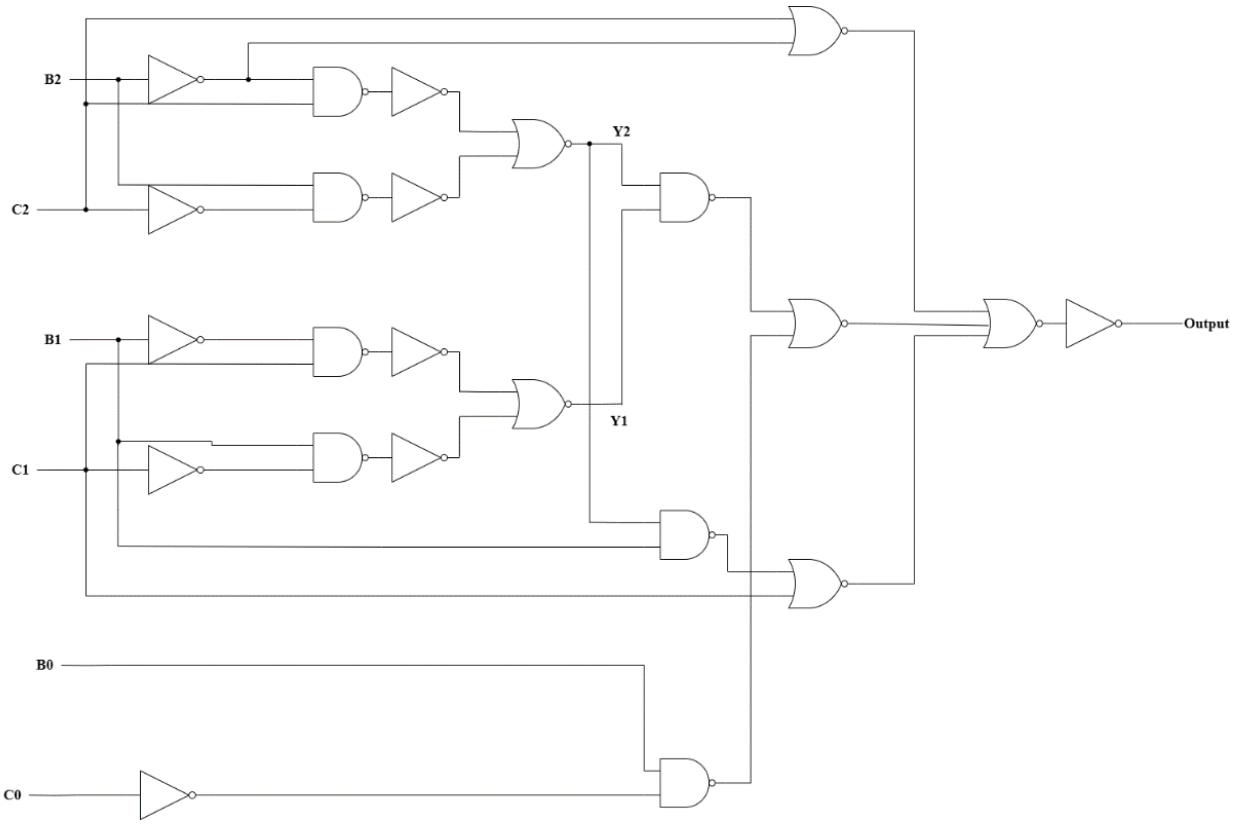


Figure 4. Circuit diagram of the comparator circuit (Photo/Picture credit: Original).

Through the above analysis of the two parts of the designed circuit, we only need to combine the circuit of the adder and the comparator part, we can realize the logical function of comparing the s EMG signal amplitude with the given threshold.

4. Circuit Optimization

After completing the required circuit logic function, we still need to optimize the size of CMOS in each logic gate of the circuit according to the structure to optimize the delay and energy consumption of the circuit. In order to make the designed circuit have a smaller delay and better power consumption, in this circuit optimization stage, we design and adjust the size of CMOS of all stages in the circuit, and comprehensively consider the influence of the power supply voltage, so as to improve the performance of delay and energy consumption.

4.1. Critical path

To facilitate the optimization of circuit delay and energy consumption, this paper has to introduce the concept of the critical path. The critical path here refers to the longest path in a synchronous logic circuit, significantly affecting the overall logic delay and design performance. It is often identified as the path with the most stages or branches, and if two branches have the same number of stages, the one with the most branches is considered the crucial route.

Through statistical analysis, the critical path of the circuit designed in this article has 14 stages and 5 branches. The gate level topology diagram of the critical path is shown in the following Figure 5.

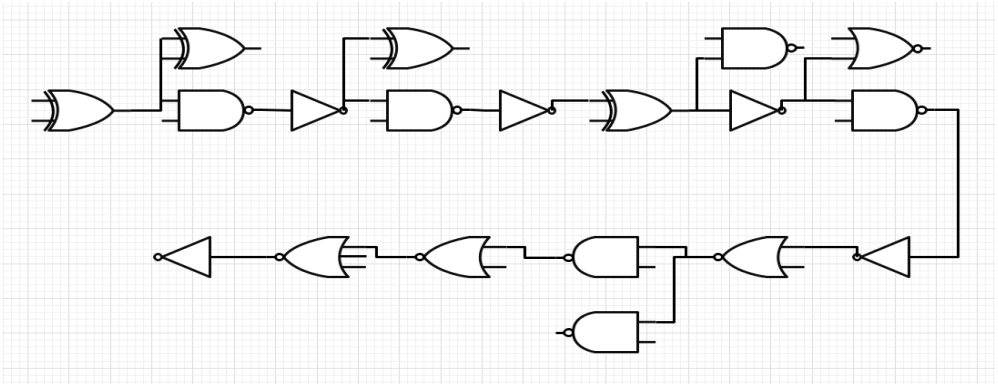


Figure 5. The gate level topology diagram of the critical path (Photo/Picture credit: Original).

As a path that significantly affects the minimum delay in the circuit structure, gate sizing and energy optimization that we need to carry out later require us to reasonably analyze and calculate the minimum delay of this critical path when VDD=1V.

The circuit designed in this paper all use CMOS complementary logic, and to facilitate the calculation of delay, the following assumptions are proposed in advance: (1) Unit-sized inverter is Wp= 650nm, Wn= 430nm, Lp= Ln= 100nm. (2) The input capacitance for all inputs is limited to two unit-sized inverters or below. To power the inputs, a unit-sized buffer (comprising two unit-sized inverters) is used for design purposes. The delay is calculated based on the time it takes for the signal to travel from the input driver to the load which includes 32 unit-sized inverters). (3) The output bit has CL= 32 unit-sized inverters placed into it [10].

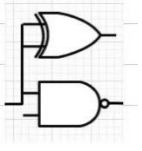
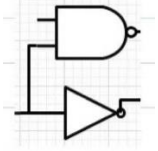
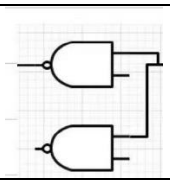
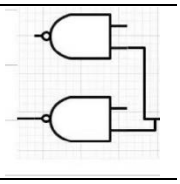
Based on the above assumptions, the logic efforts and parasitic delays of each basic logic gate that appears in this circuit can be calculated as shown in the table 1 below.

Table 1. Logic efforts and parasitic delays of each basic logic gate.

Gate Type	Number of Inputs					
	1		2		3	
	g	p	g	p	g	p
Inverter	1	1				
NAND			1.4	2		
NOR			1.6	2	2.2	3
XOR			4	4		

In addition, the branch effort of the four different branches in the critical path can also be calculated by the CMOS logic gate structure, the values of which are shown in the following table 2.

Table 2. Types and values branch effort.

Branch Type				
Branch Effort	3.86	2.4	2.6	3

As it can be known

$$Delay = \sum_{i=1}^{N} \left(p_i + g_i \bullet h_i \right) \tag{3}$$

And in this critical path, when each stage bears the same effort, which means all stages are sized by f and they bear the same fanout, each stage has the same delay, and the delay would be minimum.

$$D_{\min} = \sum \left(g_i \bullet h_i + p_i \right) = N \bullet f + P \tag{4}$$

$$f = \sqrt[N]{PathEffort} \tag{5}$$

$$F = GHB \tag{6}$$

$$H = \frac{C_{out}}{C_{in}} \tag{7}$$

$$P = \sum_{i=1}^{N} p_i \tag{8}$$

Therefore

$$H_{path} = 32, B_{path} = 185.95, G_{path} = 346.17, f = 2.82, D_{\min} = 67.84 \tag{9}$$

4.2. Gate sizing

Based on the above calculation of the minimized delay in the critical path, we can see that in order to minimize the circuit delay, we should ensure that the f of each stage is equal and 2.82. Then it can complete gate sizing based on this formula.

$$C_{in} = g \times \frac{C_{out}}{f} \tag{10}$$

So for the minimum delay, the size of each stage on the critical path can be calculated as following table 3.

Table 3. Size of each stage on the critical path.

Cin1	Cin2	Cin3	Cin4	Cin5
1	0.183	0.369	0.270	0.544
Cin6	Cin7	Cin8	Cin9	Cin10
1.534	0.451	0.489	0.985	2.778
Cin11	Cin12	Cin13	Cin14	
2.448	4.931	8.691	11.141	

4.3. VDD Optimization

After determining the size of each stage, we must also comprehend how the supply voltage affects the delay. This paper adjusts the delay to 1.5 times the minimal delay of the critical path in order to optimize the VDD within the range of 0 to 1 volts. Assume VT= 0.2V. The formula for VDD optimization is as follows [11].

$$D = \frac{K \bullet V_{DD}}{\left(V_{DD} - V_T \right)^2} \tag{11}$$

$$D_{opt} = \frac{K \bullet V_{DD-opt}}{\left(V_{DD-opt} - V_T \right)^2} \tag{12}$$

With the application of these formula, the VDD voltage is reduced to 0.7751V, which minimizes the total delay and energy consumption. This result has important reference value for optimizing circuit design and improving energy efficiency.

5. Conclusion

In this study, it has delved into the intricate realm of Surface Electromyography (sEMG) signal processing, with a particular focus on the application of a four-bit absolute value comparator. Our investigation commenced by establishing the theoretical foundations of sEMG signals, providing insight into their definition, waveform characteristics, and processing flow. Subsequently, we introduced the logic circuit design, including adder and comparator circuits, which are instrumental in implementing the four-bit absolute value comparator.

Through rigorous analysis, we identified key opportunities for circuit optimization, addressing critical path concerns, gate sizing, and VDD optimization. These optimizations promise to enhance the efficiency and accuracy of sEMG signal processing, paving the way for more robust applications in fields such as clinical medicine, ergonomics, rehabilitation medicine, sports science, and sports technology.

Looking ahead, the potential for further advancements in sEMG signal processing remains promising. Future research could explore more sophisticated circuit designs, advanced noise reduction techniques, and the integration of machine learning algorithms to unlock new dimensions of insight from sEMG data. Additionally, the real-time and non-invasive nature of sEMG signal analysis positions it as a valuable tool for the emerging fields of human-computer interaction and assistive technology. As technology continues to evolve, the synergy between sEMG signal processing and these domains could revolutionize the way we interface with and support individuals with neuromuscular conditions. Overall, this study underscores the ever-expanding horizons of sEMG signal processing, offering exciting prospects for innovation and application in diverse scientific and practical domains.

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