Design and Optimization of a CMOS-based 4-bit Absolute Value Detector

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Abstract. This research paper introduces a meticulously crafted blueprint for a 4-bit Absolute Value Detector (AVD) utilizing cutting-edge Complementary Metal-Oxide-Semiconductor (CMOS) technology. The proposed architectural marvel has been specifically fine-tuned to cater to the demands of high-speed, energy-efficient applications, making it applicable across a wide spectrum of signal-processing domains. At its core, this design harnesses the synergistic power of multiplexers, a ripple carry adder, and a comparator, strategically orchestrated to swiftly and accurately determine the absolute magnitude of the input signal, subsequently comparing it against a predefined threshold. The resultant circuit stands as a testament to its prowess, boasting a remarkably low latency while maintaining commendably low power consumption and a robust resistance to external noise interference. In doing so, it not only aligns itself with the contemporary requirements of rapid real-time signal processing but also paves the way for scalability, positioning itself as a viable solution for more intricate and demanding applications. By doing so, this innovation not only contributes to the ongoing evolution of electronic technologies but also sets the stage for future research endeavors, promising a brighter and more sophisticated future for the field.

Keywords: AVD; CMOS; Signal Processing; Threshold Comparison.

1. Introduction

With the fast-paced progress of electronic technologies, the demand for rapid real-time signal processing soars correspondingly as it plays a pivotal role in multiple electronic-related fields of engineering. Among signal processing, one of the most fundamental operations is detecting the absolute value of signals [1, 2]. In the field of neural signal acquisition systems, which has gained interest in the research community with recent advancements, absolute value detection is known for being one of the most commonly used spike sorting algorithms [3].

This paper introduces a novel 4-bit Absolute Value Detector (AVD) design, using CMOS technology. CMOS technology is known for its low power consumption and high noise immunity, making it mainstream in contemporary integrated chip design. The proposed design finds the absolute value (magnitude) of the input and compares it with a given threshold value. The circuit design aims to optimize both speed and power efficiency. Its topology comprises a series of 2-to-1 multiplexers, a ripple carry adder implemented with half adders, and a comparator. This design can be readily scaled up for more complex applications, thereby laying the foundation for further research.

2. Circuit Structure Design

2.1. Theoretical Basis

In the designing process, the circuit was divided into two functional blocks: the detector and the comparator. The former is responsible for computing the magnitude of the 4-bit binary number input. The latter is engineered to compare the output with a previously defined threshold value and give the final result. This segregation allows for modular design, thus facilitating any future modifications or upgrades [4].

In this design, the output of the former subsystem is decided to be a 3-bit number, ignoring the MSB for the reason that it will always be “0” after the process. Moreover, only a 3-bit number will

be needed for the comparator in the latter part of the circuit. The final design includes one AND gate, three inverters, three 2-to-1 multiplexers (MUX), and three half-adder, altogether composing the former block of detector and feeding the comparator a 3-bit magnitude number. The comparator block compares the received value against the threshold and gives a binary output: "1" if the magnitude is greater than the threshold, and "0" otherwise. Fig. 1 shows the structure of AVD functional blocks.

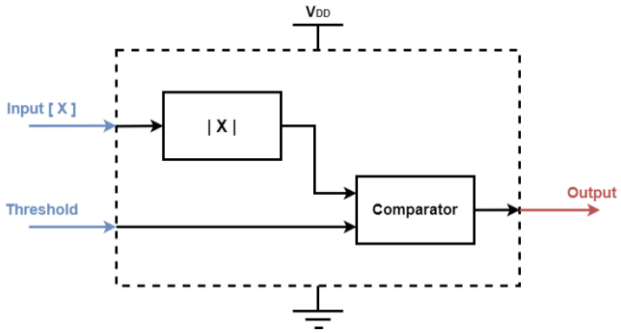


Fig. 1 Structure of AVD functional blocks (Photo/Picture credit: Original).

2.2. Absolute value detector

2.2.1. Booleans of MUX and Adders

In this case, a 2-to-1 multiplexer requires 2 AND gates, an OR gate, and a NOT gate [5]. The two inputs are designated as A and B, along with the selector input S and output Z. Boolean equation expressed as:

$$Z = A \cdot S + B \cdot \bar{S} \tag{1}$$

The composition of the chosen multiplexer is shown in Fig. 2.

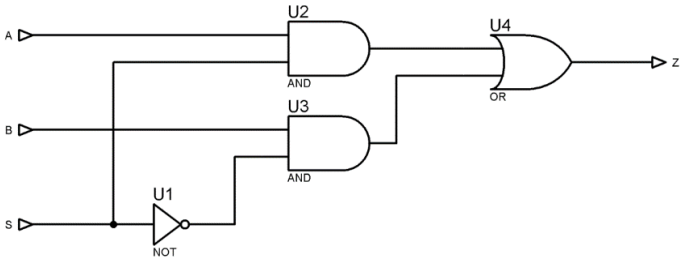


Fig. 2 Composition of a 2-to1 Multiplexer (Photo/Picture credit: Original).

A half-adder adds two digits A and B, resulting in the output consisting of a sum Z and a Carry C [6]. The Boolean equations for the outputs are expressed as:

$$S = A \oplus B \tag{2}$$

$$C = A \cdot B \tag{3}$$

The composition of the half-adder is shown in Fig. 3.

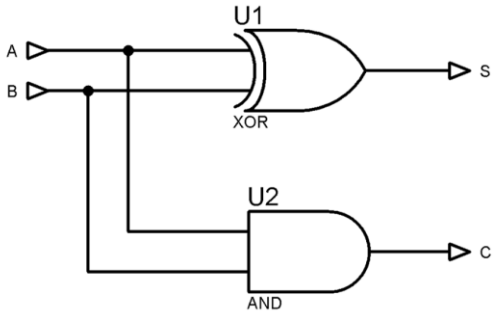


Fig. 3 Composition of a half-adder (Photo/Picture credit: Original).

2.2.2. Topology and Functionality

The circuit's topology is demonstrated below. This project envisaged the AVD's input value to be a 4-bit number, hereby denoted as *A3A2A1A0*. Among them, *A3* serves as the MSB that determines whether the input value is positive or negative. In this case, it acts as the selector input to every multiplexer.

The AND gate aims to eliminate the sign: with one input fixed at the logic state "0", the output will always be "0", regardless of A3's value. As for the MUXs, given a multiplexer MUX(n), the input *A* corresponds to *An*, while *B* corresponds to *An*'s complement. According to equation (1), we can tell that

Meanwhile, with *A3* as the selector, these digits are conditionally inverted based on the sign indicated by *A3*. This ensures that the output will correctly represent the magnitude of the input. The half-adders (HA) are connected in a ripple-carry fashion, where each takes the output from the corresponding MUX as well as the carry-out from the preceding adder. The specific configuration is demonstrated in the following figure. According to the Boolean equations (2) and (3), the outputs *B0* to *B2* are considered to be the absolute value of the input. Full topology of the detector is shown as Fig. 4.

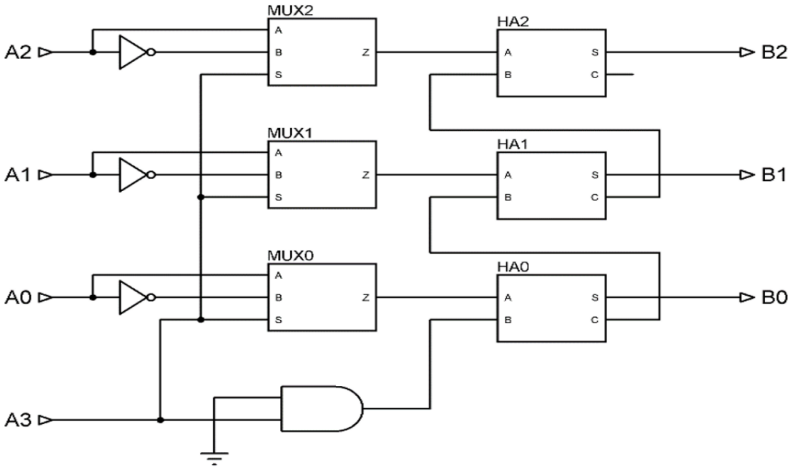


Fig. 4 Topology of the detector (Photo/Picture credit: Original).

2.3. Comparator Design Approach

The objective of this design is to compare two 3-digit binary numbers. The comparison starts from both values' most significant bit. When the output is "1", i.e., B > Th, there will be three conditions and they are considered separately: b2 > t2, b2 = t2, b1 > t1, b2 = t2, b1 = t1 and b0 > t0.
Based on these conditions listed above, the following Boolean equation is derived.

$$Z = b_2\overline{t_2} + \overline{(b_2 \oplus t_2)}(b_1\overline{t_1}) + \overline{(b_2 \oplus t_2)}\,\overline{(b_1 \oplus t_1)}(b_0\overline{t_0}) \tag{4}$$

With equation (4), the corresponding circuit topology as Fig.5 demonstrates can be obtained.

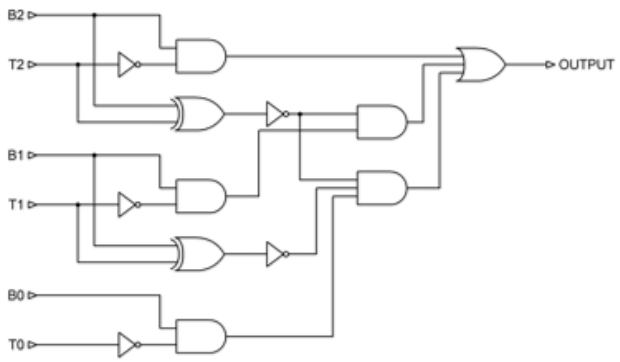


Fig. 5 Topology of the comparator (Photo/Picture credit: Original).

Upon completing the design process, the two functional blocks can now be connected and the ultimate full circuit topology is shown in Fig. 6.

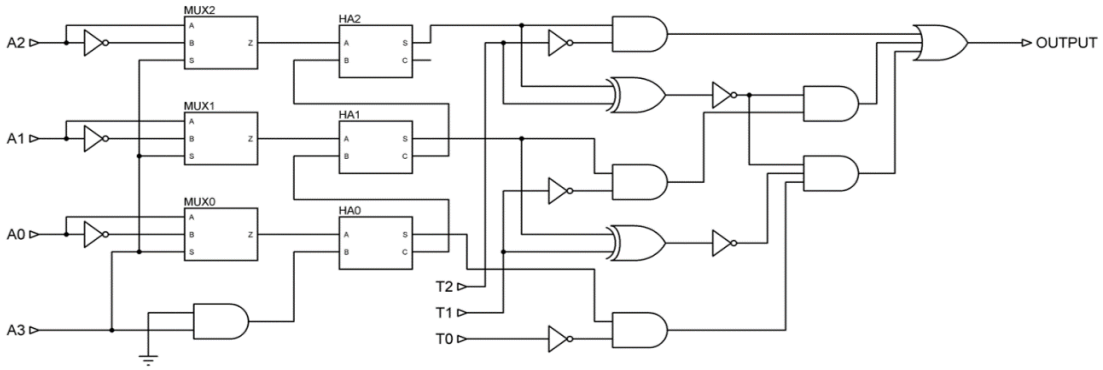


Fig. 6 Full circuit topology (Photo/Picture credit: Original).

3. Circuit Optimization

In this project, the objective is to achieve the lowest possible energy consumption while allowing for a worst-case delay that is 50% longer (1.5x) than the minimum delay in the worst case, along with an optimal VDD within the range of 0~1V.

3.1. Critical Path Analysis

When designing a circuit, the critical path is a pivotal concept that defines the longest delay path from its input to output. The performance of the critical path impacts the speed and efficiency of the entire system directly. Therefore, in order to enhance the circuit performance, optimizing the critical path is a key step [7, 8]. The critical path of the circuit designed in this paper is extracted and shown in Fig. 7 below.

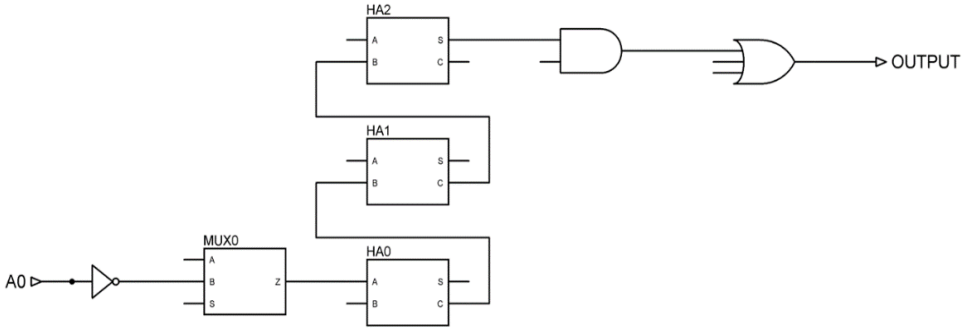


Fig. 7 Critical path in the circuit (Photo/Picture credit: Original).

The total delay can be calculated as equation (5). Note that according to Fig. 2 and Fig. 3, among the gates that constitute the MUX and HA, only those which the critical path passes by are taken into account, namely having an equivalent of 2 AND gates and 1 OR gate [9]. The total delay is considered as (5).

$$t_{\text{Critical}} = t_{Inverter} + 5t_{AND} + t_{OR} + t_{OR(\text{3-input})} \tag{5}$$

3.2. Logical Effort and Parasitic Delay Calculation

The logical effort (g) can be calculated with the equations below, where C stands for input capacitance:

$$g = \frac{C_{\text{gate}}}{C_{\text{inverter}}} \tag{6}$$

For the purpose of delay modeling, it is assumed that the ratio of parasitic capacitance to gate capacitance (C*parasitic* / C*gate*), is equal to 1, and the load capacitance of the output bit is 32 unit-sized inverters. The dimensions for a unit-sized inverter are assumed as:

$$W_p = 650\text{nm}, \quad W_n = 430\text{nm}, \quad L_p = L_n = 100\text{nm} \tag{7}$$

Where *Wp*, *Wn* denote the width of PMOS and NMOS. *Lp*, *Ln* denote the drawn L.

Since the design uses CMOS transistors, we substitute the AND and OR gates with common CMOS gates. The AND, OR, and 3-input OR gates are considered as equivalents of several NAND and NOR gates. The specific structure is demonstrated as the Boolean equations below.

$$\begin{aligned} A \cdot B &= \overline{\overline{A \cdot B}} \\ A + B &= \overline{\overline{A + B}} \\ A + B + C &= \overline{\overline{A + B + C}} \end{aligned} \tag{8}$$

The logical efforts of them are given in Table 1.

Table 1. Logical effort of common CMOS gates [9].

Gate Type	Number of inputs		
	1	2	3
Inverter	1	N/A	N/A
NAND	N/A	4/3	5/3
NOR	N/A	5/3	7/3

With the given information we can calculate the delay of each gate this design used. The logical efforts of the gates are shown in Table 2.

Table 2. Logical effort for gates used

Gate Type	**g**	**p**
Inverter	1	1
AND	2.67	6
OR	2.67	6
3-input OR	3.78	10

It can be known that:

$$H = \frac{C_{\text{out}}}{C_{\text{in}}} = 32, \; G = \prod_{i=1}^{n} g_i \tag{9}$$

As:

$$F = GBH \tag{10}$$

$$f^* = \sqrt[N]{F} \tag{11}$$

From which the stage effort is calculated: $f^* = 2.70$

Total path delay can be calculated with (11):

$$D = N \cdot f^* + \sum_{i=1}^{N} p_i \tag{12}$$

From which: D=68.60 [10].

3.3. VDD Scaling

Besides the optimization methods described above, we still have the supply voltage (VDD) left to be determined. The value of supply voltage can be obtained from the following equation [11].

$$\text{Delay} = K \cdot \frac{V_{DD}}{(V_{DD} - V_{Th})^2} \tag{13}$$

Where K is the proportionality constant, VTh refers to the threshold voltage. Given that VTh = 0.2, VDD = 1, suppose *Delay* = 1 at this condition. Substitute the known values into the equation and solve $K = 0.64$.

$$\text{Delay} = \frac{0.64 \cdot V_{DD}}{(V_{DD} - V_{Th})^2} \tag{14}$$

Plug in Delay = 1.48, solved that VDD = 0.78.

4. Conclusion

This project stands as a noteworthy milestone in the realm of 4-bit Absolute Value Detector (AVD) design, marking significant progress in this specialized field. Through an exhaustive process of rigorous analysis and comprehensive simulations, our research has culminated in the development of a circuit design that excels in both speed of response and power efficiency. This paper has navigated the challenges posed by gate limitations with ingenuity, devising solutions that ingeniously conform to the constraint of using a maximum of 4-input gates, all while maintaining stellar performance standards. The optimization techniques employed in this endeavor have not only proven their effectiveness but have also had the transformative effect of simplifying the overall topology of the circuit. This transformation renders our design accessible and adaptable for deployment across a multitude of real-world applications and industries, making it a versatile and valuable innovation.

Looking ahead to future work, this paper sets its sights on the exploration of diverse application domains where our optimized circuits can find practical implementation, including but not limited to signal processing and communication systems. It envisions a future where these circuits enhance the performance and efficiency of a wide range of technologies. Moreover, the pursuit of alternative logic functions is another avenue that holds promise for further optimization. By delving into novel logic functions, it aims to unlock even more avenues for enhancing circuit performance, thus pushing the boundaries of what is achievable in the realm of AVD design. In doing so, we anticipate contributing to the ongoing advancement of electronic technologies and paving the way for groundbreaking research in the field.

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