An Optimized Design Of 8-Bit Absolute Value Detector Based on CMOS And Logic Effort Theory

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Abstract. Absolute value detecting is widely involved in integrated digital circuits. Currently absolute value comparison happens frequently in digital integrated circuits such as RISC structure micro controllers. Considering the requirements of corresponding products, an 8-bit absolute value detector is designed and optimized in this essay. Compared with some similar magnitude comparators existing on the market, this scheme supports 2's complement input to realize calculation and comparison of absolute values. The basic structure of the design is a Complementary Metal Oxide Semiconductor (CMOS) logic gate circuit which is redesigned in order to reduce the number of transistors involved. The circuit was then further optimized in size and source voltage based on logic effort theory. Based on that, the size of logic gates and V_DD are properly adjusted to optimize both speed and energy efficiency. The final version realized a 20.12% energy consumption when the delay is 1.5 times of minimum value. In the future, similar method could be applied for optimization of other digital circuits in order to improve the performance of corresponding produces.

Keywords: Absolute value detector; CMOS; Logic effort theory; optimization.

1. Introduction

Absolute value comparison is an important calculation in digital integrated circuits including micro controllers (MCU) and field-programmable gate array (FPGA) [1]. Nowadays, binary calculations happen frequently in forms of codes from instructions sets. Take reduced instruction set computer (RISC) as example, typical length of instructions varies among 16, 32, 64 and 128, based on different functions of instructions [2]. According to the characteristics of potential calculation tasks, absolute value detectors accepting 8 or more bits inputs are required. There is a vast array of magnitude comparator chips on the market, including 54LS85, SN54HC682 and SN54AS866 from Taxes Instruments and similar integrated circuits chips. Typically, these chips are logic gate based and capable to realize 22-24ns delay [3, 4]. 54LS85 is a 4-bit magnitude comparator supporting 4-bit binary or binary-coded decimal (BCD) code and cascading inputs, which means several chips can be connected to compare 8-bit, 12-bit or longer input [2]. However, 54LS85 does not support 2's complement, or negative input. SN54HC682 is a quite similar one with 54LS85, supporting 8-bit input but binary and BCD code only [3]. Chips supporting 2's complement are not easy to find, not to mention ones capable to calculate absolute values and make comparison.

Therefore, an 8-bit absolute value detector supporting 2's complement comparison was designed and optimized in this essay. Different from previous works, the design in this essay realizes good performances in both energy efficiency and calculation speed by redesign logic gate circuit and logic effort theory. The work could provide a new scheme for 8-bit absolute value detection with smaller size and faster speed, and therefore, the ability of MCU and similar devices requiring absolute value comparison could be improved furthermore. First, the circuit designs including top structure, relative gates circuit and gate design will be introduced. Next, how the design is optimized based on logic effort theory will be described. Finally, there would be result analysis and conclusion.

2. Circuit Design

2.1. Top Structure

The top structure of the scheme can be described as an absolute value calculator and a comparator. The inputs are considered as 2's complements, which means the highest bits of the inputs are considered as symbol bits, representing whether the input numbers are positive or negative. Once a 2's complement code is inputted to the absolute value calculator, its absolute value would be outputted and transmitted to the comparator. If 2 bits of the 2 numbers on one level differ from each other and all former bits are the same, there could be a conclusion that one number is larger than the other. Or if all bits are the same, it means the 2 numbers equal.

2.2. Logic Gate Circuit

2.2.1 Absolute Value Calculator

Jingzhan Ge from Tiangong University and his team came up with a design using mirror adders and multiplexers to realize absolute value calculation with simpler structure compared using full adders [5]. Its logic is very easy to understand and thus the circuit is easy to maintain. However, the critical path is relatively long, resulting in longer delay. In this essay, the circuit is directly based on truth table as Table 1 and combine the 2 steps of finding 2's complement together.

Table 1. Truth Table of Absolute value Calculator

A [7:4]	A [3:0]	A' [7:4]	A' [3:0]	A [7:4]	A [3:0]	A' [7:4]	A' [3:0]
0xxx	NCNC	0xxx	NCNC	1xxx	1100	1xxx	0100
1xxx	0001	1xxx	1111	1xxx	1101	1xxx	0011
1xxx	0010	1xxx	1110	1xxx	1110	1xxx	0010
1xxx	0011	1xxx	1101	1xxx	1111	1xxx	0001
1xxx	0100	1xxx	1100	1000	0000	1000	0000
1xxx	0101	1xxx	1011	1001	0000	0111	0000
1xxx	0110	1xxx	1010	1010	0000	0110	0000
1xxx	0111	1xxx	1001	1011	0000	0101	0000
1xxx	1000	1xxx	1000	1100	0000	0100	0000
1xxx	1001	1xxx	0111	1101	0000	0011	0000
1xxx	1010	1xxx	0110	1110	0000	0010	0000
1xxx	1011	1xxx	0101	1111	0000	0001	0000

The design stratagem is focused on in which cases the output equals to the input. Therefore, the relationship between the input and output is as Equation 1.

$$A_i' = A_i \oplus \left(A_7 \sum_{n=0}^{i} A_n\right) \tag{1}$$

where A_i' is the i^{th} output, A_i is the i^{th} input and $1 \leq i \leq 6$. In addition, there is.

$$[A_7' \quad A_0'] = [0 \quad A_0] \tag{2}$$

Based on Table 1 and Equations 1 and 2, absolute value calculator as Fig. 1 was designed.

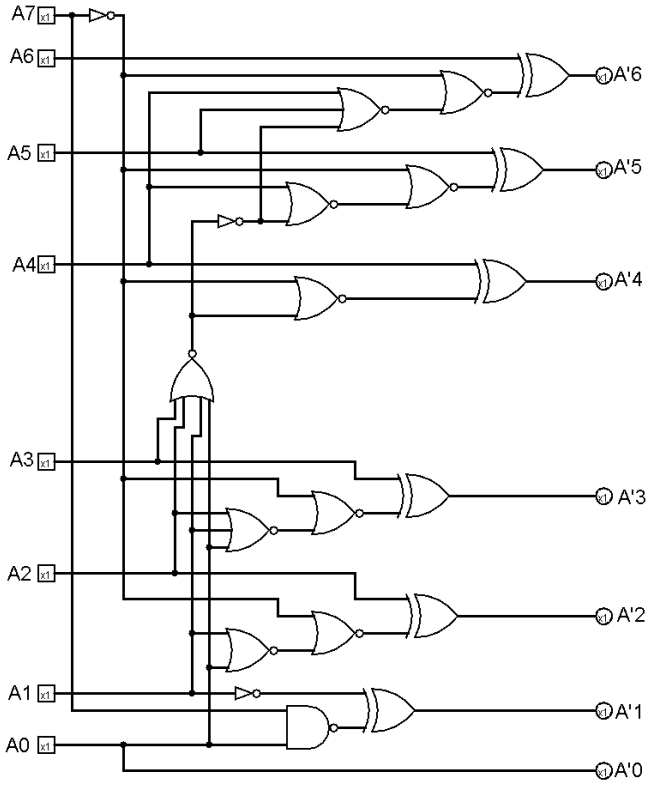


Fig. 1 Logic gate circuit of absolute value comparator for 1 input (Photo/Picture credit: Original)

2.2.2 Comparator

According to the output from absolute value calculator, only 7 bits need comparing. The truth table of comparator is as Table 2.

Table 2. Truth Table of Comparator

$A_6'B_6'$	$A_5'B_5'$	$A_4'B_4'$	$A_3'B_3'$	$A_2'B_2'$	$A_1'B_1'$	$A_0'B_0'$	Output
10	NC	NC	NC	NC	NC	NC	>
01	NC	NC	NC	NC	NC	NC	<
00/11	10	NC	NC	NC	NC	NC	>
00/11	01	NC	NC	NC	NC	NC	<
00/11	00/11	10	NC	NC	NC	NC	>
00/11	00/11	01	NC	NC	NC	NC	<
00/11	00/11	00/11	10	NC	NC	NC	>
00/11	00/11	00/11	01	NC	NC	NC	<
00/11	00/11	00/11	00/11	10	NC	NC	>
00/11	00/11	00/11	00/11	01	NC	NC	<
00/11	00/11	00/11	00/11	00/11	10	NC	>
00/11	00/11	00/11	00/11	00/11	01	NC	<
00/11	00/11	00/11	00/11	00/11	00/11	NC	>
00/11	00/11	00/11	00/11	00/11	00/11	NC	<
00/11	00/11	00/11	00/11	00/11	00/11	00/11	=

The design of the comparator is based on Table 2, where $<$, $>$ and $=$ mean $|A| > |B|$, $|A| < |B|$ and $|A| = |B|$ respectively and NC means Not Care. According to the truth table, there are relationships as Equations 3 to 5.

$$L = A_7\overline{B_7} + \sum_{i=0}^{6}\left(\overline{\sum_{n=i+1}^{7} A_n \oplus B_n}\right) \tag{3}$$

$$S = \overline{A_7}B_7 + \sum_{i=0}^{6}\left(\overline{\sum_{n=i+1}^{7} A_n \oplus B_n}\right) \quad (4)$$

$$E = \overline{\sum_{n=0}^{7} A_n \oplus B_n} \quad (5)$$

Where L, S and E refer to A is larger than, smaller than and equal to B respectively. Based on Equations 3 to 5, design as Fig. 2 was completed.

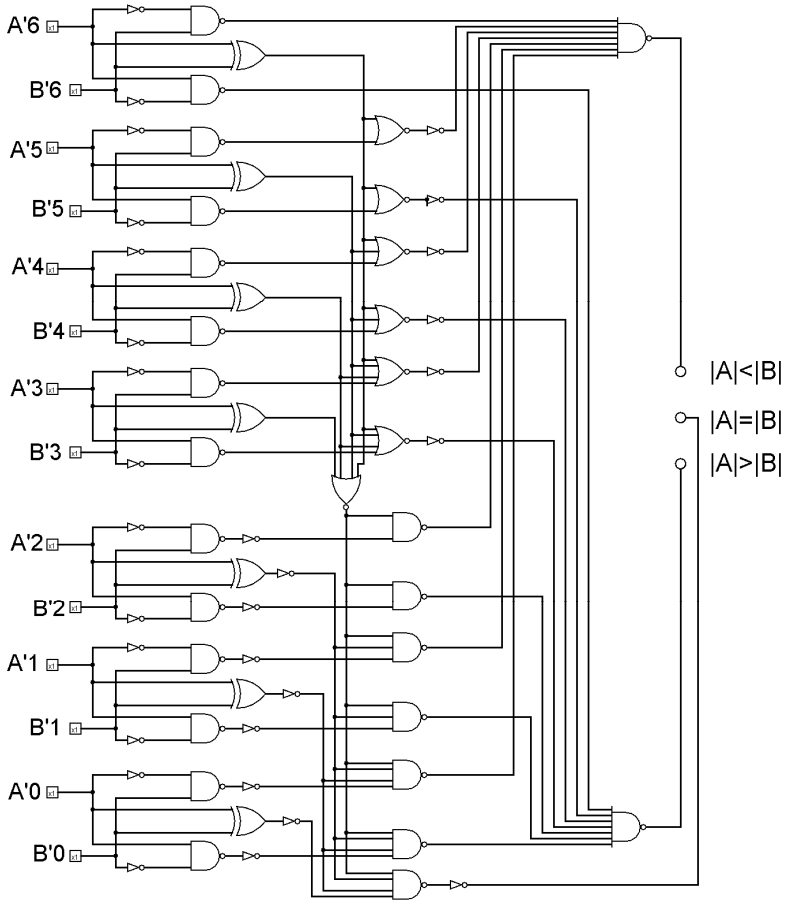


Fig. 2 Logic gate circuit of comparator (Photo/Picture credit: Original)

Instead of applying NAND gates with more than 4 inputs as what typical 8-bit magnitude comparators do, this design is more like a cascade connection of 2 4-bit detectors. Only when $A[6:3] = B[6:3]$ would the following bits be compared. Or a conclusion can be directly made according to the comparison of the first 4 bits. This design can effectively reduce the number of transistors involved.

2.3. Gates Structures

In the design, inverters, 2/3/4-input NOR, 2/3/4/7-input NAND and XOR gates. The design of corresponding logic gates is based on CMOS, considering CMOS technology is energy-efficient, stable and responsive [6]. Typically, designers of CMOS circuits often need to consider large energy consumption, and that is why optimization is required to get a balance between energy and delay.

3. Optimization Stratagems

The optimization is centered on delay and energy consumption of the critical path, which is the path with maximum delay. Considering the requirements on speed and size of real products, simply reducing delay or energy consumption are not wise choices. In order to obtain a balance between 2 significant parameters, the aim of optimization is to realize a maximum delay equaling to 1.5 times of minimum delay, or the delay when there is maximum energy consumption.

3.1. Logic Effort Theory

Logic effort (LE) theory was originally put forward by Sutherland I E et al, frequently used for estimating and reducing delay of CMOS digital circuits [7]. LE theory describes a model where the absolute delay of a logic gate equals to unit less delay, or d, times delay of load-free inverters, or τ_0 [8]. The relationship can be expressed as Equation 6.

$$d_{abs} = \tau_0(gh + p) = \tau_0 d \tag{6}$$

Where g is the logic effort of the logic gate, h is the ratio of output capacitance and input capacitance of the gate and p is the parasitic delay of the gate [9]. The logic efforts of corresponding gates are as Table 3 [6]. In the case, the width of PMOS is set to be twice of the NMOS in inverters so that there would be no declination resulting from different mobility of holes and electrons [10].

Table 3. Efforts of Gates

	INV	2-NAND	3-NAND	4-NAND	7-NAND	2-NOR	3-NOR	4-NOR	XOR
g	1	4/3	5/3	2	3	5/3	7/3	3	4
p	1	2	3	4	7	2	3	4	4

3.2. Critical Path Analysis

Critical path refers to the path with highest delay and usually the path containing most gates. Therefore, the critical path of the design is as Fig. 3. It contains 1 2-input NOR gate, 1 3-input NOR gate, 2 4-input NOR gates, 1 4-input NAND gate, 1 7-input NAND gate, 2 XOR gates and 1 inverter.

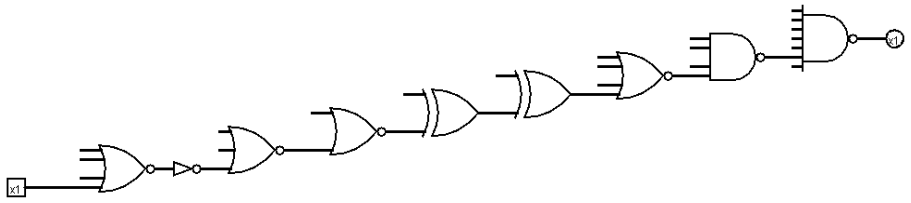


Fig 3. Critical Path (Photo/Picture credit: Original)

3.3. Critical Path Delay

The overall logic effort of the critical path satisfies.

$$G = \prod g = 3360 \tag{7}$$

$$H = \frac{C_{out}}{C_{in}} \tag{8}$$

where C_{in} are settled to be 1 unit.

$$B = \prod b = 294 \tag{9}$$

where $b = \frac{C_{on-path}+C_{off-path}}{C_{ob-path}}$ at each branch.

Based on the calculations above, the minimum delay of critical path D can be found as

$$F = GBH \tag{10}$$

$$D = N\sqrt[N]{F} + \sum p \tag{11}$$

where F refers to the effort of the whole path. The best C_{out} in this case should satisfy.

$$\frac{C_{out}}{C_{in}} = \log_{3.59}(F) \tag{12}$$

Therefore, $\frac{C_{out}}{C_{in}} = 10$, $F = 9878400$ and $D = 86.88$.

3.4. Gates Sizing

An optimization stratagem is to adjust the sizes of gates so that the fan out is distributed on the gates more uniform [11]. According to $C_{in} = g\frac{C_{out}}{f_r}$, where $f' = gh$, the sizes of gates and corresponding energy consumption should be as Table 4.

Table 4. Sizing Result with Minimum Delay

Stage	1	2	3	4	5	6	7	8	9	C_{out}
Size	1	1.07	3.41	4.64	8.85	7.04	5.60	5.93	9.43	10
Energy	2.07	4.48	8.05	13.49	15.89	12.64	11.53	15.36	19.43	102.94

Considering fraction sizes could bring extra difficulty of manufacturing, it is a good choice to optimize the path by both size and V_{DD} [11]. The sizing stratagem is based on the form as Table 5.

Table 5. Sizing Form

Stage	1	2	3	4	5	6	7	8	9	C_{out}
Size	1	1	1	1	1	1	1	1	S	10
Energy	2	2	2	2	2	2	2	$S+1$	$\frac{10}{S}+S$	

As V_{DD} is fixed at 1V, in order to realize a delay of 1.5 times minimum delay, there should be.

$$\sum g_i \frac{S_{i+1}}{S_i} + p_i = 1.5D = 130.32 \tag{13}$$

Therefore, $S_{min} = 4.76$.

3.5. Joined Optimization of V_{DD} and Size and Energy Consumption

Adjusting voltage supply to improve energy performance is a commonly applied in circuit optimization [12]. Considering the optimization objective that $D_{max} = 1.5D = 130.32$, assume $|V_T| = 0.2V$ for all transistors, there should be.

$$D \propto \frac{V_{DD}}{(V_{DD}-V_T)^2} \tag{14}$$

$$1.5 = \frac{\frac{V_{DD}'}{(V_{DD}'-V_T)^2}}{\frac{1V}{(0.8V)^2}} \tag{15}$$

Thus minimum $V_{DD} = 0.78V$. Therefore, the minimum energy consumption could be calculated as

$$E_{min} = 102.94 \times {V_{DD}}'^2 = 62.63 \tag{16}$$

According to Equation 13, S could be set as 6 so that V_{DD} could be higher, considering the MOS is not expected to work in sub-threshold region. In that case, the delay given $V_{DD} = 1V$ should be.

$$D_m = \sum g_i b_i h_i + p_i \tag{17}$$

Therefore, optimized V_{DD} should satisfy.

$$\frac{168.33}{130.32} = \frac{\frac{V_{DD-opt}}{(V_{DD-opt}-V_T)^2}}{\frac{1V}{(0.8V)^2}} \tag{18}$$

Thus $V_{DD-opt} = 0.85$ and $E_{opt} = {V_{DD-opt}}^2 \sum e_i = 20.71$.

4. Results & Discussion

The design of logic gates circuit can successfully realize absolute value comparison of 2 8-bit 2's complements, based simulation of Logisim. The scheme is optimized based on logic effort theory so that it could perform well both in energy consumption and delay. The optimization realized the balance between the 2 important parameters by setting its maximum delay equals to the minimum delay by adjusting both V_{DD} and size. In the final version, the circuit realized a minimum energy consumption equaling to 20.12% of the maximum value, as the delay is 1.5 of the minimum value.

So far, a new design of an optimized absolute value detector is put forward. Currently the optimization is only based on logic effort calculations. In the future, it is meaningful to carry on more detailed simulations and experiments to ensure the design has advantage on speed and energy efficiency. In addition, considering the shortages in energy saving and size of CMOS and the difficulty of scaling MOSFET, similar products using other types of gates, such as transition gates, also worth consideration [13, 14]. This method could reduce the number of transistors furthermore. Because of limitations of pages, detailed discussion of corresponding possibilities would not be concluded in this paper.

5. Conclusion

A high-speed and energy saving absolute value detector is designed and optimized in the essay. By redesigning logic gate structures and applying logic effort theory, the design could realize both low energy consumption and high speed. Based on the scheme, digital circuits such as arithmetic and logic units in MCU could realize faster calculation within limited space, which is meaningful for high-performance integrated circuits design.

In the future, similar method based on logic effort theory could also be applied in other high-process digital circuits analysis and design. Different technologies which require fewer transistors than CMOS could also be expected to be applied for similar missions so that the performance of integrated circuits could be further improved. In addition, it is essential for designers to consider channel length modulation and other effects that are no obvious in long-channel devices and likely to affect logic effort analysis. In high-process manufacturing, that could be significant to the circuit optimization.

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