Raptor Codes with LT-LDPC Precoding Performance Analysis and FPGA Optimization

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Abstract. Raptor codes are designed to effectively handle packet loss and erasures as a type of fountain code, capable of generating an unlimited number of encoded symbols from source informations, which is particularly useful in scenarios where the number of transmissions is unknown or variable. Luby Transform (LT) codes, a kind of fountain code encoding method, exhibit linear complexity, and Low-Density Parity-Check (LDPC) codes can be constructed by the generator matrix and the parity-check matrix. The LT-LDPC pre-coding method combines the advantages of both, enhancing encoding and decoding efficiency. Deploying code on Field-Programmable Gate Arrays (FPGAs) involves several steps: synthesis, place and route, and bitstream generation, followed by loading the bitstream onto the FPGA to configure its internal logic according to the coding methods. This paper introduces a method of encoding and decoding Raptor codes, utilizing the intimal LT codes and the peripheral LDPC codes constructed by PEG. It employs a lop-BP decoding method over noise channels based on the Tanner graph for decoding and deploys the optimized algorithm on FPGA to enhance performance.

Keywords: Raptor code, LT-LDPC code, Performance analysis, FPGA optimization.

1. Introduction

Introduced by Amin Shokrollahi in 2006, Raptor codes are a revolutionary class of fountain codes designed to enhance data transmission reliability over unreliable communication channels. As a subset of fountain codes, Raptor codes are named for their ability to generate an endless stream of encoded symbols, akin to continuously filling a fountain with water drops [1]. This feature allows for the reconstruction of original data from any sufficiently large subset of received symbols, even in the presence of packet loss. The ratelessness of Raptor codes enables the sender to produce an arbitrary number of encoded symbols without pre-determining the exact number needed for decoding. Built upon Luby Transform (LT) codes, Raptor codes introduce randomness during the encoding process through the Luby Transform, enhancing resilience against packet losses [2]. The decoding process entails collecting plentiful enough encoded symbols, allowing for the high-probability reconstruction of the original data.

Combining LT codes and LDPC codes leverages the strengths of both to create a robust error correction mechanism in communication systems [3]. LT codes are renowned for their simplicity and efficient erasure correction, offering rateless encoding with probabilistic characteristics that enhance fault tolerance. The key idea behind LT codes is based on the Luby Transform, a process that involves encoding a message into a set of symbols in a random and independent manner. These encoded symbols are then transmitted over the communication channel. The receiver collects a subset of these symbols and uses them to reconstruct the original message. LT codes have some notable characteristics. The encoding process is linear, meaning that a linear combination of codewords results in a valid codeword for the combination of the original messages. Also, the decoding process is flexible, allowing for partial decoding. This means that even if only a subset of the codewords is received, the receiver can still partially reconstruct the original message. These characteristics make LT codes suitable for scenarios where the communication channel is prone to erasures (symbols are lost) rather than errors (symbols are corrupted). Applications include reliable data transmission over networks, distributed storage systems, and peer-to-peer communication.

On the other hand, LDPC codes use iterative message-passing algorithms for decoding and sparse bipartite graphs for generating high-performance error correction near the Shannon limit [4]. Their

sparse parity-check matrix serves as a distinguishing feature. Stated otherwise, the matrix exhibits a low density of 1s, thus the term "Low-Density Parity-Check." Tanner graphs are an effective way to visualize the structure of LDPC codes. The relationships between check nodes, which stand in for parity-check equations, and variable nodes, which represent bits, are shown in a Tanner graph. A belief propagation algorithm is used to encode LDPC codes. Parity-check equations are created throughout the encoding process using the sparse parity-check matrix as a guide. For LDPC code decoding, iterative message-passing techniques are frequently utilized. One such approach is the sum-product algorithm, which is also referred to as belief propagation. These algorithms update messages across variable nodes iteratively, checking nodes in between until a decoding threshold is met or a valid codeword is obtained. LDPC codes provide performance close to the Shannon limit. This indicates that, for a certain communication channel, its error-correction performance approaches the theoretical bounds established by Claude Shannon. Digital video broadcasting (DVB), Wi-Fi (IEEE 802.11n/ac), DVB-S2 (digital video broadcasting via satellite), and 5G wireless communication are among the communication protocols that use LDPC codes. The flexibility of LDPC codes to various communication settings is well recognized. It is possible to modify LDPC codes to satisfy particular needs. It has been suggested that structured LDPC codes, including quasi-cyclic LDPC codes, can be implemented more easily on hardware by streamlining the encoding and decoding procedures. The size of the parity-check matrix and other characteristics can be changed to customize LDPC codes to match particular needs. It has been suggested that structured LDPC codes, including quasi-cyclic LDPC codes, can be implemented more easily on hardware by streamlining the encoding and decoding procedures. In contemporary communication systems where dependable data transmission is essential, LDPC codes have gained popularity due to their superior error-correction capabilities and adaptability. They are particularly well-suited for scenarios with challenging channel conditions, such as those encountered in wireless communication.

The combination of LT and LDPC codes is motivated by the idea that LT codes are particularly effective in handling erasures, which occur when symbols are lost during transmission. LDPC codes, on the other hand, excel in correcting errors in received symbols. By combining these two types of codes, the system aims to exploit the adaptability of LT codes to varying channel conditions and the exceptional error-correction capabilities of LDPC codes [5], making it ideal for advanced communication protocols where efficiency, adaptability, and high reliability are paramount.

The integration of Raptor codes, LT codes, and LDPC codes involves strategic deployment based on the characteristics of the communication channel and the specific requirements of the application.

In practical terms, the system could be designed to use LDPC codes for initial error correction, addressing random and burst errors effectively. Raptor codes and LT codes would come into play when erasures are detected, providing a rateless and adaptable framework for recovering lost information due to missing symbols. This dynamic combination allows for a flexible and efficient response to different types of errors, maximizing the chances of successful data recovery. The synergy among Raptor codes, LT codes, and LDPC codes highlights the importance of a holistic approach to error correction in communication systems. By combining these diverse coding techniques, the system gains the ability to handle a wide array of error scenarios, making it well-suited for challenging and dynamic communication environments. As technology continues to evolve, the strategic integration of these codes will likely play a pivotal role in enhancing the reliability and efficiency of data transmission across various platforms and applications.

Field-Programmable Gate Arrays, or FPGAs, are a class of integrated circuit (IC) that allows for post-manufacturing configuration and reconfiguration by designers or users. Optimizing designs for Field-Programmable Gate Arrays (FPGAs) involves customizing hardware implementation to maximize performance and resource efficiency. This process necessitates a careful consideration of design architecture, parallelism, resource utilization, and timing constraints [6].

2. Raptor code Cooperation

2.1 LT Code

LT Code, a type of graph-based fountain code, is recognized for its linear encoding and decoding complexity [7]. During the LT encoding process, two components are generated: the symbol degree d_n and the block code t_n. The degree probability distribution function is employed to randomly select the degree for each symbol, and the encoder's output is derived from the XOR operation of these degrees.

In the LT decoding process, two algorithms are predominantly used: Back-Propagating (BP) decode and Gaussian Elimination (GE) decode. The process begins by identifying a check code with a single degree. Following this, an XOR operation is performed, excess connections are eliminated, and the process is repeated to refine the decoded message. It is essential to visually represent the effectiveness of these decoding methods; thus, in Fig. 1 and Fig. 2, the error rate graphs for BP and GE decode algorithms relative to LT code are plotted to provide a clear comparison of their performance.

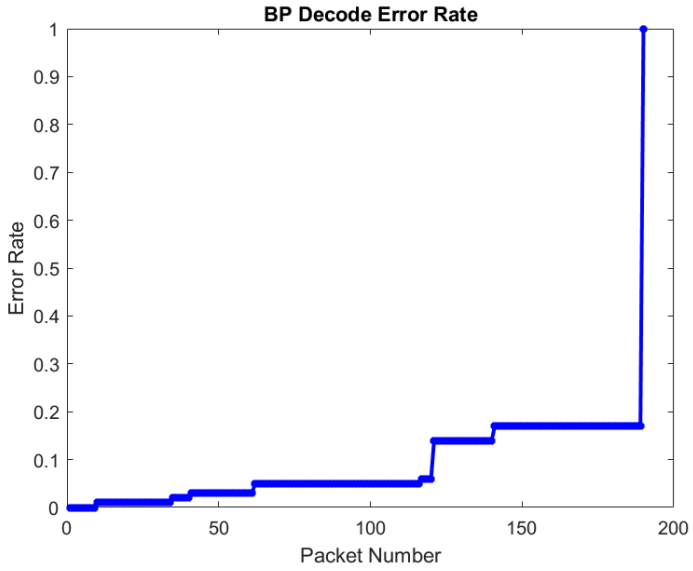


Figure 1. The graph of BP decode error rate.

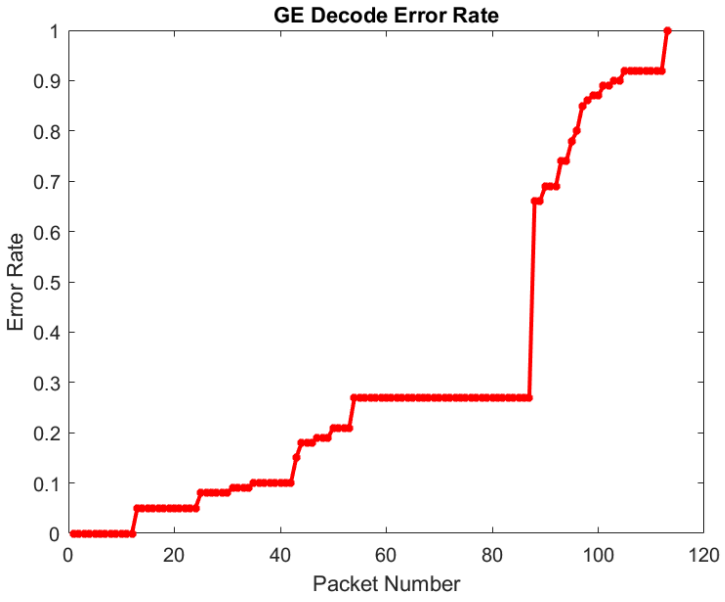


Figure 2. The graph of GE decode error rate.

2.1.1 The ideal soliton distribution

The design of both the ideal and robust soliton distribution is tailored to minimize the degree distribution for the required number of coded symbols alongside the total number of symbols modulo two additions. This distribution is distinctively characterized by a state of balance, where ripple diffusion and refraction are perfectly equilibrated. The ideal soliton distribution, specifically, is a probability distribution over integers ranging from 1 to *M*, where *M* is the sole parameter defining the distribution. This distribution's significance is visualized in Fig. 3, which illustrates the ideal soliton distribution. Accompanying this, the probability mass function, crucial for understanding the distribution's behavior, is defined by a specific equation denoted as (1).

$$P(n) = \begin{cases} \frac{1}{M}, & n = 1 \\ \frac{1}{n(n-1)}, & n = 2,3,4 \dots M \end{cases} \tag{1}$$

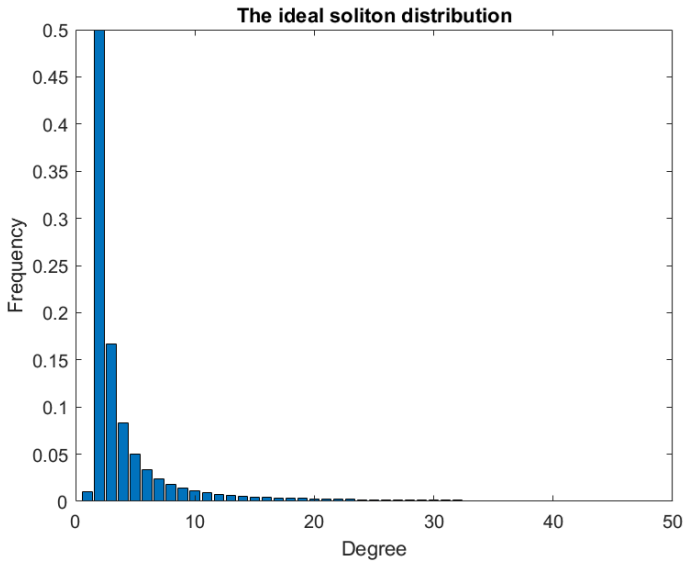


Figure 3 The ideal soliton distribution graph.

2.1.2 The robust soliton distribution

The robust soliton distribution adds extra values for the elements of the ideal soliton distribution and normalize them together. Fig. 4 shows the robust soliton distribution.

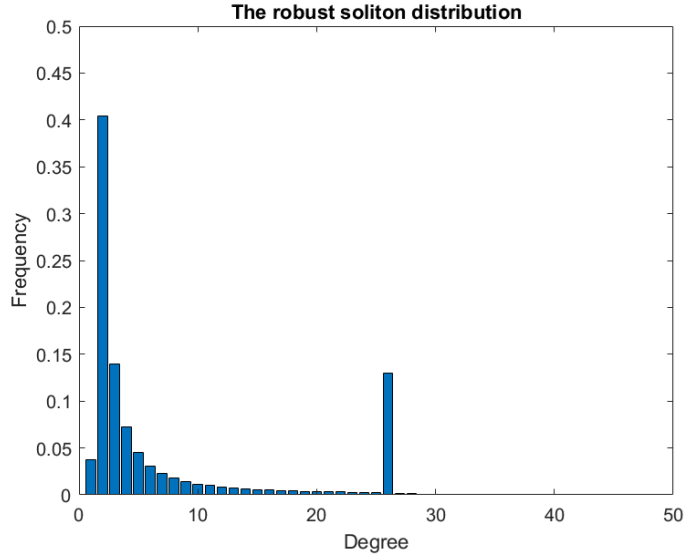


Figure 4. The robust soliton distribution graph.

In (2), define the robust distribution function and the probability mass function is same as the (1).

$$\mu(n) = \frac{P(n)+T(n)}{\alpha}, \qquad i = 1,2 \ldots, K \tag{2}$$

According to (3)(4)(5), define the T(n), α and γ.

$$T(n) = \begin{cases} \frac{\gamma}{nM}, & n = 1,2, \ldots, \left[\frac{K}{\gamma}\right] - 1 \\ \frac{\gamma ln\left(\frac{\gamma}{\delta}\right)}{M}, & n = [M/\gamma] \\ 0, & n = \left[\frac{M}{\gamma}\right] + 1, \ldots, M \end{cases} \tag{3}$$

$$\alpha = \sum_{n=1}^{K}(P(n) + T(n)) \tag{4}$$

$$\gamma = kln\left(\frac{M}{\delta}\right)\sqrt{M}, \quad k > 0 \tag{5}$$

2.2 LDPC Code

LDPC Code, a category of linear block codes, is generated by a sparse, nonsystematic parity-check matrix and is employed to correct bit errors during information transmission. The encoding of these codes involves the multiplication of information bits by this sparse matrix, resulting in the generation of codewords [8]. Decoding is primarily conducted using iterative algorithms such as belief propagation, which is designed to recover the original information from the received codewords. A notable characteristic of LDPC codes is their graceful degradation property, ensuring superior error-correction performance, even when operating near the Shannon limit [9]. An illustrative example of this, depicted in Fig. 5, demonstrates a tanner graph construction with 30 variable nodes and 15 check nodes.

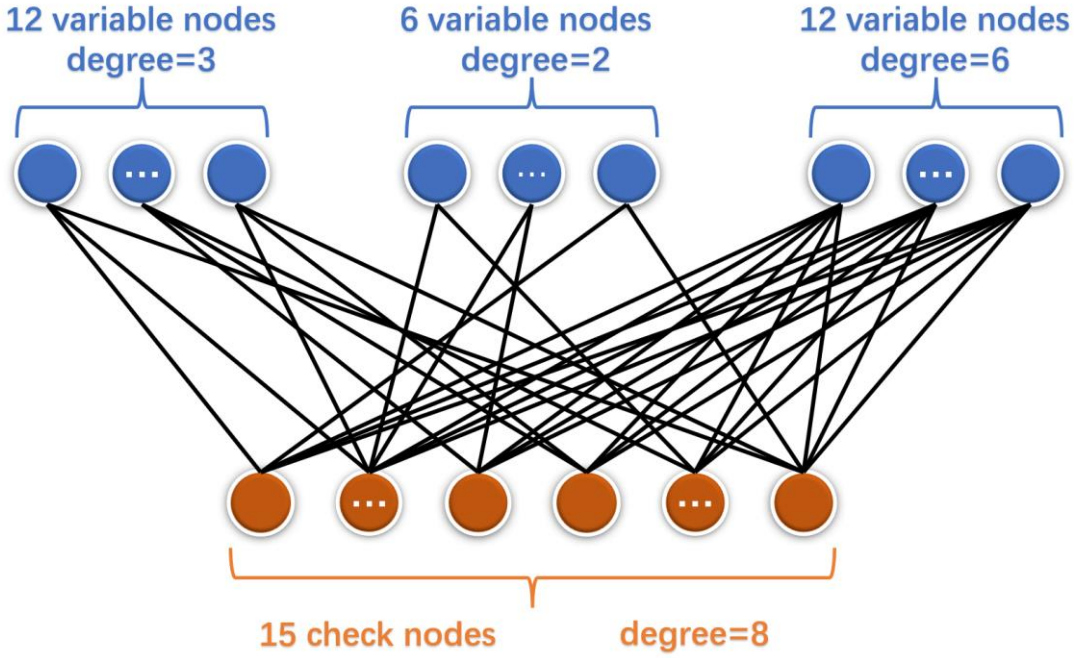


Figure 5. The tanner graph.

LDPC codes use sparse parity-check matrices, meaning that only a small fraction of elements in the matrix are non-zero, contributing to their efficiency [10]. The irregular LDPC code has the parity check matrix *H* which has different weights of rows and columns. In Fig. 6, plot the scatter graph of the irregular *H*.

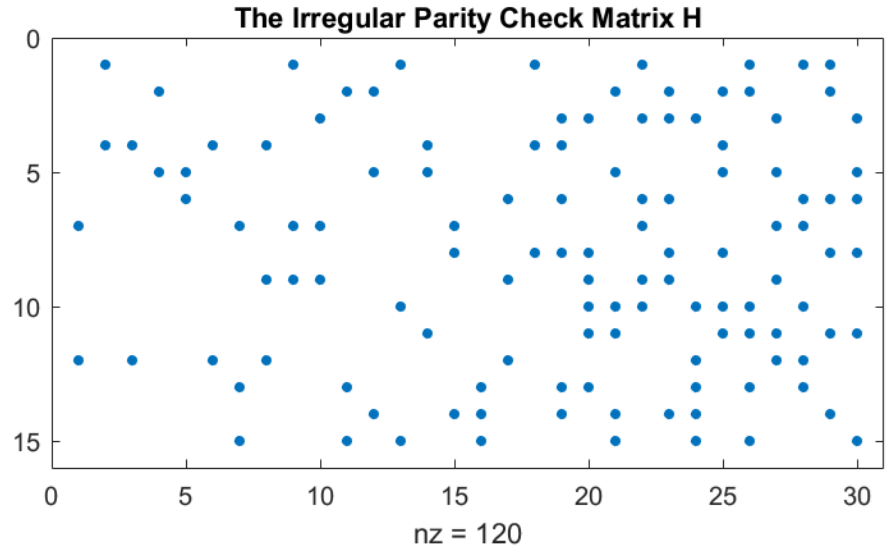


Figure 6. The scatter graph of the irregular H.

In Fig. 7, BER simulations involve assessing individual bit accuracy, revealing LDPC's capability to achieve low error rates as signal quality improves. LDPC's effectiveness is evident in applications where precise bit-level accuracy is crucial. FER simulations extend this evaluation to the frame or packet level, measuring the code's ability to recover from errors at a higher abstraction. LDPC's iterative decoding process, instrumental in achieving low BER, also contributes to its resilience against errors across entire frames. By varying parameters such as signal-to-noise ratio, code rate, and potentially decoding algorithms, a comprehensive comparative analysis provides insights into LDPC's adaptability across different communication scenarios.

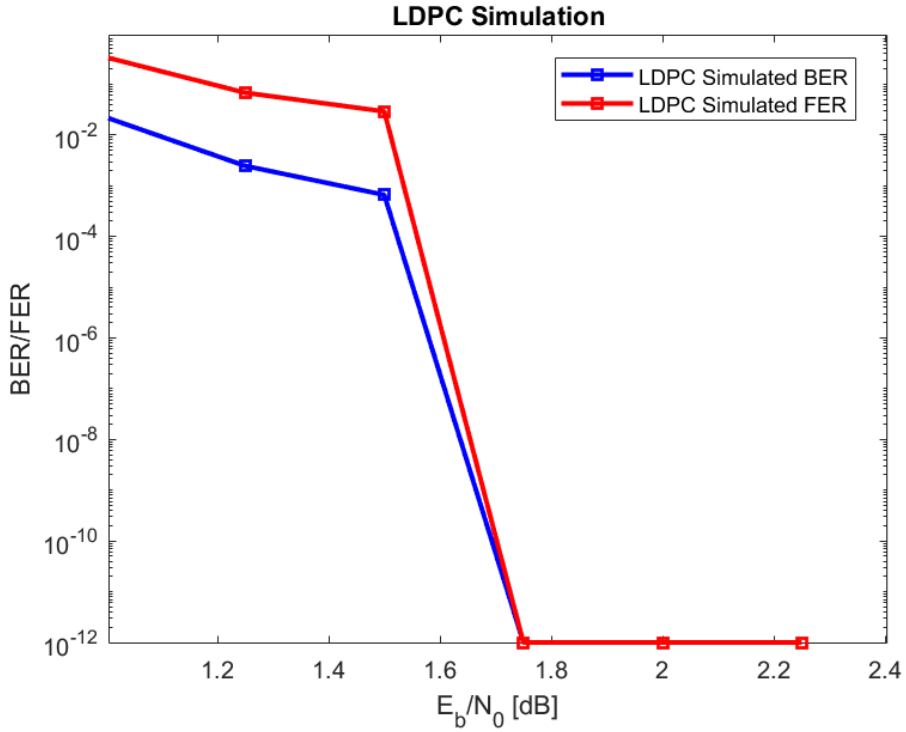


Figure 7. The BER and FER graph of LDPC simulation.

2.3 Raptor Code Cooperation

In collaborative communication scenarios, the combination of Raptor codes and Luby Transform Low-Density Parity-Check (LT-LDPC) codes provides a flexible solution. Raptor codes, with their rateless and cooperative nature, complement LT-LDPC's strong error-correction capabilities. Nodes

can cooperatively generate Raptor-encoded symbols and efficiently share them, while LT-LDPC codes contribute robust error correction during decoding. In Fig. 8, plot the relative irregular marix.

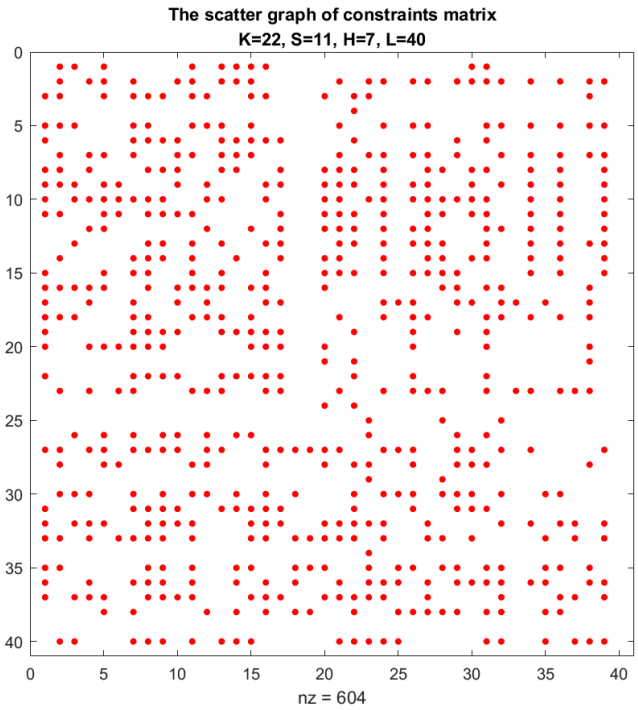


Figure 8. The scatter graph of constraints matrix.

3. Performance Analysis

The decode ways of Sum-Product (SP) Decoding Algorithm, Min-Sum (MS) Algorithm, Offset Minimum Sum (OMS) Decoding Algorithm and Non Max Suppression (NMS) Decoding Algorithm are implemented on this receiver under BPSK channel transmissions.

The Sum-Product (SP) Decoding Algorithm presents the probability of information by using the log-likelihood ratio (LLR), and this process can be structured in four steps including initialization, check nodes renewal, variable nodes updates and posterior probability information regeneration. The SPA primarily makes an assumption that the input datas have the initial probability $P_n^0 = P(x_n = 0)$ and $P_n^1 = P(x_n = 1)$, n=1,…,i. Then, compute the beginning channel information in (6), γ_n is the message with noise and σ^2 is the average noise power.

$$L(c_n) = L(q_{nm}) = log\frac{P_n^0}{P_m^1} = \frac{2\gamma_n}{\sigma^2} \tag{6}$$

The Min-Sum (MS) Algorithm is named for its use of the "min-sum" operation during message updates. At each node, it computes the minimum sum of incoming messages and adjusts the outgoing message accordingly. This process continues iteratively, gradually refining the estimates of the transmitted bits. The Offset Minimum Sum (OMS) Decoding Algorithm introduces an offset term to the LLRs, providing a means to correct for biases introduced during quantization or other sources of inaccuracy in LLR computations. This offset term helps to improve the reliability of the decoding process, especially in low signal-to-noise ratio (SNR) conditions where the impact of quantization errors is more pronounced. The NMS decoding algorithm suppresses local non-maxima and eliminates redundant by multiplying the alpha factor which value less than one.

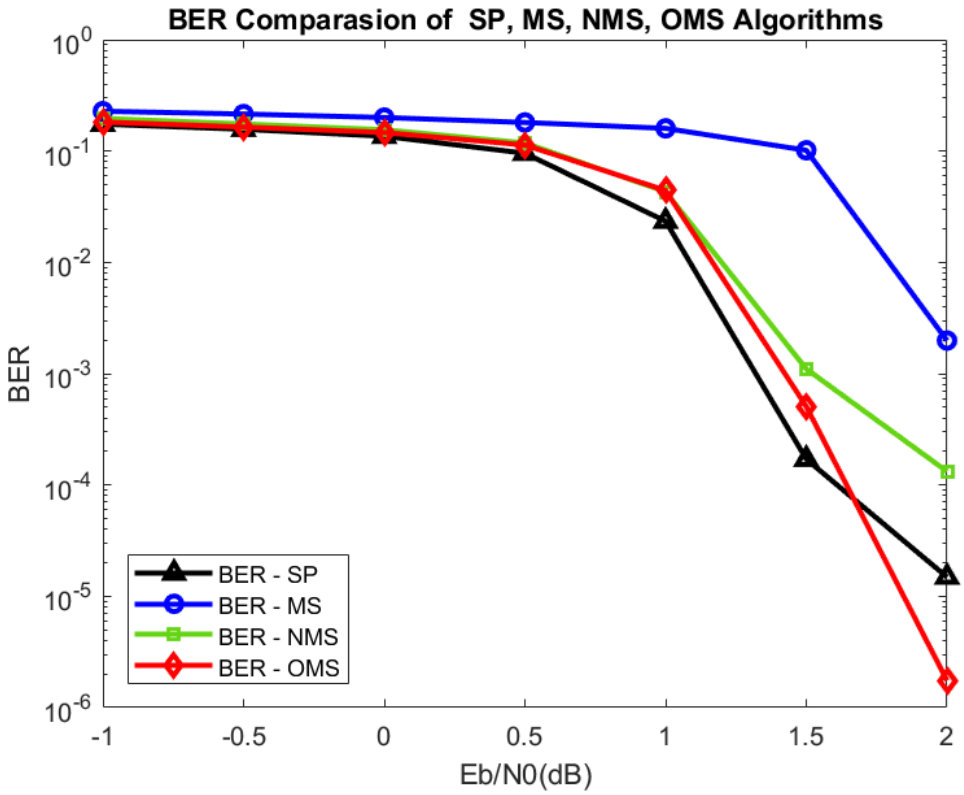


Figure 9. BER Comparasion of SP, MS, NMS, OMS Algorithms.

Fig. 9 shows the BER comparison of SP, MS, NMS and OMS algorithms. As SNR decreases, the bit error rate declines as well. These four algorithms again about the FER comparison is shown in Fig. 10.

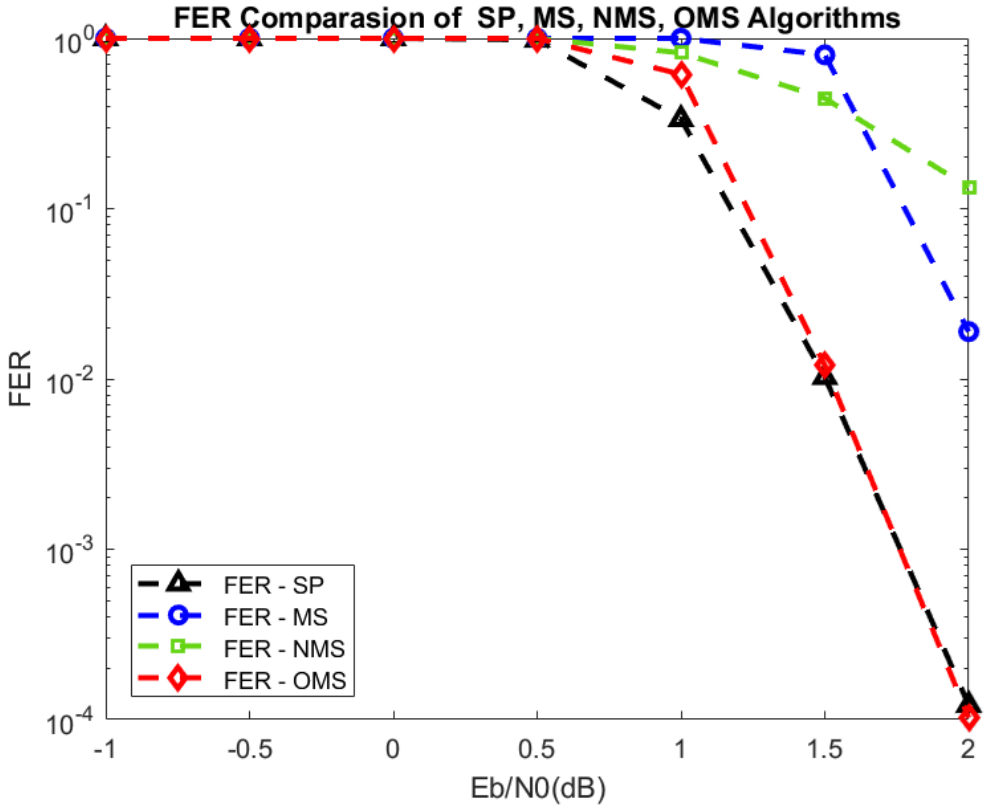


Figure 10. FER Comparasion of SP, MS, NMS, OMS Algorithms.

4. FPGA Optimization

Optimizing the deployment of Raptor codes with LT-LDPC precoding on Field-Programmable Gate Arrays (FPGAs) is crucial for achieving efficient performance. Start by capitalizing on the parallel processing capabilities of FPGAs, dividing encoding and decoding tasks into simultaneous operations to boost throughput. Considering the finite hardware resources of FPGAs, it's essential to maximize resource efficiency. Aim to reduce the consumption of lookup tables (LUTs) and flip-flops by refining the code. Investigating various code representations and algorithms is vital to identify the most effective hardware-friendly implementation.

Memory efficiency is another critical factor in FPGA implementations. Optimize the patterns of memory access, make strategic use of on-chip memory blocks, and aim to reduce the demand for external memory bandwidth. Employing memory hierarchies effectively, including registers, on-chip memory, and off-chip memory, can significantly enhance performance. These models represent the behavior and interactions of the digital circuits at the register-transfer level (RTL), and timing simulation assesses the performance of the design with respect to clock cycles, signal delays, and setup/hold times. Visual representations of these optimizations are presented by Fig. 11 and Fig. 12, which display the RTL view of the Raptor code with the LT-LDPC Precoding algorithm and the corresponding waveform, respectively.

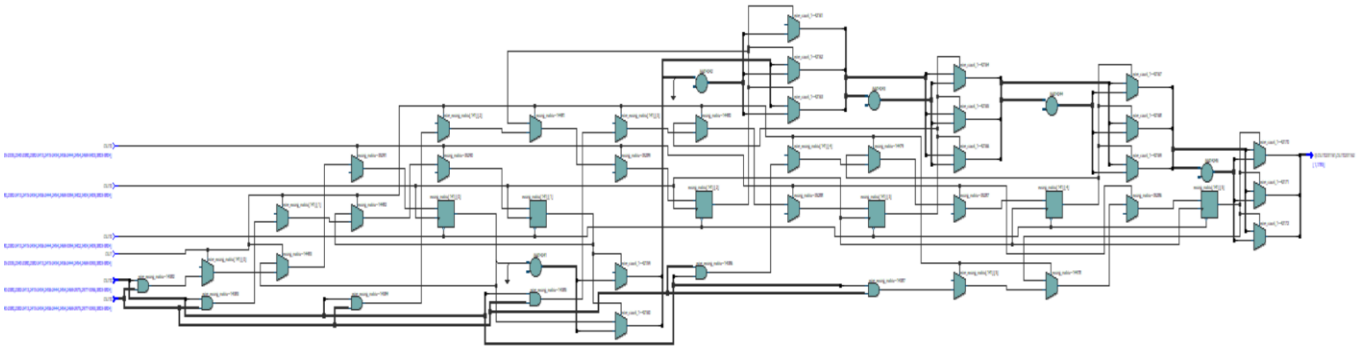


Figure 11. RTL Design.

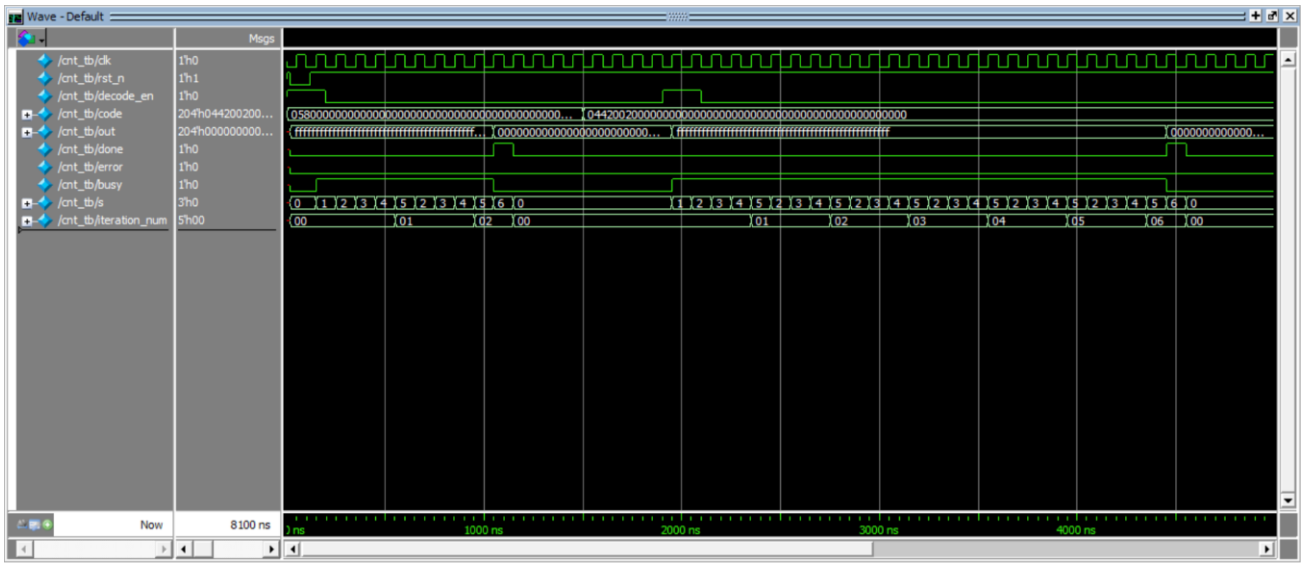


Figure 12. Modelsim Waveforms.

5. Conclusion

In this paper, the integration of Raptor codes with LT-LDPC precoding on FPGA is a promising development for boosting the transmssion efficiency and reliability of communication systems. This amalgamation capitalizes on the unique strengths of each code type, aiming to deliver robust error correction and efficient data transmission, even amidst channel noise. Such a strategy has the potential to significantly enhance the performance and reliability of data transmission in various communication environments.

Acknowledgements

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