Capacitor-Less Low Dropout Regulator Development Research

Yangyang Liu *

Bangor College, Central South University of Forestry and Technology, Changsha, China

* Corresponding Author Email: 1801010729@stu.hrbust.edu.cn

Abstract. With the popularity of portable smart devices, the electronics industry has become more and more stringent in controlling the size and cost of electronic components, and the development of low dropout regulators has become one of the key topics in today's research. Researchers have iterated capacitor-less low dropout regulators by modifying the internal and external structures of a typical model of a first-generation LDO. However, capacitor-less low dropout regulators still suffer from a series of problems, such as low transient response performance and weak interference immunity. In order to understand the problems in the industry, the researcher analyzes and summarizes the results of the methodology of the previous research by reviewing the previous literature, and through the comparison of each classical literature, combined with the advantages of each scheme, summarizes the methodology that can be combined with multiple typical models to improve the performance of the whole capacitor-less low dropout regulator, and looks forward to the direction of the future research, so that capacitor-less low dropout regulator can be further developed in the direction of more miniaturization, more energy-saving and other directions for further development.

Keywords: Low dropout regulator; capacitor-less LDO; stability; minimization; power consumption.

1. Introduction

With the development of the electronics industry and the popularity of portable devices, the application of low dropout regulators with small size, low power consumption, and high performance has become more and more widespread. However, with the need to increase the integration of portable devices, the traditional low-dropout regulators have been unable to meet the industry demand for a variety of devices. In these circumstances, the study of capacitor-less low dropout regulators meets the needs of the development of portable devices [1]. Although the capacitor-less low dropout regulator improves the integration of electronic devices, the stability and speed of the LDO will be reduced due to the lack of capacitor-less low dropout capacitors. Tianshuo Li and Yan Li. improved the transient response speed by studying push-pull buffers, flip-flop voltage followers, and swing rate enhancement circuits [2]. Ziqi Wang and Shaoqing Huang. provided a dynamic self-biased low-power capacitor-less LDO to enhance the integrated performance [3].

This article is about the study of low dropout Regulator (LDO), which focuses on the basic principle of LDO, the function of each component, and the summary of the research related to LDO as well as the optimization scheme by comparing the classical circuit of LDO. It points out the direction of development for the design and research of low dropout regulators. The aim is to show the development direction for the design and research of low-voltage differential regulators.

2. Low Dropout Regulator Fundamentals

The main structure of the LDO has a startup circuit, a reference circuit, an error amplifier, a feedback load network, a power tube, a capacitor-less load capacitor, a capacitor-less load resistor, and auxiliary protection circuits [4]. Figure. 1 illustrates the main structure of LDO.[5] It can achieve a constant output voltage within a certain range of input voltage and load variations, which makes it very useful in scenarios where the power supply voltage is unstable, or the power supply load is unstable and needs to output a stable voltage. This makes it very useful when the power supply voltage is unstable or when the power supply load is unstable and needs to output a stable voltage.

The basic principle is as follows:

The LDO is fed by a variable voltage supply, but the input voltage of the LDO must be greater than the output voltage of the LDO. The current passes through the reference circuit to output the reference current Iref and the reference voltage Vref, which is connected to the error amplifier in the next section. The current passes through the error amplifier to compare the reference voltage with the feedback voltage. When the output voltage changes, the difference in the voltage change will be sent to the error amplifier through the feedback resistor network, which amplifies the difference between these two parameters by comparing the voltage reference source and the output voltage adjusting channel resistor to maintain the stability of the LDO output voltage [6].

The current passes through the power stage, which consists of a power tube, a feedback resistor network, and a capacitor-less load capacitor. The selection of power tubes, generally uses PMOS tubes because the PMOS drain-source voltage VDS can act as the voltage difference of the entire LDO loop, as well as the difference between the input voltage and the output voltage [7]. The feedback resistor network can again regulate the output voltage via the power tube output, which can improve the output robustness of the LDO. When the input voltage fluctuates, the power stage adjusts the output voltage after getting the data from the error amplifier to keep it at the set value. After going through the entire network, the current output from the power tube is the output current of the LDO.

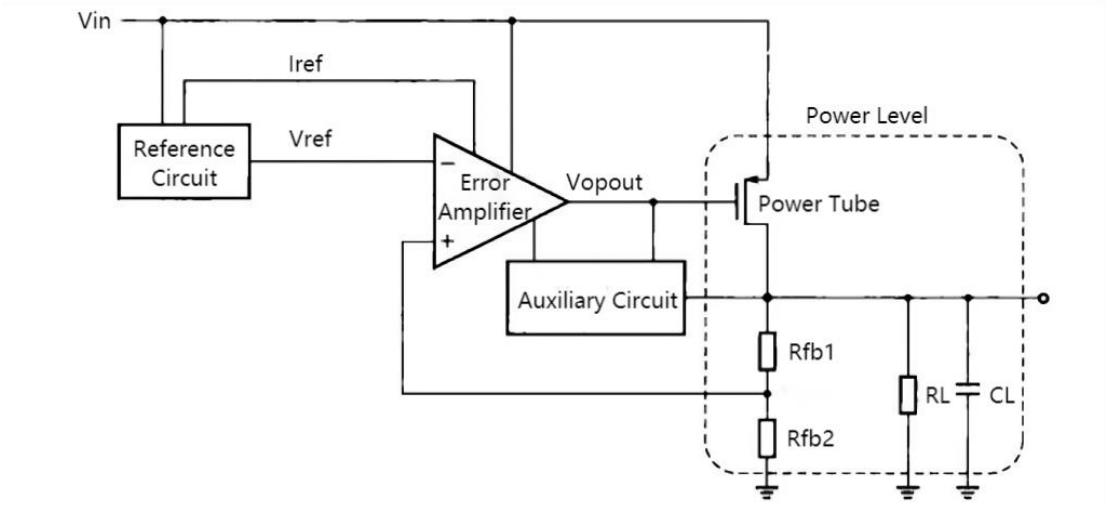


Figure. 1 Basic strctural components of LDO

3. LDO-related Module Functions

The main structures of the LDO low dropout regulator are the startup circuit, reference circuit, error amplifier, feedback load network, power tubes, outside load capacitors, and auxiliary protection circuits.

In LDO circuits, the start-up circuit is generally based on a low-voltage source (not greater than 5V), the start-up circuit allows the existence of certain voltage fluctuations (the interval is generally 2V ~ 5V) and load changes, but its minimum input voltage cannot be less than the output voltage Vout.

The reference circuit consists of a bandgap voltage reference circuit and a current reference circuit, whose functions are to give the LDO an accurate reference current and reference voltage. The main component of the bandgap voltage reference circuit is a transistor, and the main component of the current reference circuit is a constant current source. As the function of the reference circuit is set to a large extent determines the overall performance of the LDO circuit, the general situation of the bandgap voltage reference circuit to the temperature drift coefficient, supply voltage drift coefficient, output noise and power consumption to assess the performance of the bandgap voltage reference circuit is high or low; the reference current circuit by the size of the reference circuit, the temperature drift coefficient, the power supply voltage drift coefficient, noise rejection ability PSR, area to determine the current reference circuit by the reference circuit size, temperature drift coefficient,

supply voltage drift coefficient, noise rejection PSR, area to determine the performance of the current reference circuit[8].

The basic principle of the error amplifier in the LDO circuit is to compare the reference voltage generated by the reference circuit and the output voltage and subsequently output a value that is proportional to the difference between the reference voltage and the output voltage, which can control the back-end circuits and provide the output standard. The amplifier can operate over a voltage range of 2.5V to 6.5V with low power consumption is insensitive to noise and ripple and can work well under most conditions.

The power stage in this paper includes power tubes, capacitor-less load capacitors, and capacitor-less load resistors. The power tube is selected as a PMOS tube, and the drain-source voltage VDS of the PMOS tube represents the difference between the output voltage and the input voltage in the LDO circuit, and the whole power stage with PMOS as the core will become a common-source stage amplifier structure, which will, in turn, improve the gain of the LDO circuit.

In the LDO system, auxiliary protection circuits are distributed in each LDO module, and they protect the LDO from damage in extreme conditions and enhance the comprehensive performance of the LDO. Common LDO circuits include disconnect circuits, current limit circuits, and short-circuit protection circuits.

4. Capacitor-Less LDO Research Orientation

As the LDO chip removes the outside capacitance, the volume of the CL-LDO capacitance is reduced, the cost is lowered, and the integration rate of the PCB board is increased [9]. However, due to the lack of outside capacitance, the transient response performance and anti-interference of the whole LDO circuit are reduced, and at the same time, it is faced with the problem of a low power supply rejection ratio.

Conventional LDOs face stability problems due to the pole relationship between the error amplifier and the output. To overcome this problem, a pole compensation technique is generally used, i.e., a large capacitor-less capacitor (microfarads) is used. using this reduces the PSRR power supply rejection ratio of the LDO. Figure 2 shows the schematic diagram of the LDO without outside capacitance: from the figure, it can be seen that the LDO without outside capacitance replaces the outside capacitance of the traditional LDO with a small capacitor inside the chip [10].

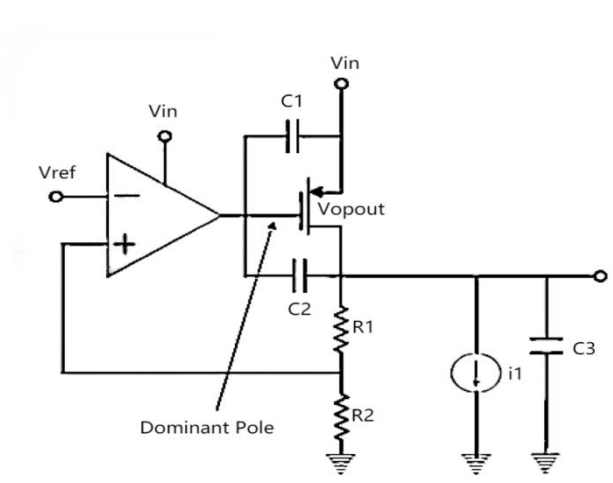


Figure. 2 capacitor-less LDO

Although capacitor-less regulators improve the integration of electronic devices, the stability and speed of LDOs will be reduced due to the absence of capacitor-less capacitors. Tianshuo Li, Yan Li . improved the transient response speed by studying push-pull buffers, flip-flop voltage followers, and swing rate enhancement circuits, but the problem of interference and crosstalk between devices is aggravated if the LDO size is reduced to deep submicron and nanoscale processes; Ziqi Wang,

Shaoqing Huang provided a dynamically self-biased low-power capacitor-less LDO to enhance the integrated performance, but the LDO The input voltage range of this LDO is narrower than typical LDO models, and the voltage conversion ratio is smaller [3]. In terms of future directions, there are the following directions.

With the further miniaturization of future smart wearable devices, the size of capacitor-less LDOs needs to be further reduced in order to improve the integration of LDOs, including simplifying the components around the transistor, integrating multiple capacitors into one to reduce the size of internal circuits, directly reducing the overall package size of LDOs by using more advanced and highly integrated packaging technologies, designing LDOs with high-frequency efficiency inputs, and simplifying the internal capacitance of LDOs without sacrificing the overall performance of LDOs by redesigning feedback resistor networks. [5]The use of high-frequency operating state of small interference between components, without sacrificing the overall performance of the LDO under the premise of simplifying the internal capacitance of the LDO, to reduce the size of the LDO at the physical level through the redesign of the feedback resistor network to achieve a higher accuracy of the internal compensation mechanism, including adjusting the frequency response of the circuit, according to the load dynamically adjust the compensation parameters, and other directions to achieve the internal and external electronic components of LDOs. Streamlining of the LDO to achieve the purpose of reducing the size of the LDO chip, etc., but the compression of the internal space will lead to the components of the heat between the components being difficult to release, and the chip operating efficiency is reduced [11].

By reducing the energy consumption of the feedback network resistor within the capacitor-less LDO, optimizing the configuration of the LDO bias current to reduce the static power consumption of the entire capacitor-less LDO, and designing a more efficient feedback control system, which in turn reduces the static power consumption of the capacitor-less LDO, and improves the service life of the device, including the addition of wide-bandgap semiconductor materials such as silicon carbide and gallium nitride, which have a good performance of thermal stability, makes it possible to make the LDO work stably even at high temperatures, and widen the optimal operating temperature range of the LDO. High-temperature conditions can also work stably, to broaden the optimal operating temperature range of the LDO [12]. However, there is still no breakthrough in the industry technology.

The use of external device control to achieve intelligent control and adaptive technology regulation, reduce or remove the LDO internal load network to achieve higher accuracy and faster speed of load regulation, reduce power consumption, and improve efficiency, which only applies to the situation where there are multiple components to be controlled.

Engineers have redesigned the connections between the modules inside the LDO, including the symmetrical design of the transistors inside the LDO, to reduce the response time of the LDO when the load changes and to satisfy the requirements of future high-demand devices that require various components, including the LDO.

Design LDOs to support a wider input voltage range, so that the LDO chip can be applied to more electronic devices, in more flexible power supply conditions, such as the design of LDOs capable of switching operating modes under different input voltages and load conditions, such as operating in buck mode under high input voltage conditions, in boost mode at lower input voltages, and in normal mode at input voltages in the range of voltages. normal mode when the input voltage is in the voltage range to broaden the input voltage range range of LDOs. Broaden the market of LDOs and increase the share of LDOs in electronic devices.

5. Conclusion

The article begins by describing the study of LDOs and finds that capacitor-less LDOs lead to higher static power consumption, lower power rejection ratio, and slower transient response due to the use of small on-chip capacitors instead of capacitor-less capacitors. The article provides four general directions, and six specific recommendations to improve the chip area, static power

consumption, power regulation, and materials, and improve the overall performance of the LDO. Electronics engineers need to provide better solutions to meet the future development needs of the electronics industry in terms of smaller capacitor-less LDO chip packages, reduced static power consumption of capacitor-less LDO chips, wider operating voltage range of capacitor-less LDO chips, and smarter capacitor-less LDO voltage feedback system strategies. The theoretical support of the current research is still lacking, and the research direction is relatively narrow, future research should provide novel research directions to make breakthroughs in the direction of the current capacitor-less LDO chip with broader theoretical support.

References

[1] Peng Y, Huang S, Duan Q. A fast transient response LDO without on-chip compensated capacitor. International Conference on Electron Device and MeChanical Engineering,2021:163-166.

[2] Li Tianshuo, Li Yan, Liu Ying, A Survey Paper on Capacitor Less Low Dropout Regulator Progress research on LDO without off chip capacitor.Application of Electronic Technique, 2023, 49(11):35-41.

[3] Ziqi Wang, Shaoqing Huang, Peilei Xiao, A dynamic self-biasing low-power LDO without capacitor-less capacitance. Modern Electronic Technology, 2023, 46(11):175 - 180.

[4] Guo J, Leung K N. A 6- W Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology.Solid-State Circuits, IEEE Journal of, 2010, 45(9):1896-1905.

[5] Wang Yi, He Lelian, CMOS low dropout regulators.Beijing: Science Press, 2012

[6] Gabriel A. Rincon-Mora, and Phillip E. Allen, Fellow, IEEE A Low-Voltage, Low Quiescent Current,Low Drop-Out Regulator IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1998,33(1).

[7] Li R, Zeng Y, Lin Y,et al. High-PSR and fast-transient LDO regulator with nested adaptive FVF structure, International Conference on Integrated Circuits, Technologies and Applications, 2020.

[8] H. Qiao, C. Zhan, Q. Pan, Y. Chen, and N. Zhang, An area-efficient low quiescent current output capacitor-less LDO with fast transient response, Int. Symp. Circuits Syst, 2021,22:21-24.

[9] Tang, Lee J, Roh J. Low - power fast -transient capacitor-less LDO regulator with high slew -rate class-AB amplifier.IEEE transactions on circuits and systems II: express briefs.2019, 66(3): 462-466.

[10] Maliha Naaz, Kaleem Fatima, B. Rajendra Naik, A Survey Paper on Capacitor Less Low Dropout Regulator, Proc. of the International Conference on Electrical, Computer and Energy Technologies ,2022

[11] Fu X , Zhou Y , Leduc P ,et al.A High-Speed Capacitor Less LDO with Multi-Loop Fast Feedback and Bandwidth Enhancement Control, IEEE International Symposium on Circuits and Systems, 2023

[12] Xu Ye, Zhang Pei-yong,A Low-Quiescent-Current Capacitor-less LDO Using an Adaptive PSR, Optimization Technique, 2022,50(7)