Ldo Chip Advanced Technology Development Exploration

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Abstract. In the wake of the exponential advancement of information technology, electronic devices are widely used in consumer, automotive, medical, and other fields, which has an escalating demand for power management chips. Low Dropout Regulator (LDO) occupies a significant position in power management chips because of its advantages of low cost, low power consumption, and simple structure, which is the basis for electronic devices to output stable voltage without ripple and low noise. The article first introduces the research background and significance of the LDO chip. Secondly, it analyzes the basic structure of LDO consisting of five modules: reference circuit, power device, resistive feedback network, error amplifier, and auxiliary circuit. The function of each module is expounded upon, and the basic operational principle of the LDO is elucidated. Finally, the research status and development trend of LDOs in the three directions of robust power attenuation, minimal idle current, and swift transient reaction. A brief explanation of the factors influencing each parameter and their respective optimization methods is also provided.

Keywords: LDO; power supply rejection ratio; quiescent current; transient response.

1. Introduction

Current consumer electronics, encompassing mobile phones, tablets, and computers, are profoundly integrated into daily life, work, and study, offering numerous conveniences to consumers. From portable electronic products such as cell phones to specialized fields such as computers and industrial equipment, all electronic products face the problem of power supply. A stable power supply is a prerequisite for the safe operation of electronic equipment, but due to fluctuations in the voltage of the externally connected power supply may cause the equipment to fail to work properly. In order to solve this problem, electronic devices necessitate the incorporation of a power management chip. This chip manages and distributes power uniformly, converting the fluctuating and noisy external voltage into a stable, low-noise power supply voltage with robust anti-interference capabilities. This voltage drives the device internal circuits, which are sensitive to voltage fluctuations, thereby playing a stabilizing role in the circuit [1].

Power management chips can be categorized into three distinct types: reference chips, linear voltage regulator chips, and switching power converters, each type possesses its unique application and structure [2]. This paper primarily focuses on two specific types of chips within the realm of switching power converters: the DC-DC converter and the LDO. These chips are of particular significance in the context of DC power supply applications.

The DC-DC converter can realize boost and buck voltage, mainly used in the case of large differences between input and output voltage. However, the ripple caused by its switching is relatively large, and its peripheral need for more components such as capacitors and inductors lead to a larger size and high cost [3]. In contrast, LDO has the advantages of low ripple, low noise, and small size, making them more compatible with circuits that require low noise and high precision supply voltages.

This paper analyzes the basic structure of LDO linear regulators and explains the basic principles of their operation by reviewing a large amount of literature. The focus is primarily on three pivotal research directions of LDO: robust power attenuation, minimal idle current, and swift transient reaction, thereby indicating the trajectory for LDO development.

2. The Basic Structure and Principles of LDO

The fundamental configuration of the LDO, as shown in Fig 1, mainly includes five modules: reference circuit, power device, resistance feedback network, error amplifier, and auxiliary circuit.

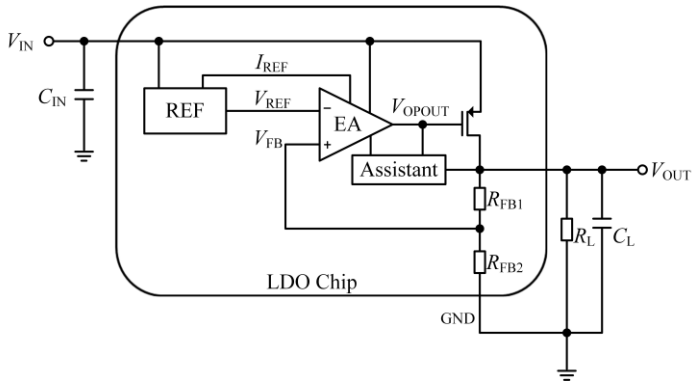


Fig. 1 Basic Structure Diagram of LDO

The main function of the reference circuit is to provide the LDO with the required stabilized reference voltage or reference current. The reference circuit REF is tied to the inverting input of the error amplifier, providing a stable benchmark voltage VREF and benchmark current IREF for the other components.

Power devices, which are typically comprised of NPN transistors, PNP transistors, and MOS transistors, play a pivotal role in the operation of the system. These components are designed to receive the output signal from the error amplifier, subsequently controlling their respective operating states. This process involves the modulation of the output current magnitude, thereby facilitating the adjustment of the output voltage. It is noteworthy that this mechanism significantly influences the driving capability of the LDO.

The resistive feedback network is composed of two voltage-dividing resistors, RFB1 and RFB2. This sampled signal is promptly feedback to the negative terminal of the discrepancy magnifier, where it is compared with the benchmark voltage. The output VOPOUT is then directed to the control terminal of the power semiconductor device to adjust its operating state. The core function of the feedback network is to adjust the ratio of the voltage-dividing resistors to set the closed-loop gain of the circuit, thereby determining the magnitude of the output voltage.

The Error Amplifier, as a key component of the LDO, significantly influences the comprehensive performance of the LDO with its various parameter indicators. The primary function of the error amplifier is to compare the feedback voltage VFB with the reference voltage VREF. By adjusting its output, it can modulate the gate voltage of the power device, thereby adjusting the size of the drive current to achieve output stability. Typically, a high loop gain of the error amplifier makes the system more sensitive to fluctuation in the load at the output end, thereby improving the regulation accuracy. However, excessively high gain may lead to instability in the LDO system. Therefore, the relationship between the stability and accuracy of the system should be a tradeoff in the design process.

In the LDO regulator, based on specific application requirements, some auxiliary circuit modules are included to enhance performance and protect the chip. Common LDO auxiliary circuits include startup circuits, slew rate enhancement circuits, over-temperature protection circuits, current limit protection circuits, as well as under-voltage and over-voltage protection circuits [4].

The core operational concept of the LDO regulator is to manage the output voltage by employing a system of negative feedback in order to maintain stability at the reference voltage. The LDO negative feedback loop operates in the following manner: As the output potential of LDO VOUT rises, the feedback voltage VFB, acquired through voltage division using feedback resistors RFB1 and RFB2, also increases. When both the feedback voltage VFB and the reference voltage VREF are fed into the error amplifier EA at the same time, the output voltage VOPOUT will increase. As a result, the base-emitter voltage difference of the transistor is diminished, as the gate voltage is increased. The transistor's leakage current reduces, leading to a reduction in the voltage differential

VOUT across the feedback resistors RFB1 and RFB2, thus enabling the negative feedback function. When VOUT decreases, the feedback voltage V_{FB} will fall as well. This will result in a decrease in the output voltage V_{OPOUT} of the error amplifier EA, leading to an increase in the base-emitter voltage differential of the transistor. Consequently, the transistor residual current will rise, resulting in an increase in the output voltage V_{OUT}.

3. Research Directions in LDO

Through comparative analysis of domestic and international literature in recent years, it can be observed that the current development trend of LDO regulators primarily focuses on several performance parameters, including robust power attenuation, minimal idle current, and swift transient reaction.

3.1. High Power Supply Rejection Ratio

The Power Supply Rejection Ratio (PSRR) refers to the circuit ability to suppress power supply ripple. This parameter reflects the ability to resist interference from power supply input noise, thereby playing a pivotal role in assessing the impact of the power supply on the output. For the LDO regulator, a higher PSRR value is indicative of a heightened ability of the circuit to resist power supply input noise. According to relevant research, the PSRR of the LDO can be improved by adding an RC low-pass filter circuit or cascading a transistor to reduce the noise of the power supply [5].

In 2020, Huang C et al. proposed a high-performance LDO regulator. Through the incorporation of a programmable recursive binary resistor array, the primary control circuit of this LDO regulator exhibits a high gain bandwidth. It is furnished with a brief speed enhancement route and a singular power supply disturbance gain creator, proficient in sustaining a power supply rejection ratio of 60 dB within the frequency band of 0-1 MHz [6].

In 2023, Yanhan Zeng et al. proposed an LDO that eliminates the need for output capacitance. This circuit employs dual buffering stages to bolster both loop equilibrium and the current of the load. They also suggested sophisticated methods for enhancing PSRR, specifically feedforward PSRR and a PSRR technique that utilizes equivalent negative capacitance. These techniques significantly enhanced the PSRR performance at frequencies of 10 kHz and 100 kHz, achieving gains of 24 dB and 38 dB respectively [7].

As the fabrication scale progressively reduces and the demand for low power consumption of mobile devices increases, the supply voltage is further reduced. Future LDO research targets focus on low-supply voltage application scenarios, which puts forward higher requirements for the PSRR performance of LDO.

3.2. Low Quiescent Current

The quiescent current primarily consists of the bias current and the drive current of some power devices, and its magnitude affects the efficiency of the LDO regulator. Due to the thermal effect of the current, an excessive quiescent current may cause an increase in the internal temperature of the chip, leading to chip burnout. Therefore, the efficiency of the LDO can be improved and chip burnout can be prevented by reducing the bias current and circuit branches, using a low-power reference voltage source, and employing an error amplifier with low quiescent current [8].

In 2020, Mii Kenji et al. proposed an LDO with ultra-low quiescent current. This regulator employs a load transient enhancement circuit based on a flipped voltage follower. During no-load operation, the LDO consumes a quiescent current of 204 nA [9].

In 2022, Hanyang Univ et al. proposed an LDO with reduced quiescent current. They also introduced a capacitance feedforward fluctuation suppression method to eradicate disturbances from the power source. This approach employs feedforward capacitors and consecutive pseudo-resistor biasing to attain energy efficiency. The total idle current consumed by the proposed LDO is 0.9 μA [10].

The quiescent current of LDO is a key factor that determines the standby time of portable electronic devices. Reducing quiescent current can not only improve the energy efficiency of LDO but also enhance the portability of electronic devices. Therefore, the future quiescent current research of LDO will focus on how to reduce quiescent current.

3.3. Rapid Transient Response

The LDO transient response pertains to its capacity to adapt and stabilize in response to fluctuations in supply voltage or load, which is due to the inability of the power tube gate voltage to mutate. To swift the transient reaction of the LDO, improving the fundamental yaw rate and expanding the closed-loop bandwidth is achievable. The specific measures are to adopt a high conversion rate error amplifier and a power tube base yaw rate boosting circuit and to use dynamic bias to detect the load change.

In 2021, Yu Peng et al. proposed a rapid reaction to transients in an LDO circuit that does not require on-chip compensation capacitors. This setup utilized an active class-AB transient amplification circuitry based on a differentiator, with a reaction time of only 1.58μs [11].

2022 A. T. Grăjdeanu et al. proposed an LDO circuit with a fast load transient response. The circuitry can respond more swiftly to alterations in the emitted voltage by incorporating an internal feedback cycle that connects the AC supply to the LDO output. and associates the output with the control terminal of the power semiconductor device [12].

The LDO transient response efficacy is intimately tied to the loop bandwidth, the amplification, and the control potential oscillation rate of the energy-switching transistor. Boosting the power transistor gate oscillation rate can hasten the LDO response pace. However, the gate of the high-capacity transistor might generate substantial parasitic capacitance, constraining the LDO reaction duration. Increasing the loop bandwidth can shorten the system response time, but it may affect the system stability and increase the static power consumption. Hence, the crux of ongoing research is enhancing the transient reaction of LDO without compromising the performance of other system aspects.

This chapter delves into the three primary research directions of the LDO regulator, highlighting the complex interdependencies and mutual influences among the LDO parameters. The design of LDO should be considered in many aspects, optimizing specific parameters based on particular application scenarios, while potentially de-emphasizing less critical parameters.

4. Conclusion

This paper introduces the research background and significance of LDO, analyzes the current development trend, and proves that this topic has practical research value. It briefly describes the basic structure and working principle and analyzes three main research directions: robust power attenuation, minimal idle current, and swift transient reaction. The research focuses on three topics: how to improve the power rejection ratio in low supply voltage scenarios, how to reduce the quiescent current to improve the standby time of the mobile device, and how to swift transient reaction of the LDO without sacrificing other system performance. This paper recognizes that the LDO circuit design process needs to sacrifice part of the less influential parameter performance for specific optimization for application requirements. There are still many shortcomings in the current research, and simulation and verification are not carried out due to the time problem. Simulation software can be used for system-level simulation and layout design in future research.

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