

Application and Research of Voltage-Controlled Oscillator in Phase-Locked Loop

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Abstract. The first PLL chip in history was created by some researchers in the middle of the 1960s. PLL has significant uses in numerous industries, including communication and aerospace, because to its clear benefits. It can accomplish a wide range of tasks at a reasonable cost. This paper delves into the application and study of Voltage-Controlled Oscillators (VCOs) within Phase-Locked Loops (PLLs), crucial components in modern communication technology. Various VCO design techniques, including Colpitts, Clapp, ring oscillator, and CMOS VCOs, are analyzed with a focus on performance metrics such as phase noise and tuning range. The research also presents innovative high-performance VCO designs, showcasing advancements in frequency switching and phase noise reduction. Practical applications of VCOs within PLLs are explored through case studies, highlighting their role in aerospace sensorless control schemes and communication system distributed beamforming. The paper underscores the significance of VCOs in achieving stable frequency outputs and enhancing system performance, offering insights into future advancements in communication technology. Through detailed analysis and case studies, The goal of this research is to support the continuous improvement and enhancement of VCOs in PLL systems.

Keywords: VCO, PLL, CMOS.

1. Introduction

In recent years, advancements in wireless communication have spurred significant developments in communication technology. Among these innovations, Voltage-Controlled Oscillators (VCOs) have emerged as crucial components, particularly in Phase-Locked Loops (PLLs). A module called a phase-locked loop (PLL) gives the circuit system a steady clock, high frequency, and high precision. As transceiver systems, high-speed data processing systems, and wireless communication systems continue to advance, so too do the performance requirements for PLL [1]. PLL with higher frequency, wider bandwidth, and lower noise has always been a common problem in the field of high performance integrated circuits [2]. VCOs serve as the heart of PLLs, generating adjustable-frequency signals essential for various applications like frequency synthesis, clock recovery, and frequency tracking.

This paper delves into the application and research of VCOs within PLL systems. It begins by exploring the design techniques of VCOs, comparing various types such as Colpitts, Clapp, ring oscillator, and CMOS VCOs. Key metrics like phase noise and tuning range are discussed to evaluate VCO performance. The study then shifts focus to high-performance VCO designs, presenting cases such as continuous-frequency switching VCOs and LC VCOs with impressive specifications.

Further investigation is conducted into the practical application of VCOs within PLLs. The role of VCOs in achieving stable frequency outputs, enhancing communication system performance, and enabling distributed beamforming is analyzed through case studies. These cases range from aerospace applications, where sensorless control schemes are employed, to communication systems using PLL-assisted distributed antenna arrays.

2. Typical VCO design techniques and comparison of different types of VCOs

The academic community has been working to improve the speed and efficiency of communication technology in recent years, thanks to the invention of wireless communication.

To satisfy more stringent communication standards, the structure of VCO is being examined and enhanced.

This research categorizes four approaches to maximize VCO that have been studied in the various domestic and international literatures to date: colpitts VCO and clapp VCO, ring oscillator VCO and CMOS VCO. The passive components of a VCO such as inductors and capacitors are one reason that limit the oscillator's performance.

A common VCO design that creates oscillations using a feedback loop consisting of one or more transistors and capacitors is the colpitts VCO. colpitts VCO: the oscillation frequency is modulated by varying the feedback capacitor's voltage [2]. In order to increase frequency stability, the clapp VCO, a variation of the colpitts VCO, adds a fixed capacitor in parallel to the colpitts structure [3].

One kind of VCO constructed with a multistage inverting amplifier is a ring oscillator VCO. Typically, an odd number of inverters are connected in a ring, and each stage's delay or gain is adjusted to control the VCO frequency [4].

A type of voltage-controlled oscillator created and utilised by CMOS technology is the CMOS VCO. The CMOS VCO is a popular integrated circuit component, particularly in radio frequency and communication systems, due to its low power consumption, low phase noise, and excellent integration performance [5].

Colpitts VCO is ideal for medium and high frequency, and it is straightforward to change; ring VCO with adjustable frequency adjustment and suitability for digital integration; a fixed capacitance based on Colpitts is added to the Clapp VCO to improve its frequency stability. CMOS VCO reduced phase noise, broad frequency range, and low power consumption. When designing a system to suit its requirements, factors including power consumption, adaptability range, and structural simplicity should be taken into account. For electronic engineers, the comparison of different VCO design methods offers a valuable resource.

3. High performance VCO design

Phase noise and tuning range are crucial metrics for assessing VCO performance [6,7]. A compromise approach must be found to build a VCO because achieving both broad tuning range and low-phase noise can be challenging. These days, modern communication equipment frequently has a high demand for VCO phase noise in order to reduce interference to other devices. Furthermore, the communication device's practicality and compatibility increase with the greater tuning range of VCO.

Yuri Lu et al. presented a continuous-frequency switching VCO based on a 40 nm CMOS technology from East China Normal University in 2022. To attain a greater linear voltage tuning gain, the proposed circuit uses complementary PMOS and NMOS varactors. Its frequency ranges are 23.38 GHz to 27.63 GHz, its KVCO is 0.56 GHz/V to 1.12 GHz/V, and its phase noise at 1 MHz frequency offset is -106.6 dBc/Hz [8].

Based on 65 nm CMOS technology, Kai Sun et al. from Southeast University suggested an LC VCO with high-quality factor inductance in 2021. In order to attain a high Q value, the construction suppresses the skin effect of inductance within the working frequency range by using parallel double-turn single-width inductors. With a frequency offset of 10 MHz, the VCO has a phase noise of -136.57 dBc/Hz and is tuned between 11.8 GHz and 15.3 GHz [9].

Colpitts and Clapp VCO, for example, exhibit good noise performance because to their capacitive three-point structure. The China Academy of Engineering Physics' Xinlin Xia and colleagues presented a low phase noise GaAs Colpitts VCO in 2020. The heterojunction bipolar transistor emitter of the VCO has an inductor on it that raises the , making it easier to initiate vibrations and increasing oscillation speed. This oscillator also employs a collector-emitter cross-coupling capacitance, which lowers the transformer ratio and increases the resonator's quality factor and oscillation amplitude while also lowering phase noise. The VCO has a phase noise of -137.44 dBc/Hz at 1 MHz offset and is adjusted between 3.25 GHz and 3.4 GHz [10]. Table 1 provides further details about the previously cited literature.

Table 1. Three Scheme comparing

Ref.	Process (nm)	VDD (V)	FTR(%)	Core frequency(Ghz)	Power consumption(mW)	Phase noise(dBc/Hz)
Ref. [8]	40	1.1	16.5	25.5	12.69	-107@1MHz
Ref. [9]	65	1.2	26	13.6	14.4	-137@10MHz
Ref. [10]	2000	5	4.5	3.4	45	-137@1MHz

The dual-tail current biasing technique improves the oscillator's phase noise performance by introducing a controllable phase shift in the Voltage-Controlled Oscillator (VCO)'s coupling path. This is accomplished by gating the self-tail current with anti-phase signals to introduce a tunable phase shift in the total bias current and by gating the coupling-tail current with quadrature signals to maintain the quadrature state [11]. This technique allows for reconfigurability to mitigate performance degradation caused by process variations. Improving the phase noise and tuning range of the VCO is the main goal in creating a high-performance VCO design.

4. The application of VCO in PLL

The Voltage-Controlled Oscillator (VCO) plays a key role in the Phase-Locked Loop (PLL). As one of the core components of the PLL, the VCO is responsible for generating a signal of adjustable frequency and comparing it with a reference signal to adjust the output frequency. In the closed-loop control of PLL, the frequency output of the VCO is regulated by the control voltage, usually through a feedback control circuit. The basic principle of VCO is to use voltage to control the oscillation circuit's frequency, and adjust the oscillation frequency by changing the control voltage to realize the functions of PLL, such as frequency tracking, clock recovery and frequency synthesis [12]. As illustrated in Figure 1, PLL's fundamental construction.

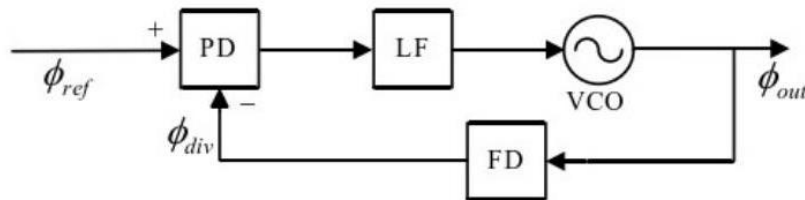


Fig. 1 Basic structure of phase-locked loop [13].

In real-world applications, the output signal's frequency can be slightly changed to maintain a steady relationship with the phase and frequency of the reference signal by altering the control voltage of the VCO. This stability and accuracy make VCO widely used in communication systems, RF modulation, clock generators, and other fields, providing reliable timing control and signal processing basis for the system. By understanding VCO's role and regulation principle in PLL, engineers can better design and optimize PLL circuits to improve system performance and stability.

The continuous advancement of theories and technologies associated to PLL has resulted in significant improvements in the performance of related goods in recent years, and a substantial amount of research data has been gathered.

In 2020, the University of Electronic Science and Technology of China designed a high-speed and low noise PLL. Under the 40nm process, the output frequency of the PLL is between 1.7 and 3.05GHz. Under the 2.5GHz frequency, the locking time is 3.2, the power consumption is 27.3mW, and the phase noise is -111.4 dBc/Hz@1MHz. The jitter obtained by integrating over the interval [1K, 100M] is 436.5fs [13]. In 2020, Zhejiang University designed a single-loop charge pump PLL and an innovative two-loop charge pump PLL, both of which can operate at a voltage combination of 1.8V and 2.8V analog supply voltages and 1.5V and 1.8V digital supply voltages. Both of them support input reference frequencies ranging from 6 MHz to 40MHz, and by adjusting the frequency division

ratio, both of them can achieve the frequency adjustment range of 0.4 GHz to 1.5 GHz. At the operating frequency of 945MHz: single-loop PLL lock time is 3, TIE jitter value is 23.3ps, Period jitter value is 1.22ps, Long Term jitter value is 33.5ps, power consumption is 2.875mW, area is 0.0571. The two-loop PLL lock time is 25, TIE jitter value is 18.2ps, Period jitter value is 1.21ps, Long Term jitter value is 26.4ps, power consumption is 3.058mw, and area is 0.0397 [14].

In order to obtain performance equal to tabletop instruments, Jong-Yoon Park et al. created a portable quartz crystal microbalance (QCM) measuring system. The QCM measuring system was customized using PLL electrical circuits, which made it possible to create a battery-powered, compact, and reasonably priced QCM system. During a 0.1-second measurement interval, the device successfully detected two common volatile organic compounds (VOCs), methanol and dichloromethane, with a minimum frequency resolution of around 0.22Hz [15].

Researchers Jagdeep and colleagues created a PLL in 2021 that has a wide frequency range, a compact size, and minimal phase noise. The PLL uses 0.18mCMOS technology to efficiently increase locking speed; at 1.6GHz and 1.8V, the output frequency and voltage have just 2.13ps of jitter. Phase noise of -137dBc/Hz and power consumption of 2.63mW can be attained in the case of 1.6GHz and 100MHz frequency offset, respectively [16]. Table 2 summarizes the performance of the different PLL research techniques described above.

Table 2. Comparison of different PLL research techniques [13, 14, 15, 16].

Ref.	Process (nm)	Output Frequency Range (GHz)	Locking Time (ns)	Power Consumption (mW)	Noise (dBc/Hz @ 10MHz)	Jitter (ps)	Area (mm ²)
Ref. [13]	40	1.7 - 3.05	3.2	27.3	-111.4	436.5 (1K-100M)	n.a.
Single-loop Ref. [14]	n.a.	0.4 - 1.5	3	2.875	n.a.	23.3 (TIE), 1.22 (Period), 33.5 (Long Term)	0.0571
Two-loop Ref. [14]	n.a.	0.4 - 1.5	25	3.058	n.a.	18.2 (TIE), 1.21 (Period), 26.4 (Long Term)	0.0397
Ref. [15]	n.a.	n.a.	n.a.	n.a.	n.a.	0.22 (minimum frequency resolution)	n.a.
Ref. [16]	0.18	1.6	n.a.	2.63	-137	2.13 (1.6GHz), - (100MHz offset)	n.a.

Broadly speaking, low power consumption, high locking efficiency, low noise reduction, wide band, etc. are the key features of the present PLL development trend. Studies on pertinent technologies are conducted to enhance PLL performance even more.

5. Research on VCO applications in PLL communication systems and aerospace

In order to provide the best possible performance in terms of high working frequencies, low noise, small area, and low power consumption, circuit design techniques have been pushed to their limits by the high data processing and bandwidth needs of wireless/wired communications and aeronautical systems.

Jinquan Xu et al. suggested a novel sensorless control approach for a permanent magnet synchronous motor (FTPMSM) drive system to increase its fault tolerance for the aerospace VCO use case in PLL [17]. The applied non-orthogonal PLL design is shown in Figure 2.

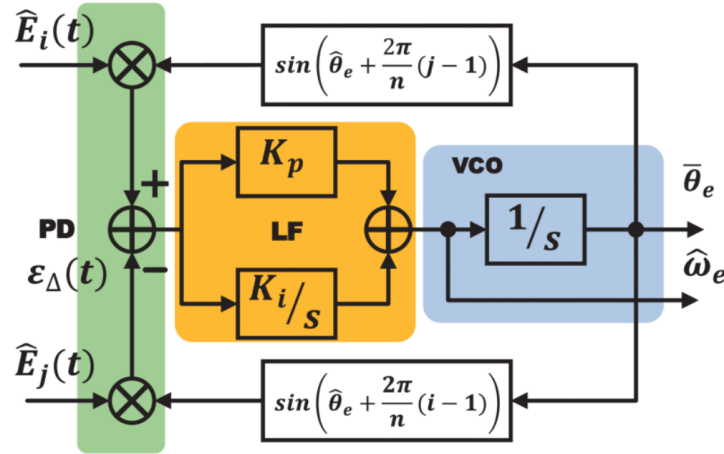


Fig. 2 Non-orthogonal PLL design [17].

Even in the event of phase open and short faults in the FTPMSM, sensorless control performance at medium and high speeds is guaranteed by the use of a resilient observer, non-orthotropic phase-locked loop (PLL), and variable phase delay compensation. Back electromotive force (EMF) estimations for any two normal phases can be obtained thanks to the robust observer, which is unaffected by phase defects, external interference, or parameter changes. In the meantime, two observed non-orthogonal opposite electromotive forces are used to derive rotor position information using non-orthogonal PLL. The high-frequency noise of the measured phase back electromotive force is removed by introducing a variable cutoff frequency low-pass filter (VLPF) to increase the accuracy of the rotor location estimation when the speed varies. Furthermore, phase delay correction is suggested as a way to offset the estimation variation brought on by VLPF. The research demonstrates that the sensorless FTPMSM system has good speed control performance under both normal and fault scenarios by verifying the six-phase FTPMSM system experimental platform. This study demonstrates VCO's significance and prospective utility in PLL applications, particularly in the aerospace industry where high performance and reliability standards are required. This sensorless control approach offers fresh perspectives and technical assistance for developing and implementing motor drive systems.

Qi Xiang et al. proposed a single-event hardening scheme to suppress radiation effects in aerospace environments for phase-locked loop (PLL) Microsystems [18]. The model of CP hardening is shown in Figure 3.

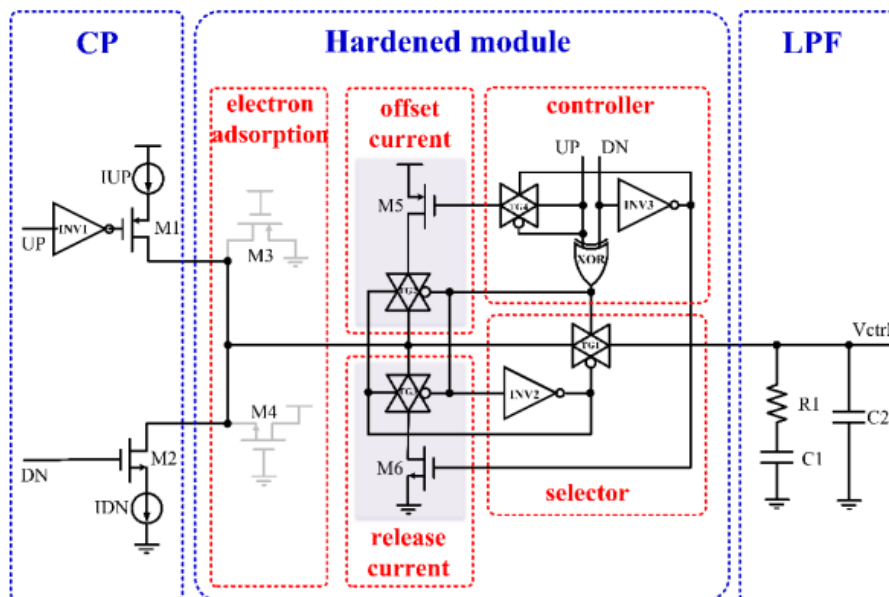


Fig. 3 The suggested CP is SET-hardened [18].

An effective charge pump hardening strategy was created using radiation hardening design (RHBD) technology to increase the PLL microsystem's ability to suppress radiation impacts. An analysis is conducted on the sensitivity of single event transients (SET) at various charge pump nodes and bombardment energies. To suppress single-event impacts without altering the original structure and loop parameters, a phase-locked loop hardening approach is developed. The addition of a digital control circuit between the low-pass filter and the charge pump significantly lowers the charge pump's sensitivity to SET. The single-event transient effects of unstrengthened and strengthened phase-locked loops are simulated and the validity of the suggested strengthening strategy is confirmed using the conventional double exponential current pulse model. The performance comparison of PLLS before and after hardening is compiled in Table 3. Table 3 displays PLL's performance both before and after hardening.

Table 3. Comparison of PLL performance before and after hardening [18].

Performance Parameter	Non-hardened PLL	Hardened PLL
Supply voltage	1.2 V	1.2 V
Output frequency range	0.6 GHz~1.6 GHz	0.6 GHz~1.6 GHz
CP working current	25 μ A	25 μ A
CP current mismatch	0.65%	0.67%
Control voltage ripple	8 mV	8 mV
Lock time@0.8 GHz	2.3 μ s	2.5 μ s
Power consumption	8.56 mW	9.12 mW
Area	265 μ m $\times$ 199 μ m (1 $\times$)	275 μ m $\times$ 207 μ m (1.08 $\times$)
SET response		
Vctrl fluctuation peak	112.3 mV	6.5 mV
Recovery time	1031 ns	254.3 ns
Number of error pulses	7	2
Maximum phase error	86.58 $^{\circ}$	7.93 $^{\circ}$

The proposed single-event hardening scheme reduces the transient response wave peak value of the phase-locked loop by 94.2%, increases the locking recovery time by 75.3%, and reduces the maximum phase offset by 90.8%, according to simulation results based on SMIC 130 nm standard complementary metal oxide semiconductor (CMOS) process. This implies that PLL Microsystems' sensitivity to single-event effects can be successfully decreased by this hardening method. This work offers a novel method for mitigating radiation impacts while using VCO in PLL for aerospace applications.

For a communication system VCO application case in a PLL, The impact of phase noise in phase-locked loops (PLLs) and voltage-controlled VCOs (VCOs) on distributed beamforming in distributed antenna arrays was investigated by Serge R. Mghabghab et al [19]. The coherent distributed array is shown in Figure 4.

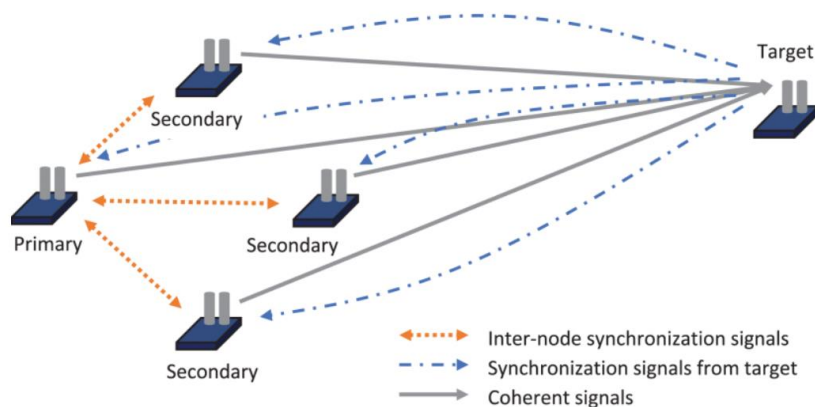


Fig. 4 coherent distributed array [19].

A high degree of coordination between the relative electrical states of the system is required for distributed beamforming among several wireless nodes in order to achieve and maintain a phase-consistent state in a distributed antenna array. The relative stability of the local VCO at each node is important for distributed phase consistency. For all nodes to operate on the same reference frequency and provide a consistent state, a reference frequency needs to be set. To enable distributed beamforming, the reference frequency must be given wirelessly, usually via a phase-locking loop (PLL) on a secondary node. Due to the limited bandwidth of wireless networks used for frequency allocation in large arrays, VCO locks and drifts in frequency between updates, requiring sporadic link refreshes. Consequently, the overall performance with respect to update time is impacted by the VCO's stability. Phase noise and update interval effects on distributed beamforming performance are discussed, and the PLL and reference VCO sources of phase noise are investigated. A parametric comparison of their influence on beamforming performance is provided by analyzing the beamforming performance in two specific scenarios employing nominal high stability and poor stability VCOs. Additionally, a framework for evaluating distributed beamforming performance in terms of VCO and PLL parameters is offered. The practical effects of VCO in PLL applications in communication systems are thoroughly examined in this work, which also emphasizes the significance of VCO and PLL parameters in distributed beamforming.

Applications based on phase-locked loops (PLLs) are essential parts of every communication system-on-a-chip (SoC). A high-speed PLL with LC-VCO is described by S. ophiya Suan et al. in 180 nm CMOS technology [20]. In Figure 5, the suggested PLL structure is displayed.

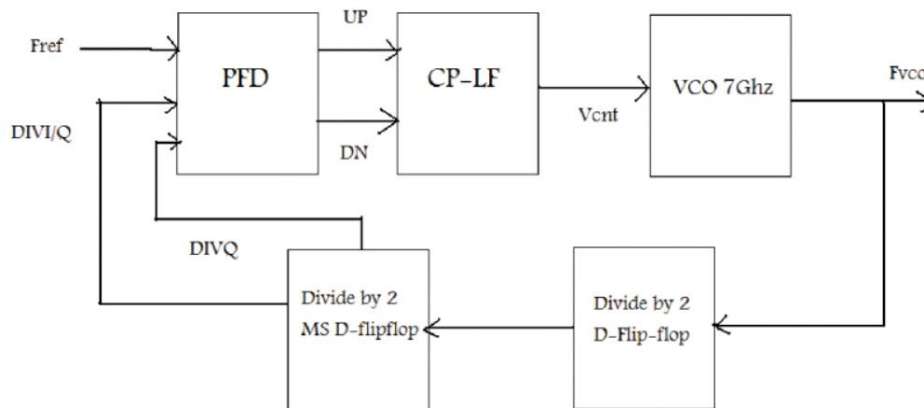


Fig. 5 Block schematic of the suggested PLL [20].

Its goal is to maintain linear VCO gain while achieving a larger tuning range and reduced phase noise. The Spectre emulator and the Cadence Virtuoso tool were used to create the PLL. The PLL's sub-modules were initially designed using the schematic editor and the specifications were checked for accuracy. A high-speed PLL was subsequently created by combining these sub-modules. With a phase margin of 60 degrees and a band width of 100 kHz, the PLL under consideration is a second-order system. To ensure linearity and a 6.7 GHz to 7.5 GHz bandwidth, the LC VCO is designed to operate at 1.8 volts of power. The locking range is 0.454 GHz, and the capture range is 0.807 GHz. With its resonance frequency of 7GHz, output power of 2.25mw, gain of 484 Mhz/V, and phase noise of -131.5dbc/Hz at 10Mhz, the projected LC VCO is very outstanding. This work is an essential resource for designing and optimizing VCO in PLL-assisted communication systems.

6. Summary

In this comprehensive exploration of Voltage-Controlled Oscillators (VCOs), the research has provided valuable insights into their diverse designs, applications, and significance in modern communication systems. The study commenced with an in-depth analysis and comparison of classic VCO types, including the Colpitts and Clapp VCOs, to the more contemporary CMOS VCOs. This

comparison highlighted the evolution of VCO design techniques, emphasizing their varying capabilities in terms of frequency stability, phase noise, and tuning range.

Moving forward, the research delved into the specific design strategies employed in enhancing VCO performance. The discussion on high-performance VCO designs elucidated the importance of metrics such as phase noise and tuning range, crucial for applications demanding precision and efficiency. Case studies presented further underscored the versatility of VCOs, showcasing their applications in aerospace systems and communication technologies.

The exploration of VCOs within Phase-Locked Loops (PLLs) provided a deeper understanding of their role in signal generation, frequency synthesis, and system stability. The research highlighted the interplay between VCOs and PLLs, emphasizing their symbiotic relationship in achieving accurate frequency control and modulation/demodulation processes.

As the technological landscape continues to evolve, the quest for high-performance VCOs persists. Engineers and researchers are driven by the need for lower phase noise, wider tuning ranges, and efficient power consumption. This study serves as a foundation for further advancements in VCO design, offering a roadmap for optimizing communication systems' efficiency and functionality.

In conclusion, the research has shed light on the intricate world of VCOs, from their historical foundations to their modern applications. It provides a comprehensive understanding of the design techniques, performance metrics, and practical implications of VCOs in communication technologies. This study aims to inspire continued innovation in VCO design, paving the way for enhanced efficiency and performance in modern communication systems.

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