A Comprehensive Analysis on CMOS Comparators: Principles, Design Optimizations, and Applications

Zixi Zeng

School of Data Science, Chinese University of Hong Kong, Shen Zhen, 518172, China

121090023@link.cuhk.edu.cn

Abstract. The paper aims to systematically review the basic principles, structure, and optimal design of Complementary Metal Oxide Semiconductor (CMOS) comparators, discussing their specific applications in various fields and their future development trends. CMOS comparators are crucial in signal processing and data conversion due to their low power consumption and high integration capability. The paper begins with an introduction to the basic principles and technical analysis of CMOS comparators, providing a foundation for understanding their operations. It then explores the detailed structure and optimization design of both traditional and new CMOS comparators, highlighting advancements in speed and power efficiency. The paper concludes with an analysis of performance optimization techniques, including device parameter adjustments and deep learning-based optimizations, and discusses the integration and packaging trends that will shape the future of CMOS comparators. This comprehensive review of CMOS comparators summarizes current knowledge and advancements, making it a valuable resource for researchers and engineers. It highlights key developments in speed, power efficiency, and integration, and discusses future trends and optimization techniques. This work contributes to the continued innovation of electronic systems, enhances signal processing capabilities and guides future research directions.

Keywords: CMOS comparators, power efficiency, speed, optimization technique.

1. Introduction

In modern electronics industry, complementary metal-oxide-semiconductor (CMOS) technology has become the corn technique in integrated circuit design and manufacturing, which using complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions [1]. First invented in 1960s, CMOS technology has experienced rapid development, from the initial simple circuit to today's high-performance, processors and complex system-on-chip (SoC), and its application in various electronic field sis everywhere. Due to its low power consumption, high-density and high performance, CMOS technology is widely, used in the field of computer, communication, consumer electronics, and promotes the process of information technology and digitalization. CMOS comparators are a fundamental component within this technology, crucial for tasks that require precise voltage comparison, such as signal processing and data conversions. The continuous demand for higher speeds, higher precision and lower power consumption in electronic devices has stimulated extensive research and development in CMOS comparator design and optimization.

This paper provides a comprehensive review of CMOS comparators, covering their basic principles, structural designs, optimization techniques, and applications. It begins with an exploration of CMOS technology fundamentals, followed by a detailed examination of traditional and modern CMOS comparator designs, highlighting advancements in speed and power efficiency. Optimization strategies such as device parameter adjustments and the use of deep learning are discussed to show how performance improvements are achieved. Practical applications in fields like analog-to-digital converters (ADCs) and power management systems are examined, demonstrating the critical role of CMOS comparators in enhancing system performance and reliability. Future trends in integration and packaging such as SoC designs and 3D packaging techniques, are also analyzed to point out further advancements in CMOS comparator technology.

In summary, this review offers an in-depth look at CMOS comparators, from basic principles to advanced applications, highlighting the continuous innovation needed to meet the demands of modern electronic systems and enhance their capabilities.

2. Basic Principle of CMOS Comparator

2.1. CMOS technology analysis

CMOS technology is remarkable for its low power consumption high noise immunity and scalability, and has played a dominant role in manufacturing technique in digital integrated circuits. According to CMOS technology, digital logic circuits are constructed using pairs of complementary MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) – NMOS(n-type) and PMOS(p-type) working together to minimize power consumptions while maintaining high performance. The PMOS and N-MOS structures is shown in Figure 1.

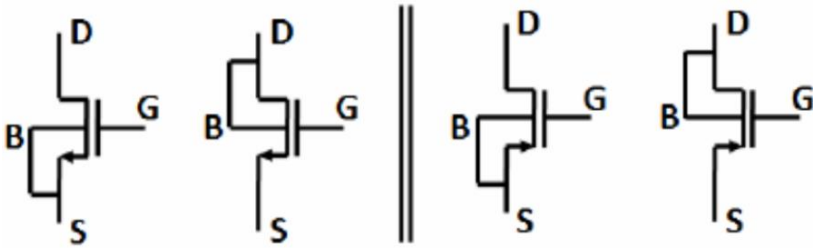


Figure 1. PMOS and NMOS

The CMOS process foster the progress of intricate logic functions on a single chip, along with facilitating the development of sophisticated electronic systems. CMOS enables the creation of numerous powerful analog and digital circuit configurations. Unlike BJT logic devices, which are switched by current, CMOS devices are switched by voltage, with no current flowing into the gate of a CMOS transistor [2]. Furthermore, CMOS technology portends a new era of integration by enabling the combination of analog and digital circuits on a unified platform.

Another key advantage of CMOS technology is scalability, this powerful characteristic allows the integration of millions of transistors on a single chip. The scalability has driven continuous advances in semiconductor technology, resulting in increasingly more delicate and more powerful electronic devices.

Thanks to the advantages of low power consumption, high integration density and compatibility with digital brought by CMOS, CMOS mixed-signal circuits that combine analog and digital components are used in many applications such as wireless communication, audio processing and power management. The multifunctionality and high-efficiency make CMOS technology an irreplaceable part in the development of advanced electronic system. From the smallest wearable devices to the largest super computer, every step of CMOS improvement may bring new possibilities in electronic field.

2.2. Basic principle of CMOS comparator

The fundamental principle underlying the operation of a CMOS comparator, which is an essential component innumerous analog and digital systems, lies in that it can compare to analog input voltages and generate a digital output based on the result of the comparison. A comparator is the basic component mainly used in analog-to -digital converters. Ideally, it generates an output logic as an instant response to the sign of an analog input, but in reality, which is almost impossible [3].

With the development of CMOS comparators, digit analog field has been through a huge revolution. Device with comparators play a vital role in various analog and mixed-signal applications such as sensor interfaces and signal processing circuits. During the working time of comparators compare the inputs, they signify which input voltage is greater. The operation of a CMOS comparator relies on the principles of differential amplification and threshold detection, which are inherent to it intrinsic design.

In typical CMOS comparator, the input stage consists of a pair of different input transistors, one NMOS and one PMOS, connected to the input voltages. To make sure they can be compared properly, these transistors are used to amplify and buffer the input signals. The output correspond to the input

voltage is then fed to a latch or flip-flop, determining the output state based on the magnitudes of the input voltages. If one input voltage is higher than the other, the output will be determined as a logic high; if the opposite is true, the output will be driven to a logic low.

3. Structure and Optimal Design of CMOS Comparator

3.1. Traditional CMOS Comparator Structure

Other than its ancestor's structure, CMOS comparators use many advanced techniques to improve its performance. In TTL technology, the comparator usually consists of transistors that are configured as different pairs to perform voltage comparison operations, while in diode technology, the comparators usually were made by a diode to switch the output by comparing the input voltage. These early comparators did well in their time, but still some limitations on power consumption and performance in today's view.

With the development of CMOS technology, CMOS comparators become a better choice with better flexibility, high-efficiency and low power consuming. The precise structure help CMOS comparators combine low-power consumption and good performance. The first is the input stage, which is the starting point of the comparator and is used to receive the analog input voltage. The input stage usually includes a pair of differential input transistors, namely an N-type metal oxide semiconductor (NMOS) transistor and a P-type metal oxide semiconductor (PMOS) transistor. The role of these transistors is to amplify and regulate the input signal to ensure that the subsequent comparison process can be carried out accurately. Right after the input stage is a series of amplification and feedback circuits, which are designed to improve the sensitivity and dynamic range of comparators to identify the voltage changed accurately. At last, the output stage of the comparator with transfer the result into the digital output signal using a latch or a flip-flop to prove a stable and reliable representations of the numbers.

3.2. New Types of CMOS Comparator

In our daily life, CMOS comparators are used in almost all electronic devices. In mobile communication devices such as smart phones or tablet PC, CMOS comparators are used to monitor battery voltage and realize management of battery status. They may also use to realize circuit protection in consumer electronics or ECU systems, ABS systems in automobile electronic systems. However, according to Ryckaert' respond, for many years people have made more and more complex system-on-chips (SoCs), for instance CPUs and GPUs, leading to more and more operations have been integrated onto the same silicon die [4]. These innovative operations improve the efficiency for moving data on a single silicon die is much faster than moving from chip to chip in a computer. Fror many years, CMOS transistors and interconnects work better with the help of scaling down. However, in recent days, simply scaling the device and the interconnect start to be difficult to build the whole SoC and make all of it better. For example, SRAM [the system's cache memory] no longer scale well as Moore's Law define in logic. To improve the performance of CMOS comparators, new design needs to be approached.

To better make CMOS comparators fit modern requirements, a significant way is to design a new comparator structure that can speed up the circuit's working time. Research group in Shanghai has developed a new high-speed, low-power self-biased comparator [5]. Based on the MIPI D-PHY physical layer transmission protocol, the research group designed the new structure of comparator with composed of two stages of op-amps: the common gate, the common source and the NMOS transistor working in the linear region form the first-stage amplification, and the op-amp with the current source as the load forms the second-stage amplification structure. Through the analysis of the small signal model of the circuit structure and the post-simulation verification, the results show that the high-speed comparator can realize the accurate reception of the low common mode electric frequency differential signal. According to Yeghiayan, in analog-to-digital conversion, where analog inputs are compared to set references, high-speed comparison is essential, and latched comparators

are the preferred blocks for achieving this high-speed performance [6]. The research group develop a 45nm CMOS high-speed latched comparator suitable for several applications including high-speed data conversion. Their two-stage dynamic latched comparator focus on reality usage and record the behavior of the comparator across different corner to guarantee the stability under different circumstances, which is different from other standard comparators. The new design strikes a beautiful balance among input clock frequency, delay, average power consumption and effective area. Ghasemi presented a new structure of two-stage comparator to realize the high-speed and high-precision [7]. The offered comparator reduces the delay time by employing the positive feedback in the first stage. What's more, the comparison speed is enhanced from the NMOS transistor used between the differential output node. Moreover, the speed and accuracy are improved from the activation of the preset delay.

In the optimal design of CMOS comparator, another important consideration is reducing the low-power consumption. In Kumari's research, FINFET technology is used to develop a two-stage and three-stage dynamic comparator architecture for highspeed, low power dissipation [8]. In their design, the comparator was designed with tail or no tail transistors with HSPICE, FINFET technologies. According to their designs, it is found that compared to 20nm technology, FINFET technology has lower power consumption than CMOS technology. As the power supply voltage increases, the operating speed also increases, making these two-stage and three-stage comparators very useful in ADC-based wireless communication applications for high-speed transmission. After their analysis and tuning, this design is more efficient for successive approximation register (SAR) ADC types. The design can be used for biomedical applications. Being used in many applications such as sensors and flash ADCs, traditional CMOS current comparators measure current from the input current signal and convert it to output voltage by differential input current or by comparison of the input current with a threshold level. Badel's research group has shown that the proposed current converter offers the lowest propagation delay and the lowest power consumption for the input current [9]. The impressive achievement was made by the utilization of Wilson current mirror circuitry at the input stage of the proposed comparator. By modifying a fundamental architecture of the current mirror circuity in the comparator, the research group designed an improved CMOS current comparator which is suitable in wireless communication and portable computers to fulfill requirements of ADC applications.

4. Application of CMOS Comparator

4.1. CMOS Comparator and Battery Power Detection

In modern portable electronic devices, battery power detection is a vital function that nobody can ignore. In these devices CMOS comparators play a key role in battery management systems by monitoring the voltage level of the batteries to ensure the usage of the device.

In most cases, a CMOS comparator is connected between the battery and the system control circuit to compares the current battery voltage with a preset reference voltage. The preset reference voltage is used as the threshold bar for the comparator to determine the current state. When the battery voltage falls below a certain threshold, the CMOS comparator will immediately output a signal warning that the battery is low. The system will then send the message to the user in pre-determined way.

Certain advantages contribute to the widely usage of CMOS comparators in battery power detection. Firstly, when the transistors in the circuits are at rest, there will be no current passes through the circuit, so the power consumption of CMOS comparator is very low. The low energy consumption makes CMOS comparator suitable to the battery powered devices. Secondly, through the accurate voltage comparison, the battery level can be reliably monitored to avoid sudden shutdown of the device due to low power. In the era that electronic products are so widely used, this high precision property makes CMOS comparators almost irreplaceable. Thirdly, CMOS comparators can be integrated in a power management IC (PMIC), reducing external components and simplifying circuit design. The high-integrity makes CMOS comparators an ideal choice in circuit designing.

CMOS comparators are used in many electronic devices in our daily life. For example, the battery management unit (BMU) in a smart phone uses a CMOS comparator to monitor the battery voltage, ensuring that the user is announced when the battery is low. What's more, in some wearable devices such as smartwatches and fitness trackers, CMOS comparators help these devices achieve longer battery life if users require efficient battery management.

4.2. CMOS Comparator and Sensor Interface

In some circumstances where analog signals need to be converted to digital signals, CMOS comparators are widely used in these sensor interface circuits. Many sensors output analog signals that need to be read and processes by a processor or digital system. The outputted analog signal is then fed into a CMOS comparator, which compares the signal with a reference signal. When the sensor output exceeds the reference voltage, the comparator then outputs a high-level signal; otherwise, a low-level signal is then be outputted. Using the CMOS comparator, the analog signal can be transferred to the digital signal that can be read by the processor or controller for further processing and decision making.

CMOS comparator has many advantages in sensor interface, which make it widely used in modern electronic systems. To begin with, CMOS comparators perform well under different environment conditions, including wide temperature ranges and power supply voltages fluctuations, which makes it suitable for various situations such as industrial environments and outdoor applications. Because of its CMOS technique, CMOS comparator has a long using age, making it a suitable choice in a sensor system that operates stably for a long time. Besides, thanks to CMOS technology, it allows the comparator to be integrated with other signal processing components on the same chip. Many useful components, for example analog-to-digital converters (ADCs) and filters, can be integrated with CMOS comparators to build a complete signal processing chain. The high integrity improves both system reliability and performance with reducing cost and space. Last but not least, CMOS comparators can quickly respond to changes in input signals. These days, many sensor applications require real-time data processing, real-time comparison is indispensable in modern systems such as industrial automation and vehicle control systems. The fast-switching capability of CMOS comparator allows the reliability in these applications.

5. Performance Optimization and New Trends

5.1. Device Parameter Optimization Technology

To optimize the performance of CMOS comparator, the first need is to start from the device parameters, and improve the overall performance by adjustment and optimization of key components. So far, researchers have found plenty of ways to enhance the performance, such as threshold voltage optimization to reduce the input offset voltage of the comparator to improve precision, output driving capability optimization by increasing the size of output stage or adding output buffers to meet higher load demands Zhuang introduces a three-stage comparator and its modified version to enhance speed and reduce noise [10]. Unlike traditional two-stage comparators, the new three-stage comparator includes an additional amplification stage to increase voltage gain and speed. Furthermore, the revised version uses a CMOS input pair to minimize kickback noise and incorporates an extra path in the regeneration stage.

5.2. CMOS Comparator Optimization Based on Deep Learning

Along with the development of artificial intelligence and deep learning technologies, optimizing CMOS comparators using deep learning has been a popular topic in the world. The optimization combines both neural networks and machine learning algorithms to optimize comparators based on the analysis made by computers. The use of deep learning can accelerate the circuit simulation process and improve the design efficiency. Online tuning can also be done by continuous learning and optimization to enhance the performance and reliability of the CMOS comparator.

5.3. Integration and Packaging Trends of CMOS Comparators

As technologies progresses, the integration and packaging technologies of CMOS comparators are also evolving. High integration SoC (System-on-chip) design, advanced packaging technologies and high reliability and durability packaging are the major directions. High integration SoC design integrates comparators with other analog and digital function modules such as ADCSs, DACs to dorm the full-functional processing unit. 3D packaging is also used to stack multiple chips together, reducing packaging area and enhancing performance and integration.

The optimization of CMOS comparators includes device parameter optimization technology, CMOS comparator optimization based on deep learning and integration and packaging trends of CMOS comparators. These optimizations and trends not only improve the devices' performance and reliability, but also expand their application fields, provides a more powerful signal processing capability for modern electronic systems.

6. Conclusion

In the paper, the basic principle, structural optimization design and application of CMOS comparator are systematically reviewed in order to provide a comprehensive reference for researchers and engineers. Through the detailed analysis of CMOS technology and the working principle of the comparator, we understand the importance of CMOS comparator in modern electronic systems and its performance influencing factors.

To optimize the performance of CMOS comparators, it is intuitive to start with device parameters, adjusting and optimizing key components. Researchers have developed various methods such as threshold voltage optimization to enhance performance by reducing input offset voltage to improve precision. The development of artificial intelligence and deep learning technologies has also introduced new optimization approaches. By combining neural networks and machine learning algorithms, deep learning accelerates the circuit simulation process and improves design efficiency through continuous learning and online tuning. Last but not least, advancements in integration and packaging technologies, such as high integration SoC (System-on-chip) design and 3D packaging, further foster performance and reliability. These developments integrate comparators with other analog and digital function modules, reduce packaging area, and expand application fields, providing more powerful performance for modern electronic systems.

References

[1] Echo. What is CMOS Memory. WickedSago, 2011. http://wickedsago.blogspot.com/2011/04/what-is-cmos-memory.html.

[2] Mari, L. An introduction to CMOS Technology. Technical Articles, 2021. https://eepower.com/technical-articles/an-introduction-to-cmos-technology/.

[3] Sangeetha R, Vidhyashri A, Reena M, et al. An overview of dynamic cmos comparators. 2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS). IEEE, 2019: 1001-1004.

[4] Ryckaert J, Samavedam S B. The CMOS 2.0 revolution [J]. Nature Reviews Electrical Engineering, 2024: 1-2.

[5] Zhang Xinyao, Huang Zunkai, Wang Hui, Tian Li, Wang Ning, Feng Songlin. A high-speed comparator based on MIPI D-PHY physical layer. Journal of Hefei University of Technology (Natural Science Edition), 2022.

[6] Yeghiayan, R., Salameh, E., Mokdad, M. E., Atallah, J. 45nm CMOS Two-Stage Latched Comparator. 2022 International Conference on Smart Systems and Power Management (IC2SPM). IEEE, 2022: 164-169.

[7] Ghasemi R, Ghasemian H, Abiri E, et al. Design and Analysis of a Low-Power Two-Stage Dynamic Comparator with 40ps Delay in 65nm CMOS Technology. 2021 29th Iranian Conference on Electrical Engineering (ICEE). IEEE, 2021: 159-164.

[8] Kumari K L V R, Sree L P, Raji P. Design of Dynamic comparator using CMOS and FINFET technologies. 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT). IEEE, 2023: 1-6.

[9] Badal M T I, Mashuri M B, Reaz M B I, et al. Low power high-speed current comparator using 130nm CMOS technology. 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES). IEEE, 2016: 72-76.

[10] Zhuang H, Cao W, Peng X, et al. A three-stage comparator and its modified version with fast speed and low kickback. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29 (7): 1485-1489.