Gan Vertical Power Finfets Using BN As Gate Dielectric

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Abstract. Over the past few decades, the semiconductor industry has undergone rapid advancements and transformative evolution, particularly in semiconductor materials. Wide bandgap (WBG) semiconductors, represented by gallium nitride (GaN) and silicon carbide (SiC), offer significant advantages over traditional silicon-based technologies. This research explores the suitability of BN as a dielectric material in GaN vertical power FinFETs, specifically targeting high-temperature applications. BN thin films are directly deposited by microwave-plasma-assisted chemical vapor deposition (CVD). The presence of BN is confirmed by X-ray photoelectron spectroscopy (XPS). GaN/BN vertical FinFETs are demonstrated for the first time with a current on-off ratio of 10. The high-resolution transmission electron microscopy (HRTEM) reveals the presence of BN on GaN non-polar sidewalls. BN metal-insulator-semiconductor (MIS) gate diode demonstrates increased breakdown voltage compared to GaN Schottky gate diode. Hydrogen plasma has been pinpointed as the main culprit behind variations in dielectric film thickness and the deterioration of crystal quality, both of which contribute to increased gate leakage current. Through the optimization of deposition conditions, the enhanced device demonstrates outstanding performance and maintains stable operation at temperatures up to 573K. This study provides a valuable foundation for future research on BN-based gate dielectrics in GaN vertical transistors.

Keywords: boron nitride, GaN, vertical FinFETs, high-temperature, chemical vapor deposition.

1. Introduction

GaN devices hold great potential for next-generation power electronics. Lateral power devices, based on AlGaN/GaN HEMT structures, have demonstrated outstanding performance and have been successfully commercialized for decades [1-3]. However, vertical GaN transistors offer several key advantages over their counterparts. These advantages include higher breakdown voltage, increased current power density, easier scalability and more convenient thermal management [4-6]. GaN vertical FinFETs, as a newly emerging structure in recent years, have garnered widespread attention due to their low epitaxial cost and excellent performance [7-9]. The ongoing reduction in device dimensions, coupled with the relentless rise in power density, elevates the operating temperature in the active region, posing a significant challenge to the stability of GaN vertical FinFETs. Experimentally, there are still very few reports on the device performance under high-temperature. The study on temperature stability and temperature-dependent breakdown on these devices is insufficient. This necessitates the investigation of improved device designs, particularly of which is the sidewall gate stack that makes the high-temperature-robust dielectric materials essential.

Recently, boron nitride (BN), an ultra-wide bandgap (UWBG) material has garnered significant research attention for its potential in high-power and high-temperature applications [10, 11]. Boron nitride (BN) exhibits various crystal phases, among which hexagonal boron nitride (h-BN)—a layered two-dimensional (2D) material with a lattice structure akin to graphite—has demonstrated exceptional potential for thermal management in power electronics. h-BN possesses a wide electronic bandgap, a high breakdown electric field, and an atomically smooth surface that is free of dangling bonds and charge traps, making it an excellent candidate as a promising non-oxide thin film dielectric [12]. Additionally, h-BN demonstrates exceptional thermal stability, enduring temperatures up to $1000℃$ in air [11]. It also features a significant in-plane thermal conductivity of $420W/(m \cdot K)$, along with a high degree of thermal conductivity anisotropy [13]. These attributes make h-BN highly promising for high-temperature applications in nanoelectronics.

In practice, integration of BN into GaN devices remains challenging from a material perspective. Exfoliating h-BN from bulk crystals is not a viable approach for scalable production, as it suffers from low repeatability, poor yield, lack of control over sample thickness, and limited area coverage. Therefore, some recent work explored the direct deposition of BN by various physical or chemical means. Yang et al. demonstrated AlGaN/GaN MISHEMTs with improved gate performance using BN deposited by chemical vapor deposition [12]. Abhijit et al. demonstrated BN/GaN metal-insulator-semiconductor Schottky barrier diodes (MIS SBDs) with improved breakdown voltages by pulsed-laser deposition [14]. Nevertheless, to the best of the author's knowledge, there has been no successful demonstration of seamless integration of BN onto non-planar GaN devices.

In this study, an innovative concept of GaN/BN vertical power FinFETs is introduced, designed to investigate the potential of BN in GaN vertical power transistors for high-temperature applications. The key challenges involve developing a nanofabrication strategy compatible with BN, achieving high-quality and conformal deposition of BN on GaN substrates, and the optimization of vertical sidewall gate stack.

2. Device Fabrication and Material Deposition

2.1. Fabrication Process

The device was fabricated on a GaN substrate, consisting of 20μm unintentionally doped n^-drift layer which refer to Fig.1. Before the start of fabrication process, the wafer underwent a standard cleaning procedure, using acetone, isopropyl alcohol, ultraviolet ozone, buffered HF solution and deionized water in sequence.

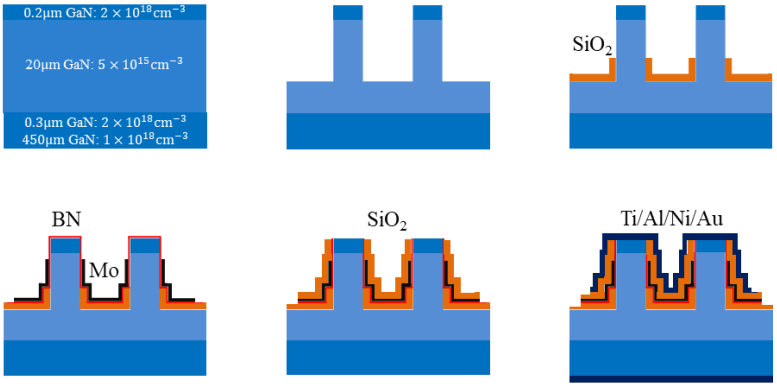


Fig. 1 Schematic of the Ga vertical FinFETs and the structures of epitaxial wafer

The fins were patterned using electron-beam lithography (EBL) with a fin-width of 200-300nm and a total number of 10-50. A bi-layer e-beam resist comprised of PMMA 950K and PMMA 495K was spin-coated for EBL to achieve a slightly undercut profile after development. After development, a short oxygen plasma was stricken to remove any organic residue to enhance the adhesion for following metal deposition. Subsequently, fin bodies were dry-etched using Cl_2/N_2 -based inductively coupled plasma-reactive ion etching (ICP-RIE), masked by Ni, aiming for the height of ~1.2μm, followed by tetramethylammonium hydroxide (TMAH) treatment to reduce the etching damage on the sidewalls [15]. The photoresist (PR)-assisted planarization technique and timed-etch technique were employed for formation of the different layers on the fin [7]. The gate stack comprises a thin layer of BN and a sputtered 125-nm Molybdenum (Mo) layer. The gate electrode is formed by $Cl_2/N_2/O_2$-based RIE. BN on the is etched together with SiO_2 spacer using CF_4/Ar-based RIE. Finally, a lift-off process was employed for sputtered Ti/Al/Ni/Au (20/120/40/100nm) source contact formation on the frontside and the backside for the drain contact. Figure 2.1 depicts the fabrication process flow and provides schematic cross-sectional illustrations of the key steps involved in the fabrication.

2.2. Material Deposition and Characterization

Boron nitride film deposition was carried out using microwave-plasma-assisted chemical vapor deposition (MPCVD) with ammonia borane as the precursor. Throughout the deposition process, a continuous flow of 20 sccm H_2 and 120 sccm N_2 gases was maintained to stabilize the pressure at approximately 1 Torr. Once the GaN substrate reached the set temperature, the microwave plasma was ignited and held at an output power of 1 kW. After 15 minutes of growth, the microwave was turned off, allowing the GaN substrate to cool naturally.

Post-deposition, surface analysis was performed using X-ray photoelectron spectroscopy (XPS) to acquire detailed chemical information near the surface. The survey scan, shown in Fig. 2(a), confirmed the presence of B and N, along with Ga peaks from the substrate. High-resolution XPS spectra, presented in Fig. 2(b) and (c), revealed binding energies of 190.5 eV for B 1s and 398.1 eV for N 1s, indicating the presence of sp2-bonded B and N in the films. An additional peak around 395.2 eV in the N 1s spectra was attributed to the GaN substrate. The B/N atomic ratio was calculated to be 1:1.3.

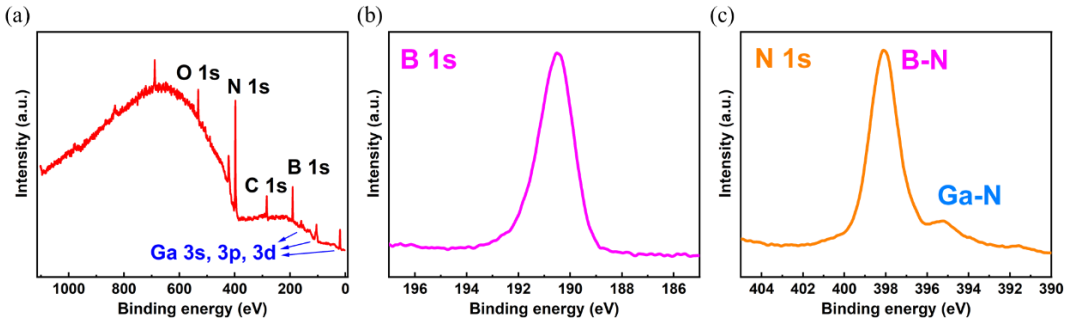


Fig. 2 XPS spectra of BN films grown on planar GaN substrates.

3. Results and Discussion

GaN/BN vertical FinFETs were demonstrated in this work for the first time. The cross-section images and EDX data of fabricated devices are presented in Fig. 3(a) and 3(b). The TEM image in Fig. 3(c) confirms the presence of ~7nm BN in sidewall GaN gate stack.

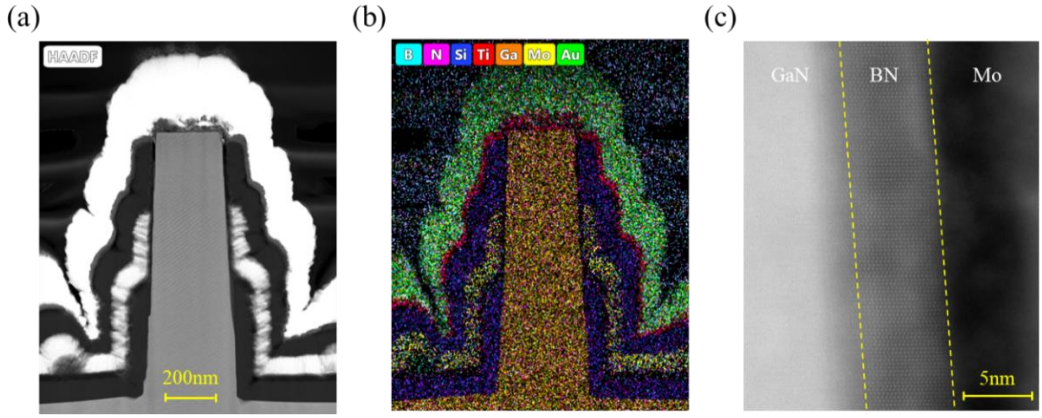


Fig. 3 (a) Cross-section SEM images, (b) EDS data of GaN/BN vertical FinFETs and (c) TEM images of sidewall MIS-structure.

The device transfer characteristics are demonstrated in Fig. 4(a). From the measurement, the device shows an on-off ratio of about 10. High voltage resistance is an important index to evaluate the device and dielectric layer. The breakdown measurement was carried out on a metal-insulator-semiconductor (MIS) structure with BN and compared with GaN vertical Schottky barrier diode (SBD) to examine the current blocking capability of the gate dielectric. The MIS structure was

fabricated on the sample wafer same as the transistors after removing the n+ cap layer but without the source electrode on the top.

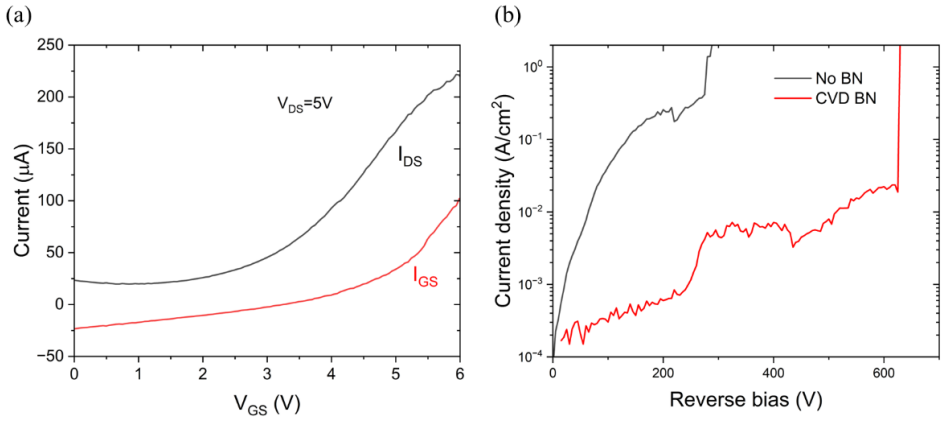


Fig. 4 (a) Transfer Characteristics of GaN/BN vertical FinFETs, (b) Reverse characteristic of gate diode with and without the insertion of BN

Fig. 4(b) shows the reverse current density–voltage (J-V) characteristics of two configurations. The hard breakdown voltage is 610V for BN MIS gate, compared to 245V for Schottky gate, indicating approximately 140% improvement with the insertion of BN. The device after breakdown shows no obvious change that is visible by optical microscope, indicating that the breakdown takes place at the fin-region instead of gate pad edge.

4. Challenge and Optimization

4.1. Gate leakage current

Gate leakage current suggests that GaN-BN-Mo gate junction needs to be studied. The junction barrier height accounts for the increased leakage current. Forward J-V characteristics of BN MIS diode were measured as illustrated in Fig. 5.

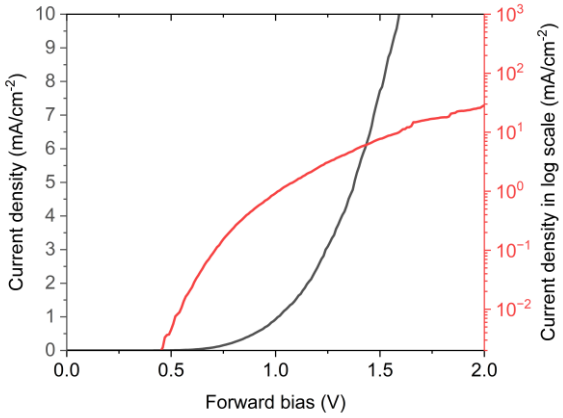


Fig. 5 Forward current density-voltage characteristics of BN MIS diode

The mechanism governing forward current transport can be elucidated using thermionic emission theory. The current density of a MIS Schottky diode is described by the following equation [16].

$$I_{TE} = I_{s0} \exp\left[\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right]$$

$$I_{s0} = A^* T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \quad (1)$$

Where n is the ideality factor, R_s is the series resistance and A^* is the effective Richardson constant. The extracted barrier height is ~0.77 eV using the method in [17]. Previous studies have determined the Schottky barrier height of the Mo-GaN junction to be 0.81 eV [18]. The insertion of BN at the metal-GaN interface decreases barrier height. Similar results were also observed in Ni/Au-BN-GaN MIS diode [14]. The lowered barrier height can be explained by the surface Fermi level pinning effect as a result of surface trap states. This prevents electrons from being effectively confined in the MOS surface channel, leading to gate leakage. The large ideality factor may be attributed to the crystal quality of the BN thin film and the presence of interfacial trap states introduced by the etching process.

The dielectric layer is also a significant factor leading to gate leakage. The inconsistency in the thickness and the inhomogeneous phase of the BN thin film results in the leakage path across the gate diode, which is thought to be due to the suboptimal deposition conditions. Due to the relatively large lattice mismatch of h-BN or c-BN to GaN, the BN thin film tends to be amorphous and exhibits leakage paths that contribute to increased gate current, making controlling capability of the sidewall gate stack falling short of theoretical expectations. Additionally, experiments have revealed that ammonia borane-based chemical vapor deposition can erode underlying GaN substrate structures. SEM images in Fig. 6(a) show that when plasma is ignited with only the carrier gas, i.e. H_2, the GaN sidewalls are significantly damaged. This is due to the existence of hydrogen plasma, which is inevitably introduced into the environment during growth, etching the GaN. Under typical deposition conditions, hydrogen plasma primarily originates from the carrier gas and the precursor. Therefore, when BN deposition and GaN fin-structure etching occur simultaneously, the stability of the substrate surface is compromised. This makes nucleation on the GaN fin-structures difficult, resulting in reduced film adhesion and decreased material quality. Moreover, this negative effect is found to be more pronounced on the GaN fin-structure [$1\bar{1}00$] crystal planes than planar [0001] surface.

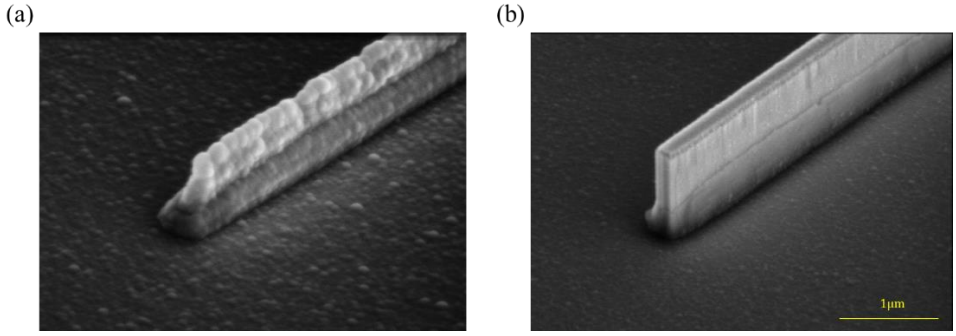


Fig. 6 GaN fin-structure after 25mins under (a) hydrogen plasma and (b) BN deposition condition with reduced temperature

4.2. Device Optimization

To tackle the deposition challenge, one effective strategy is to reduce the growth temperature. In this investigation, the growth temperature was lowered from 400°C to 300°C. Additionally, a ~12 nm thick Al_2O_3 was deposited by atomic layer deposition (ALD) before the deposition of BN, acting as a buffer layer. This buffer layer enhances the adhesion and reduces the surface damage of the substrate. Fig. 6 presents the SEM image of the optimized structure. Based on this new approach, a device was fabricated consisting of thirty 120-μm-long fins with a 300 nm fin width. The transfer characteristics and output curves are illustrated in Fig. 7(a) and Fig. 7(b), respectively.

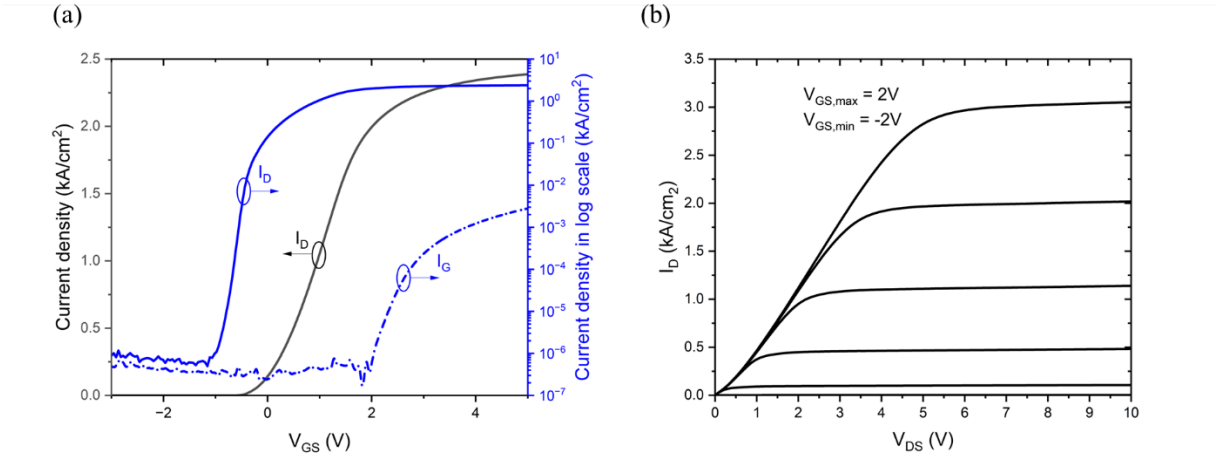


Fig. 7 (a)Transfer and (b)output characteristics of GaN vertical FinFETs using BN/Al_2O_3 bilayer dielectric.

The device exhibits an on-off ratio (I_{on}/I_{off}) up to 10^6 and a current density over $3kA/cm^2$, normalized to the active fin area. Gate current is effectively suppressed due to the improvement of dielectric layer. The threshold voltage, linearly extrapolated from the transfer curve, is approximately 0.5V. The experimental value of V_{th} is lower than that calculated from the work function of metal and GaN, indicating the presence of positive oxide charges at the interface or inside the BN/Al_2O_3 layer. The equivalent oxide charge density (Q_{ox}) can be estimated from the following equations [4].

$$V_{th} \approx V_{bi} - \frac{Q_{ox}}{C_{OX}} - \frac{qN_D W^2}{8\epsilon_{GaN}}$$

$$V_{bi} = \frac{1}{e}\left[\phi_M - \chi_{GaN} - kT\ln\left(\frac{N_C}{N_D}\right)\right] \quad (2)$$

An oxide charge density of $\sim 2 \times 10^{12} cm^{-2}$ was derived from the equation accounting for the reduced V_{th}. This positive charge was also reported in other works [4, 8, 19]. Furthermore, V_{th} can be shifted more positively by increasing the gate oxide capacitance, reducing the net donor concentration in the drift region or scaling down the channel width. The subthreshold swing reflects the switching performance of transistor and can be mathematically expressed by [20]:

$$SS = \frac{dV_G}{d(\log I_D)} = \ln(10)\frac{kT}{q}\left[1 + \frac{(C_d + C_{it})}{C_{ox}}\right] = 60\frac{mV}{dec}\cdot\eta \quad (3)$$

The result obtained from the device transfer characteristic is ~260mV/dec with $\eta = 4.3$, suggesting a large interface traps density and a small oxide capacitance due to the low dielectric constant nature of BN. The electron mobility in the channel is estimated to be ~ 23 $cm^2V^{-1}s^{-1}$ extracted from the linear regime of the transfer curve.

Temperature-dependent measurements were then performed to further characterize the electrical properties of GaN vertical FinFETs. The temperatures were measured from 298K to 573K with steps of 25K as shown in Fig.8. The device exhibits the highest operating temperature reported to date at 573K with a threshold voltage dispersion of ~1.5V. The off-state current increases by 1 order as temperature rises, indicating the degradation of double-layer dielectric at increased temperature. The reason for the variation in threshold voltage and off-state current can be ascribed to the occupancy of trapping states and effective carrier concentrations which in turn depend on the temperature.

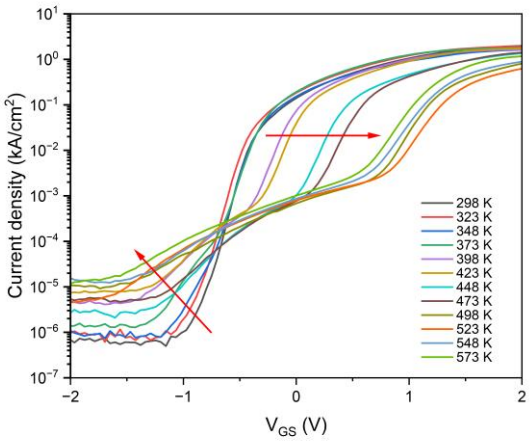


Fig. 8 Temperature-dependent transfer characteristics of GaN vertical FinFETs in semi-log scale

5. Conclusion

This work investigates GaN vertical power FinFETs using BN as the gate dielectric. BN thin films were directly grown on the GaN substrate via CVD method, as confirmed by structural characterization. The GaN/BN vertical FinFETs were demonstrated for the first time, showing an on-off ratio of approximately 10. The incorporation of BN significantly increased the device's breakdown voltage, while simultaneously leading to higher gate leakage. By optimizing the deposition conditions, the Al_2O_3/BN double-layer gate stack effectively reduced the gate leakage while significantly enhancing the device's operating temperature up to 573K. Future work can focus on developing BN deposition techniques more suitable for GaN, such as exploring hydrogen-free precursors or other epitaxial growth techniques more suitable for complex substrate structures. The findings from this study provide valuable insights for future research on BN-based gate dielectrics for GaN vertical transistors.

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