Principle and performance analysis of low-power, high-speed, low-noise comparators

Zepeng Lin *

School of Microelectronics, Fudan University, Shanghai, China

*Corresponding author: 20300750003@fudan.edu.cn

Abstract: This paper studies three different structures proposed in recent years and discusses their advantages and properties respectively. A modified strong-arm latch voltage comparator is adapted to 3GHz operating frequency through additional current paths in the pre-amplifier. A latch-type comparator with a dynamic-biased pre-amplifier (DA) greatly reduces energy and improves noise performance through the stabilization of the input common-mode voltage. An FIA comparator further reduces energy and noise and greatly enhances the delay performance and the robustness of the comparator against different input common-mode voltage.

Keywords: Comparator, Double-tailed latch-type comparator, Strong-arm latch comparator, dynamic bias, common-mode rejection, high speed, energy efficient, low noise.

1. Introduction

Comparators, an important building block of mixed-signal devices such as ADCs, have been continuously pushing towards performance limits. As the technology scales down, the demands for comparator design with higher speed, lower energy, reduced noise and better robustness under common-mode voltage fluctuation increases greatly. This paper focuses on three classic designs that achieve better overall performance through modified structures or innovative ideas.

The first design proposes a modified strong-arm latch comparator that reduces its delay and reaches a 3-GHz working frequency through enhancing the output total effective transconductance. By providing 4 additional tail current paths, the effective transconductance increases by 2 times and thus accelerates the speed of the circuit [1].

The second design illustrates an innovative method to reduce energy and noise based on the Elzakker comparator. Through adding a capacitor as tail current source, the common-mode voltage of the input pair is stabilized, and therefore the energy consumption during over-charging is reduced. Larger g_m/I_D is designed by ensuring the comparator to work in deep weak inversion region (WI). Thus, the noise performance is improved [2].

The third design adopts the idea of common-mode voltage stabilization referred in the DA comparator, and proposes the floating inverter pre-amplifier with a reservoir capacitor providing constant and isolated common-mode voltage. Compared with the conventional strong-arm comparator, the proposed design achieves great improvements in delay, noise and energy noise performance, and manifests strong insensitivity and self-adaptiveness towards the fluctuation of input common-mode voltage [3].

This paper is organized as follows. Three classic comparators are introduced in Section II. A comparative analysis is made in Section III, and Section IV concludes the paper.

2. Architecture of The Comparators

2.1 A 1V and 3GHz modified strong-arm latch voltage comparator

The structure shown in the Figure 1 is a conventional SA comparator.

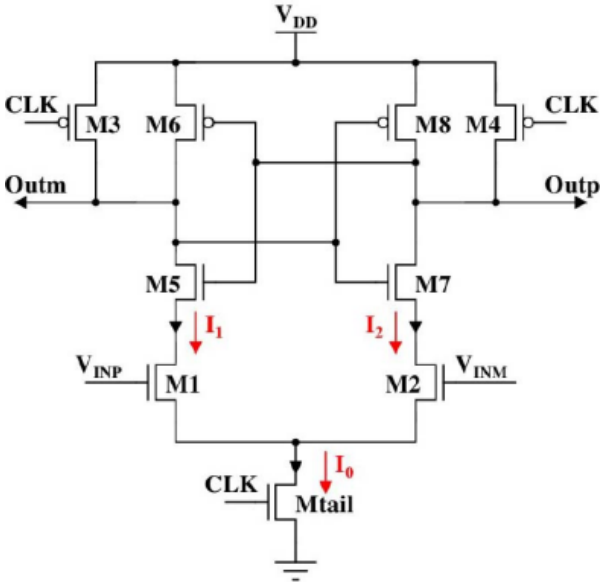


Figure 1. The schematic of a conventional SA comparator

Through mathematical analysis (1) and (2), in the conventional design, the delay and voltage offset are related to C_L and $1/g_{m,\,eff}$, which indicates that the two indexes can be cut down through enhancing the output transconductance $g_{m,\,eff}$ of the back-to-back connected inverters [1].

$$t_{delay,conv} = \frac{2C_L|V_{thp}|}{I_0} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{IN}}\sqrt{\frac{I_0}{\beta_{1,2}}}\right) \quad (1)$$

$$V_{os,conv}|M_{1,2} = \Delta V_{t1,2} + \frac{\Delta\beta_{1,2}}{\beta_{1,2}} \cdot \frac{V_{DSAT1,2}}{2} \quad (2)$$

To increase the effective transconductance of the output node, this paper proposed a modified SA latch comparator with N additional paths, which would ideally reduce delay and offset for $N^{1/2}$ times. The transistor design and level implementation are shown in the Figure 2 and Figure 3 respectively.

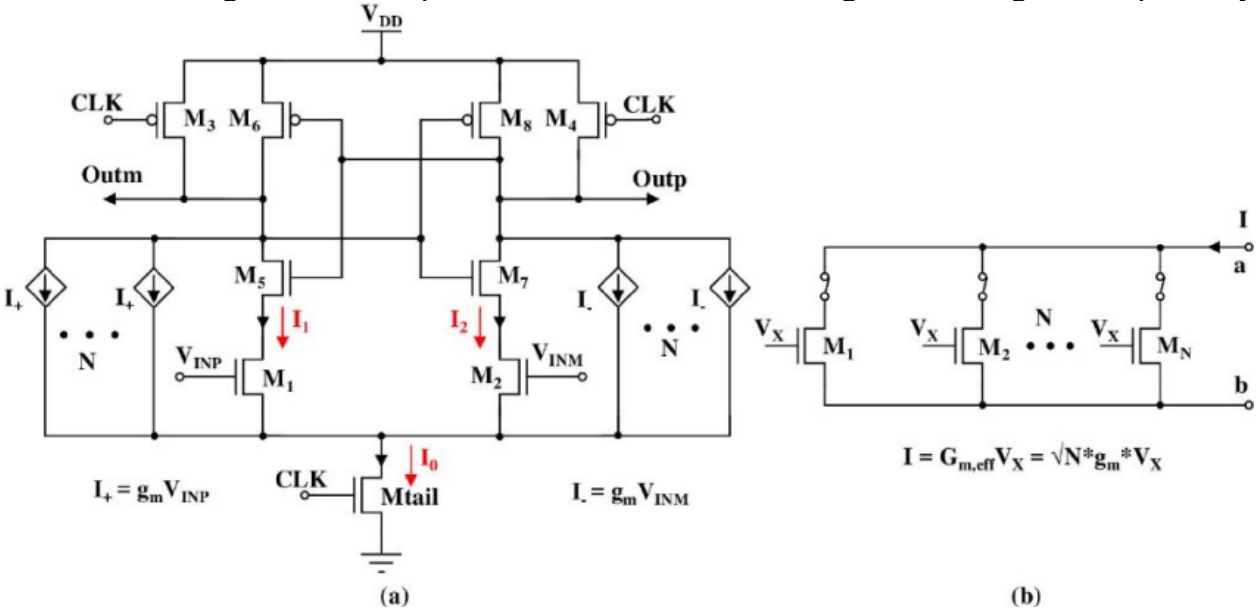


Figure 2. (a) Modified N-parallel path-based SA comparator, (b) Circuit equivalent model

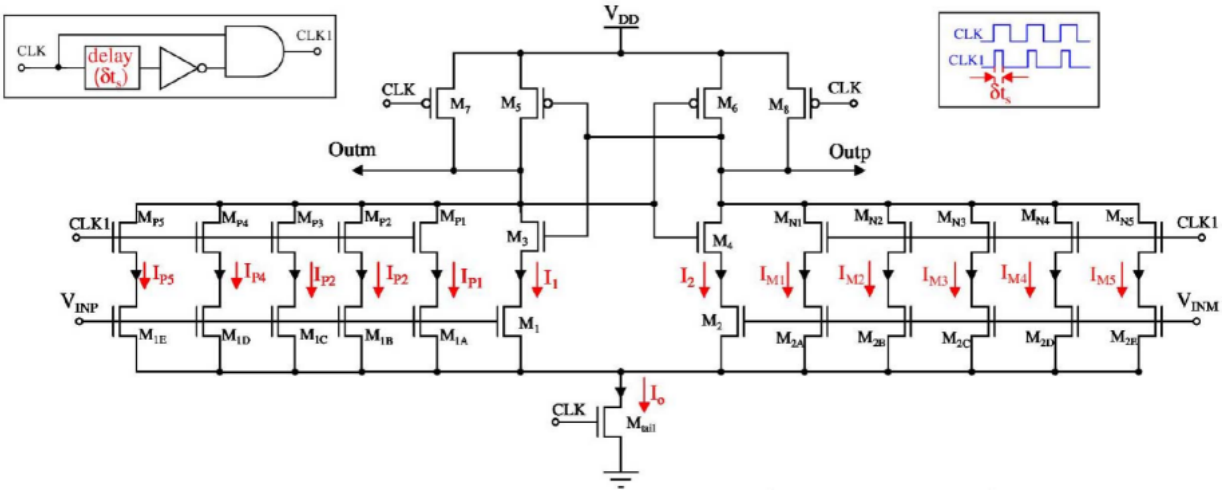


Figure 3. Implementation of the modified SA comparator on transistor level

As is depicted in the Figure 4, the simulated offset and delay approximately remain stable when N is greater than 4. These simulated results can be explained through the equation (3) and (4) respectively calculating the offset and delay of the modified structure [1].

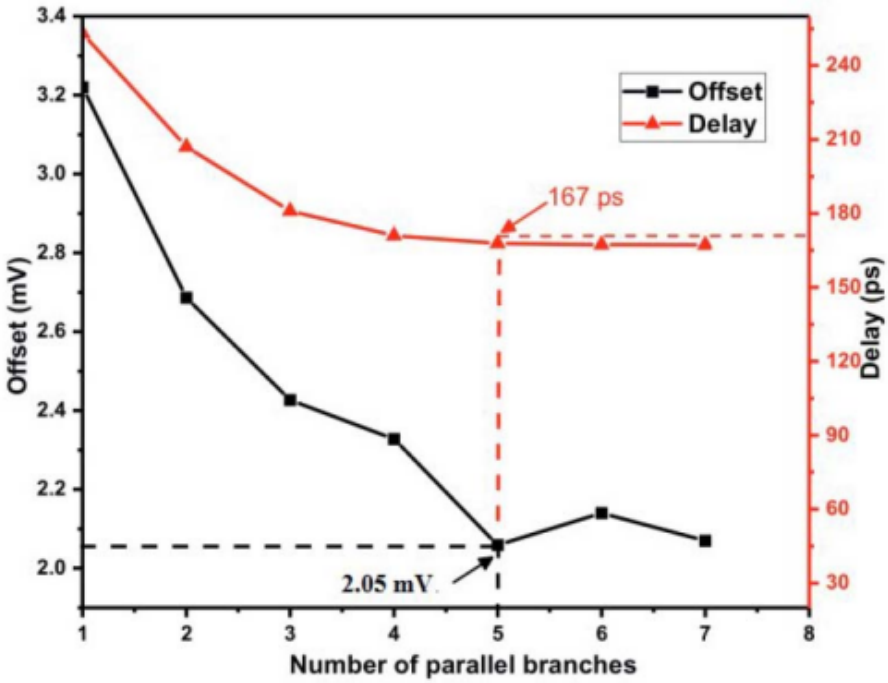


Figure 4. Simulated offset and delay versus N

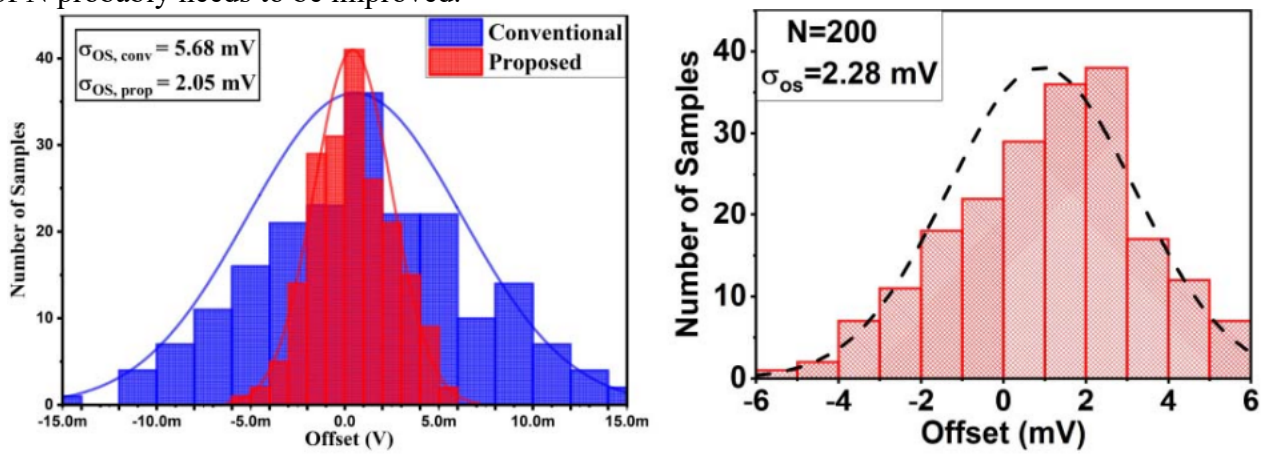
$$t_{delay,prop} = \frac{2C_L|V_{thp}|}{I_0} + \frac{C_L}{G_{m,prop}} \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{IN}}\sqrt{\frac{I_0}{\beta_{1,2}}}\right) \quad (3)$$

$$V_{os,prop}|M_{1,2} = \Delta V_{t1,2} + \frac{1}{\sqrt{N}} \cdot \frac{\Delta\beta_{1,2}}{\beta_{1,2}} \cdot \frac{V_{DSAT1,2}}{2}, G_{m,prop} = g_{mp} + g_{mn} + \sqrt{N} g_{m1,2} \quad (4)$$

Here, g_{mp} and g_{mn} correspond to the latch transistors 3 to 6, while $g_{m1,2}$ refers to the input pair transconductance. Therefore, the second term of the equation (3) is in inverse proportion to the number of the branches N. As N increases and the second term becomes negligible, the first, constant term starts to dominate the outcome of the equation, which leads to the trend line in the Figure 4. [4] This can also explain the trend of the decrease of offset through equation (4).

The author does not analyze the relationship between N and other design parameters (e.g. power), and simply chooses N to be 5 in this design. The reason might be that as the comparator works under the high frequency of 3 GHz, the power of the circuit is not a primary index.

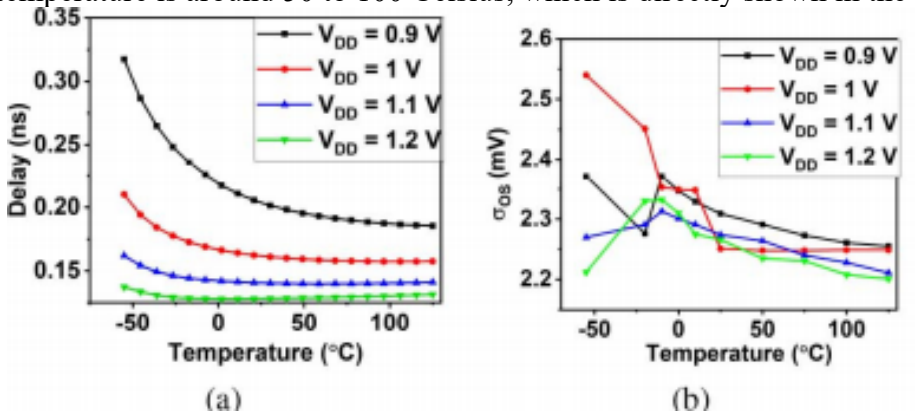
However, in Figure 5, the Monte-Carlo simulation result of the pre-layout simulation for offset is distributed in a standard way that its mathematical expectation is around 0, while after layout there is a 2-mV deviation from zero of the expectation of the offset. This deviation is to some extent related to the asymmetry of the layout because N is chosen to be an odd number 5. Thus, the determination of N probably needs to be improved.



(a) (b)

Figure 5. Simulation offset of conventional and modified structures by Monte-Carlo method, (a) pre-layout, (b)post-layout

From Figure 6 (a), the PVT variations of the comparator in delay, there is a 70% decrease in delay when V_{DD} increases from 0.9V to 1.1V. From Figure 6 (b), increasing V_{DD} does not bring the comparator noteworthy improvement in the offset, particularly when V_{DD} increases from 1.1V to 1.2V. As V_{DD} is also related to the power of the circuit, the best working voltage is around 1.1V. The best working temperature is around 50 to 100 Celsius, which is directly shown in the graph.



(a) (b)

Figure 6. Delay (a) and offset (b) performance variations under temperature and V_{DD} variations

Overall, the proposed strong-arm comparator achieves about 50~60% reduction in delay and voltage offset. However, the area is about 5 times the conventional one's, and the energy is also doubled. The preference of N can be improved in succeeding research.

2.2 A dynamic-biased (DA) latch-type comparator

This paper illustrates an innovative modification on the Elzakker comparator. [5,10] As a modified structure of the double-tailed comparator, the Elzakker design guarantees that the conduction in the latch part will not start until the output voltage Di- and Di+ becomes smaller than the $M_{6,7}$ threshold voltage, which is more energy efficient [2]. This paper further improves the energy consumption of the Elzakker comparator through adding a capacitor in the path of the tail current so as to stabilize the input V_{CM}. This is an innovative way to reduce energy. The two structures are respectively shown in Figure 7.

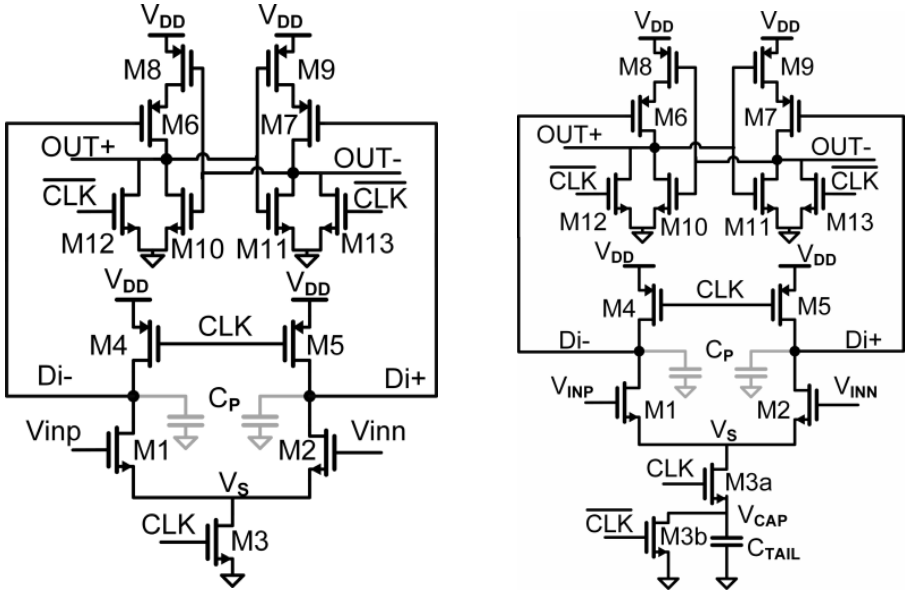


Figure 7. Circuit of Elzakker comparator (a) and dynamic bias comparator (b)

The simulated results of the transient analysis of the proposed circuit are shown in the Figure 8 (a) to (e). Figure 8 (a) indicates that the output V_{CM} of the proposed dynamic bias comparator descends much slower and is consistently higher than that of the Elzakker one. Also, the voltage gain of the proposed one is more stable, and the noise performance is slightly better, as is depicted in (d). As a trade-off, diagram (b) shows that the latch differential output reaches V_{DD} slower, resulting in longer delay. This is partially because of continuously decreasing small tail current, as depicted in (c), which ensures the circuit to work in deep WI region to achieves the greatest g_m/I_D [2].

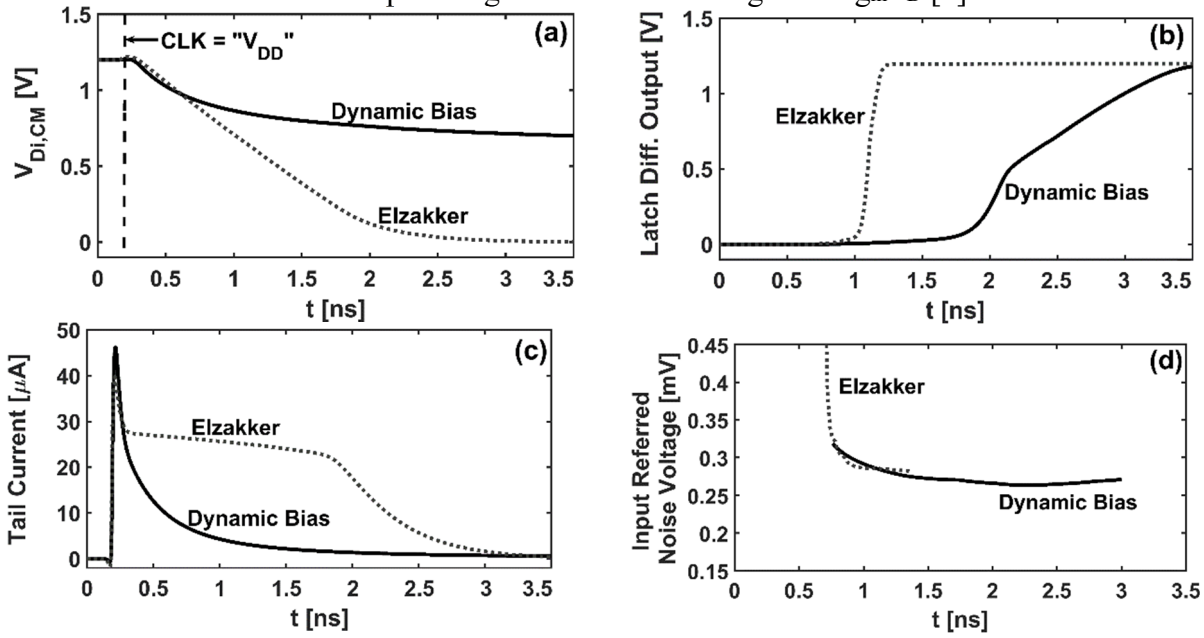


Figure 8. Simulated transient analysis of (a) output V_{CM}, (b) latch differential output, (c) tail current analysis, and (d) input-referred noise at V_{CM} = 0.6V and V_{DD} = 1.2V

g_m/I_D is a newly introduced parameter in the noise analysis of the circuit. [6-7] As presented in the equation (5), the input-referred noise in the WI region that the proposed comparator operates in is inversely proportionate with g_m/I_D, which is g_m/I_{CM} in this specific case. [2] Therefore, larger g_m/I_D can improve the noise performance of the comparator.

$$E\left[v_{n,WI,in}^2(T_{INT})\right] = \frac{2nkT}{C_P \cdot \Delta V_{Di,CM}(T_{INT}) \cdot (\frac{g_m}{I_{CM}})_{WI,T_{INT}}} \quad (5)$$

g_m/I_D increases as common-mode voltage of the input differential pair decreases. Therefore, this paper chooses the common-mode voltage to be 0.6V for the maximum g_m/I_D to improve noise performance. From the simulation results shown in Figure 9, there is a 15% reduction in input referred noise under 0.6V common-mode voltage compared with that of 0.7V.

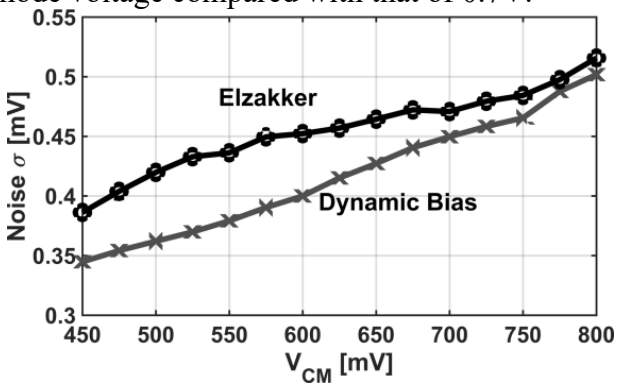
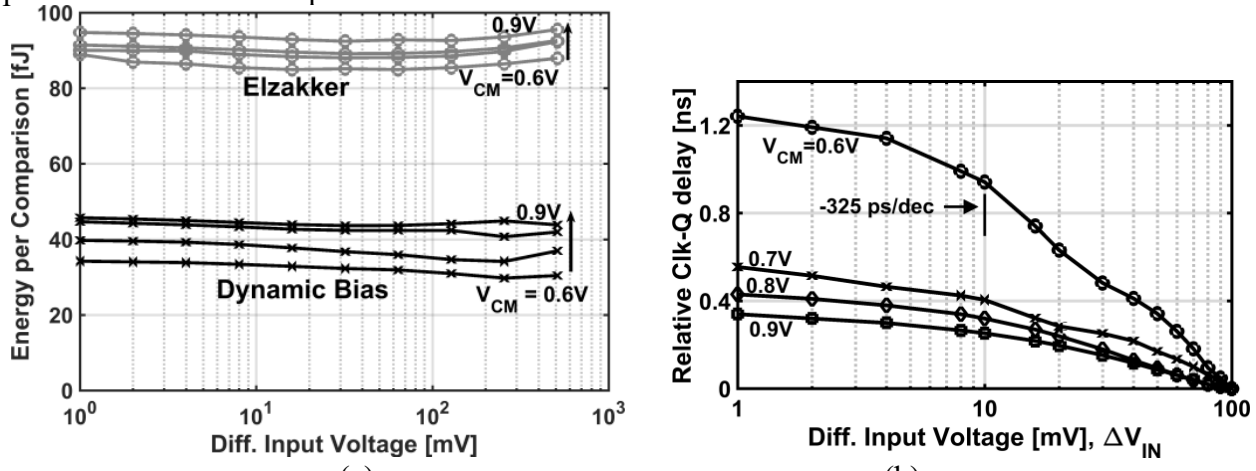


Figure 9. A comparison of the input-referred noise over V_{CM}

Figure 10 (a) shows the energy per comparison of the Elzakker design and the dynamic bias design. Overall, the proposed design achieves a 2-2.5 times energy reduction over the Elzakker one. For the V_{CM} ranging from 0.6V to 0.9V, the energy only sees a 30% increase.

Figure 10 (b) then shows a comparison of the circuit relative delay. The delay sees a 50% reduction when increasing V_{CM} from 0.6V to 0.7V, and decreases greatly as differential input voltage increases. Therefore, compared with energy, delay is more sensitive to the differential input voltage and input V_{CM}, and the best working region speculated from the simulated energy and delay is at a differential voltage of about 50mV and a common-mode voltage of 0.7V to 0.8V, which is inconsistent with the optimized V_{CM} for noise performance.



(a) (b)

Figure 10. (a) The energy performance of DA and Elzakker's comparator over different input and V_{CM}, (b) Relative delay of the dynamic-biased comparator

On the whole, a 15% reduction in noise and energy is achieved by sacrificing a 50% reduction in delay.

To sum up, this paper illustrates an innovative design that optimize energy and input referred noise through stabilizing the common-mode voltage of the differential input pair, which makes the comparator work more stably. This paper also introduces g_m/I_D parameter when optimizing noise performance, but in order to reach maximum g_m/I_D for 15% better noise and energy performance, the design sacrifices delay greatly, for about 50%, which is a possible direction for further improvement.

2.3 An FIA (floating inverter amplifier) comparator

This paper approves the innovative design of input V_{CM} stabilization in the dynamic-biased comparator mentioned above, and enhances the energy and noise performance through stabilizing both the bottom and upper source node of the pre-amplifier [3]. The overall structure is shown in Figure 11.

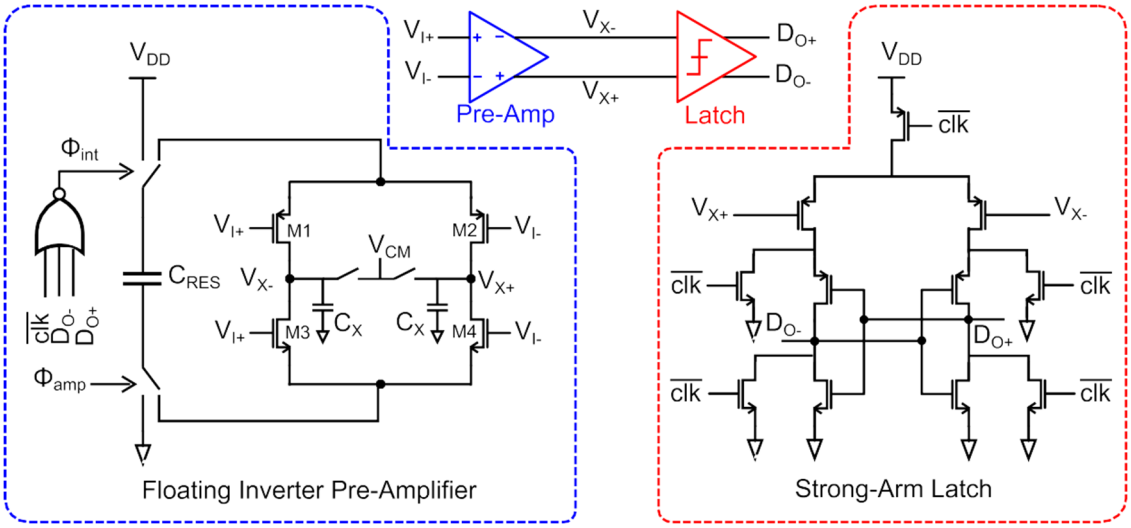


Figure 11. The FIA comparator schematic

At first, a CMOS DB integration pre-amplifier is proposed, as shown in Figure 12. Although it can stabilize the output voltage and increase g_m/I_D, its simulation results with V_{CM} and process corners variation deviates greatly as shown, which manifests that the structure is not robust. [3]

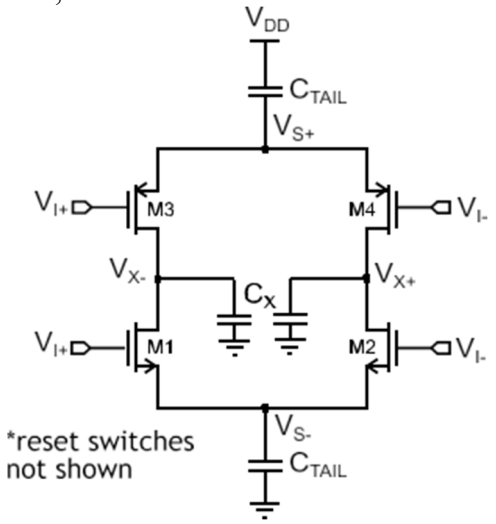


Figure 12. The discarded CMOS dynamic-biased integration model

To solve this problem, a floating inverter amplifier (FIA) connected to a pre-charged reservoir capacitor that provides an isolated and relatively constant working voltage for the pre-amplifier is proposed. [3,8] The simulation results of the pre-amplifier indicate the robustness of the proposed comparator, as is depicted in Figure 13.

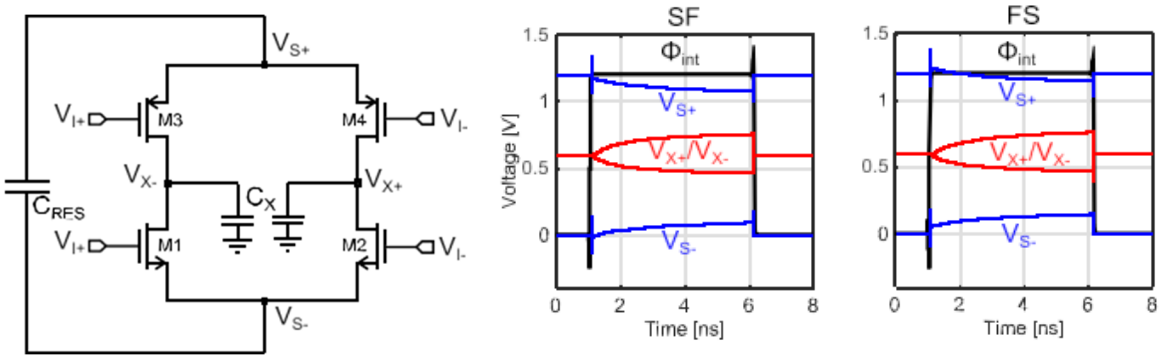


Figure 13. (a) Proposed FIA structure powered by C_{RES}, (b) FIA behavioral simulation against process corner variation

In the noise and the energy efficiency analysis, the input referred noise is calculated and the figure of merit (FoM) of the comparator is defined as the multiplication of the noise and energy [3]. Both input referred noise and FoM are inversely proportionate with g_m/I_D, as is shown in equation (6) and (7). Besides, the larger reservoir capacitor reduces noise as well.

$$\sigma_{in,FIA}^2(T_{INT}) = \frac{2nkT}{C_{RES}\cdot\Delta V_S(T_{INT})\cdot(\frac{g_m}{I_D})} \tag{6}$$

$$FoM_{SA} = \frac{4nkT\cdot {V_{DD}}^2}{V_{THN}\cdot(\frac{g_m}{I_D})} \qquad FoM_{FIA} = \frac{4nkT\cdot V_{DD}}{(\frac{G_m}{I_D})} \tag{7}$$

The energy efficiency improvement is correspondingly proportionate with g_m/I_D.

$$\frac{FoM_{SA}}{FoM_{FIA}} = \frac{V_{DD}}{V_{THN}}\cdot\frac{(G_m/I_D)_{FIA}}{(g_m/I_D)_{SA}} \tag{8}$$

As reservoir capacitor is realistic, the parasitic capacitance impact is not negligible [9]. Thus, there exists a relation between input and output V_{CM}. Figure 14 displays that, when input V_{CM} increase, both the output V_{CM} and gain decreases, which indicates that a relatively smaller input V_{CM} is preferred. This innovative analysis needs to be elaborated in the design because of the unique structure of the comparator.

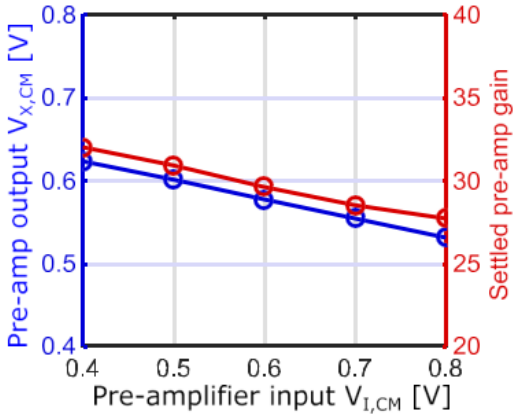


Figure 14. Simulated pre-amplifier output V_{CM} and gain versus the input V_{CM}

The determination of the value of the reservoir capacitor involves several considerations. From Figure 15 (a), the simulated delay against capacitance indicates that a value larger than 3pF is a good choice. Larger capacitance brings faster pre-amplification, and it also leads to more robustness because the slope of the delay decreases as capacitance increases and the comparator will reveal less sensitive to PVT variations. From Figure 15 (b), the simulated FoM shows that in reality, a 2.5-3.5pF reservoir capacitor will lead to the best energy efficiency [3]. However, the final value is determined to be 2pF, and this value takes the g_m/I_D and area penalty into consideration. Unfortunately, the

simulation relation between the g_m/I_D factor or area penalty and the reservoir capacitance is not given in the paper. Thus, there perhaps exist room of improvement in the value of reservoir capacitor.

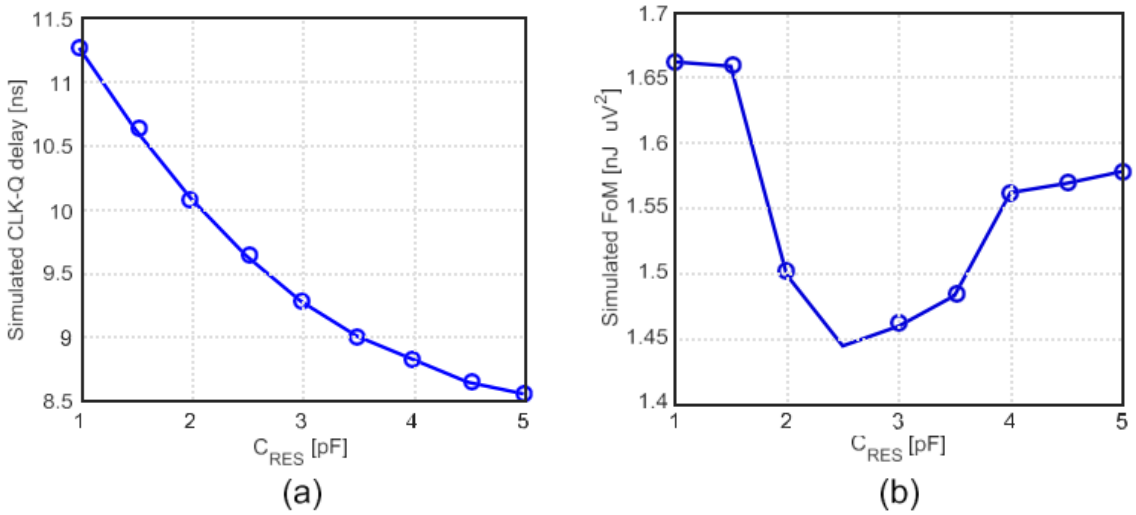


Figure 15. The simulation of (a) relative delay and (b) FoM of the FIA versus C_{RES}

From Figure 16, compared with the conventional structure, the FIA comparator achieves 4 to 7 times improvement in delay under the common-mode voltage of 0.4V to 0.6V, and the delay is insensitive to the change of voltage. The measured input referred offset also shows the stability and robustness of the design. The measured energy consumption of the proposed comparator is also consistent under different common-mode voltage, and achieves a 4 to 5 times reduction as well, as is depicted in Figure 17.

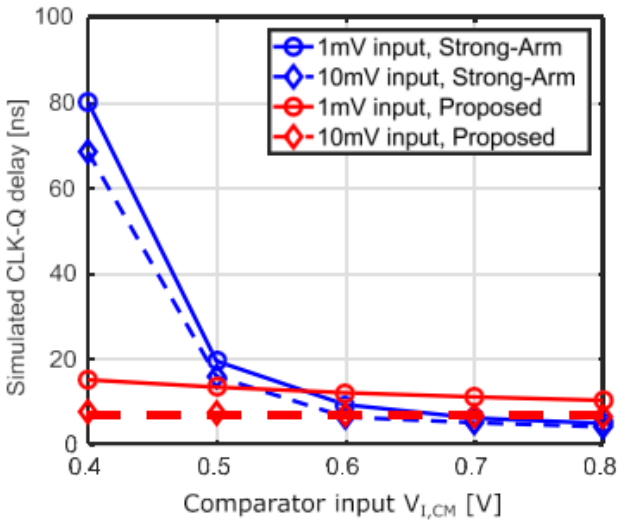


Figure 16. Simulated delay versus V_{CM}

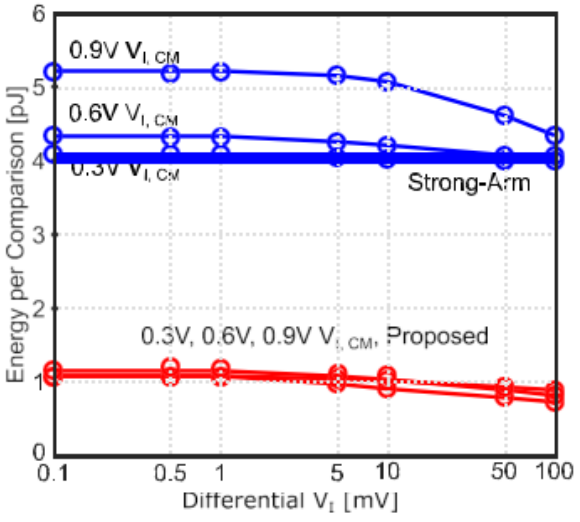


Figure 17. Measured energy consumption versus V_{CM}

In order to fully exploit the potential of this comparator, it should be applied under conditions when input common-mode voltage fluctuates greatly or remains relatively small (lower than 0.6V), and meanwhile the noise performance is highly required.

3. Performance comparison

Table.1. Comparison of the three types of comparators

Type	N-parallel SA Latch-type Comparator	Dynamic-biased Double-tailed Latch-type Comparator	SA Latch Comparator with Floating Inverter Pre-Amplifier
Technology [nm]	65	65	180
Supply [V]	1	1.2	1.2
Noise [μV]	2005	400	46
Energy [pJ]	0.108	0.034	0.98
Area [μm^2]	603	125	9800
Relative CLK-Q Delay [ps/dec]		325	10-20
Maximum Frequency [GHz]	3		
Insensitive to input CM voltage			Yes

Table 1 generalizes the gauged performance of the three classic comparators studied in the paper. From the comparison, the SA latch comparator with FIA achieves the lowest noise and the smallest relative delay, which is an ideal alternative for system with strict noise requirements. The dynamic-biased latch comparator achieves the lowest energy and area along with a second-best noise performance, being suitable for low-energy and high-density occasions. The N-parallel SA latch comparator reaches the highest maximum working frequency, which is intended for system emphasizing high speed.

4. Conclusions

Three classic designs of the comparators and their respective optimization methods are illustrated in this paper. Each design achieves great improvement over its counterparts or the state-of-the-art designs in certain aspects, including speed, energy, noise and robustness. Compared with the conventional one, the modified SA comparator for high-speed applications achieves over 60% reduction in delay, but a 2-mV deviation of the expectation of the offset is generated partially due to the asymmetry of the current paths. Through common-voltage stabilization and g_m/I_D analysis, the dynamic bias comparator achieves 2 to 2.5 times energy reduction over the Elzakker comparator and a 15% input referred noise reduction, and the common-mode voltage is optimized to be 0.6V. However, the optimized common-mode for overall energy and delay performance is around 0.7V to 0.8V, which is inconsistent with that of the g_m/I_D analysis. In the design of the FIA, a reservoir capacitor is proposed to further stabilized the common-mode voltage through providing an isolated and constant voltage. Through the new structure, the proposed comparator achieves over 4 times reduction in both delay and energy. Moreover, the offset variation is largely reduced, and both the energy and delay remain almost consistent under the variation of input common-mode voltage, which manifest its strong robustness. Unfortunately, the value of the reservoir capacitor, 2pF, is contrary to the simulated results of delay and FoM, and the relation between g_m/I_D or area and the reservoir capacitance is not elaborated.

To further improve the design mentioned above, for the first design, the value of N can be optimized through looking into relation between N and symmetry, energy and other important parameters. For the second design, there probably still exists room for an improvement of the trade-off between g_m/I_D for noise performance and energy-delay performance. For the third design, the value of the reservoir capacitor can probably be ameliorated through a more elaborated discussion into the relation of g_m/I_D and area over capacitance.

References

[1] Siddharth R, Satyanarayana Y, Nithin Kumar Y, Vasantha M and Bonizzoni E. A 1-V, 3-GHz Strong-Arm Latch Voltage Comparator for High Speed Applications [J]. IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 12, pp. 2918-2922, Dec. 2020.

[2] Bindra H, Lokin C, Schinkel D, Annema A and Nauta B. A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise [J]. IEEE Journal of Solid-State Circuits, vol. 53, no. 7, pp. 1902-1912, July 2018.

[3] Tang X. et al. An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier [J]. IEEE Journal of Solid-State Circuits, vol. 55, no. 4, pp. 1011-1022, April 2020.

[4] Figueiredo P and Vital J. Kickback noise reduction techniques for CMOS latched comparators [J]. IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53, no. 7, pp. 541-545, July 2006.

[5] Elzakker M, Tuijl E, Geraedts P, Schinkel D, Klumperink E and Nauta B. A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s [J]. IEEE Journal of Solid-State Circuits, vol. 45, no. 5, pp. 1007-1015, May 2010.

[6] Nuzzo P, Bernardinis F, Terreni P and Plas G. Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures [J]. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 6, pp. 1441-1454, July 2008.

[7] Sepke T, Holloway P, Sodini C and Lee H. Noise Analysis for Comparator-Based Circuits [J]. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 3, pp. 541-553, March 2009.

[8] Akter M, Makinwa K and Bult K. A Capacitively Degenerated 100-dB Linear 20–150 MS/s Dynamic Amplifier [J]. IEEE Journal of Solid-State Circuits, vol. 53, no. 4, pp. 1115-1126, April 2018.

[9] Tang X, Chen L, Song J and Sun N. A 10-b 750μW 200MS/s fully dynamic single-channel SAR ADC in 40nm CMOS [C]. ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, 2016, pp. 413-416.

[10] Bindra H, Lokin C, Annema A and Nauta B. A 30fJ/comparison dynamic bias comparator [C]. ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference, 2017, pp. 71-74.