Performance Analysis for Energy-Efficient Comparators

Ruichen Deng*

School of Control Engineering, Northeastern University at Qinhuangdao, Qinhuangdao, China

*Corresponding author email: 202013113@stu.neuq.edu.cn

Abstract: This work studies three different comparator proposed in recent years. Compared to the strnongARM latch as well as the Elzakker's comparator, the dynamic comparator added cross-coupled devices that keeps the pre-amplifier's integration nodes from fully discharge to the ground and thus improves energy performance. The dynamic bias latch-type comparator is an innovative design which added a tail capacitor to the pre-amplifier in order to block off the discharge route between the internal nodes and the ground. Though this design reduced the energy consumption significantly compared with the Elzakker's comparator, it results in longer delay and only little improvement on the input-referred noise. The FIA dynamic comparator implemented a floating inverter amplifier (FIA) that utilizes a reservoir capacitor which cuts off its charging path and discharging path significantly reduced the energy consumption and improved noise performance to power itself.

Keywords: Comparators, Low-power, Low-noise, Delay.

1. Introduction

Comparators are the interface between the physical world and the digital world as it is the crucial part for the ADCs. In order to meet the demand of low-energy-cost situations like devices that requires batteries and low-noise situations such as neural implants, comparators with low power and low input referred noise are desirable. The StrongARM latch was once used widely due to its low delay, negligible static power consumption and rail-to-rail outputs. However, it suffers from its kickback noise and voltage headroom. Thus, the double-tail latch-type comparator separated the pre-amplifier from the latch. It allows us to control the latch's time to regenerate and the performance of the pre-amplifier as well as optimize them separately.

The comparator in [1] added cross-coupled devices to the pre-amplifier and achieved a 30% energy reduction compared with the Elzakker's comparator proposed in [2] while not implementing any capacitor or complex circuit.

Based on the Elzakker's comparator, the comparator proposed in [3] is to obtain a solution that consumes less energy per comparison by implementing a tail capacitor that can escalate the source voltage V_S while the comparison process to prevent the pre-amplifier's integration nodes from fully discharge. Compared with the conventional dynamic comparator, it achieves an energy consumption reduced by about 2.5 times for the nominal common-mode voltage 0.6V ($V_{DD}/2$). However, it leads to a higher CLK-Q delay and there's only little improvement on the input referred noise performance.

The comparator proposed in [4] introduced a floating reservoir capacitor helps to reduce the energy further and also mitigated the input referred noise significantly and also lead to the insensitivity to input common-mode voltage and the speed of the transistors.

This paper is organized as fallows. Section II reviews the dynamic comparator with cross-coupled devices. Section III presents descriptions as well as analysis of the dynamic bias comparator. Section IV revisits the energy-efficient comparator with FIA. Section V shows the performance comparison for the three comparators. And Section VI summaries this paper.

2. Dynamic comparator with cross-coupled devices

In this passage published in 2020, the authors presented a comparator for low power consumption as showed in Fig.1. The authors added cross-coupled devices to the pre-amplifier that keeps its output nodes from fully discharging. Fig.2 shows that the proposed circuits reduced the energy consumption

while obtaining the same noise level (the proposed circuit has slightly higher input referred noise) compared with the comparator proposed in [2]. However, for small input differential voltage, the proposed circuit has a longer delay as illustrated in Fig.3.

The added cross-coupled devices and the regenerative latch operates in two phases during CLK is on as illustrated in Fig.4. During phase-I (Fig.4(a)) M_{21} and M_{22} both operates in linear region. As the integration nodes' voltage drops, at input differential voltage-controlled rate, one of the transistors will turn off, thus its drain voltage will be fixed and the pre-amplifier goes into phase-II (Fig.4(b)) (the author assumed I_1 is larger and M_{22} turned off). As the voltage of intP is fixed, the voltage of the transistor M_{21}'s gate is fixed. This leads to a lower rate for node intN to discharge.

Fig.5 showed the simulation of a conventional comparator and Fig.6 showed the simulation of the proposed circuit. As it presents in Fig.5(a) and Fig.6(a), the conventional comparator discharges its internal nodes fully to the ground while in the proposed circuit the internal nodes only discharge partially. It also shows that in Fig.5(b) and Fig.6(b), the proposed circuit has a longer delay than the conventional comparator.

Though the proposed circuit has similar noise and higher delay, comparing with other works to lower the consumption of energy, this work uses lower V_{DD} supply and does not need any capacitors or complex logical circuit and thus occupies smaller area.

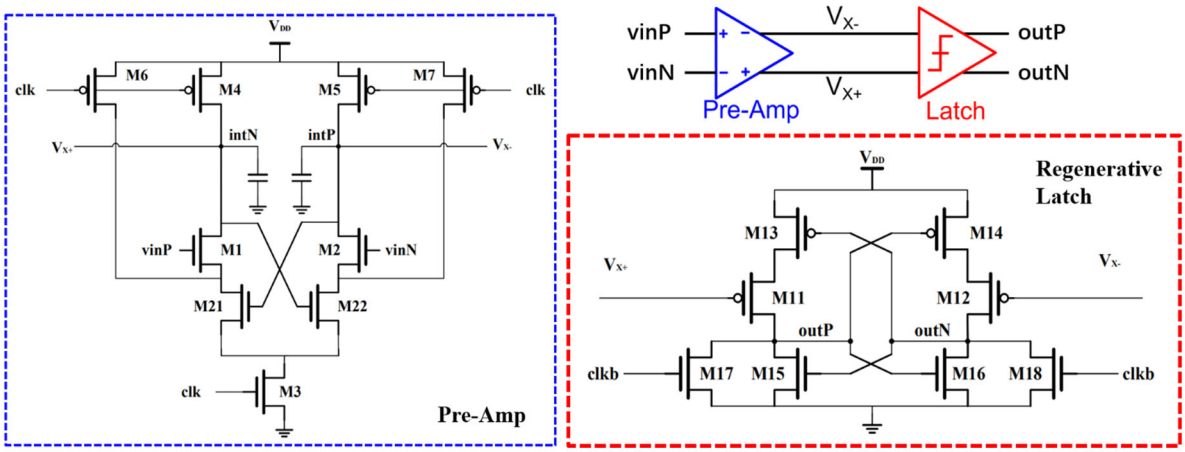


Fig.1: Proposed comparator schematic

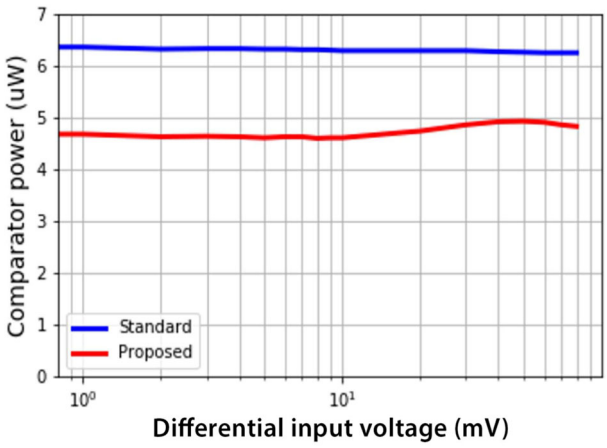


Fig.2: Simulated power versus input differential voltage with 0.5V V_{CM}

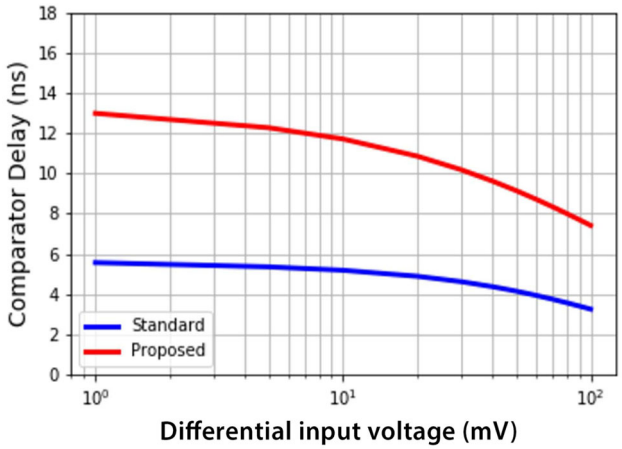


Fig.3: Simulated delay versus differential input voltage with 0.5V V_{CM}

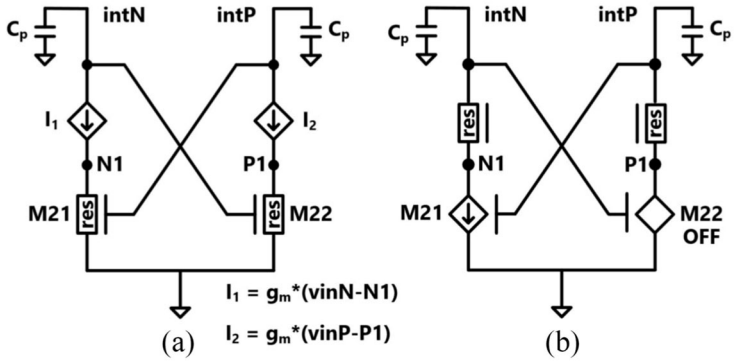


Fig.4: The proposed preamplifier during (a) phase-I and (b) phase-II

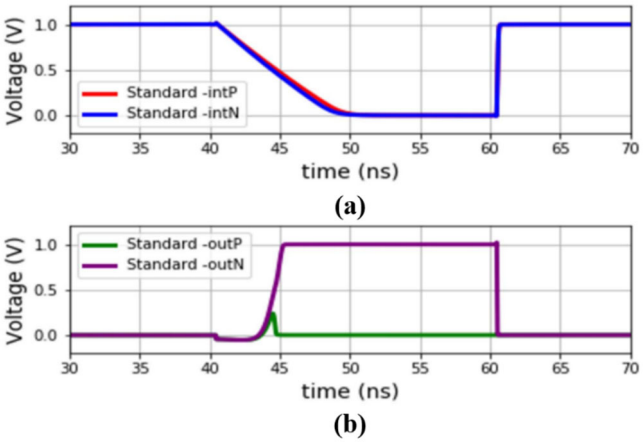


Fig.5: Simulation of the comparator in [2] with 5-mV differential input voltage while $V_{CM} = 0.5V$

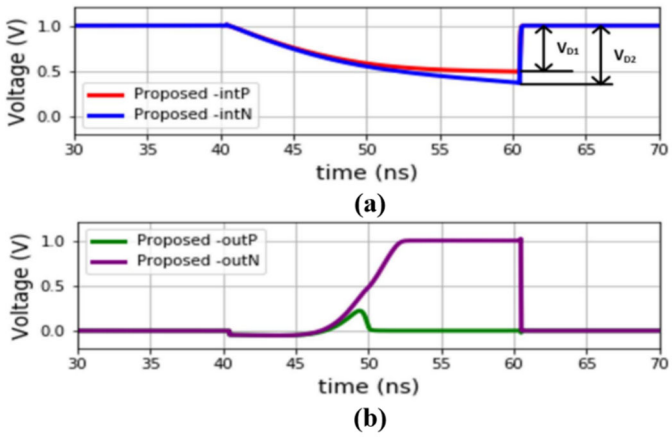


Fig.6: Simulation of the proposed comparator with 5-mV differential input voltage while $V_{CM} = 0.5V$

3. Dynamic bias latch-type comparator

In this passage published in 2018, the authors added a tail capacitor in order to partially discharge the internal nodes and thus abate the energy per comparison consumes. Fig.7 shows the topology of the proposed comparator and the Elzakker's which is proposed in [2]. Fig.8(a) and Fig.8(b) shows that comparing with the Elzakker's, the proposed comparator's voltage on the pre-amplifier's integration nodes is more stable (less voltage drop). Thus, the dynamic bias comparator can operate more stably and it has a smaller range for charging and discharging. However, it caused a longer CLK-Q delay and little improvement on the input referred noise compared with the Elzakker's.

During the simulation, the authors compared the two comparators. Fig.9(a) indicates that the dynamic bias comparator operates at a smaller tail current in the pre-amplifier which leads to less energy consumption per comparison. Fig.9(b) shows that the proposed comparator's pre-amplifier has a slightly smaller noise than the Elzakker's. It indicates that in Fig.9(c), however, the proposed comparator requires a longer generation time. It illustrates that the proposed comparator takes nearly ten times longer to generate the output signal.

The voltage gain of the proposed pre-amplifier is:

$$A_V(T_{INT}) = \frac{C_{TAIL}}{2n \cdot C_p} \cdot \frac{V_S(T_{INT})}{\frac{kT}{q}} \tag{1}$$

Where T_{INT} represents the integration time and V_s represents the source voltage of M1 and M2. And its input referred noise can be given as:

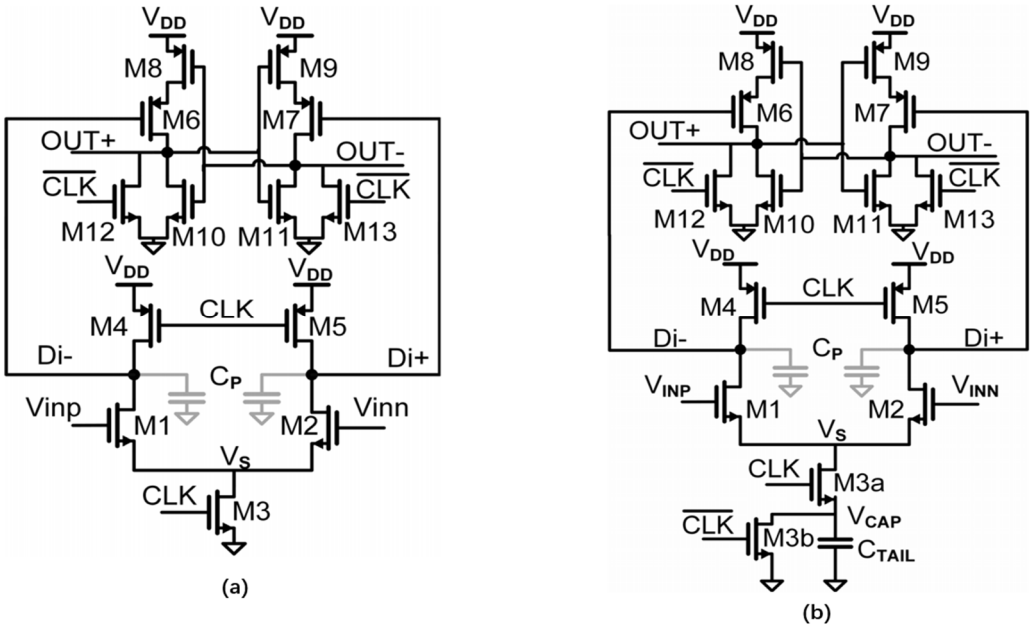


Fig.7: Schematic of (a) Elzakker's comparator (b) dynamic bias comparator

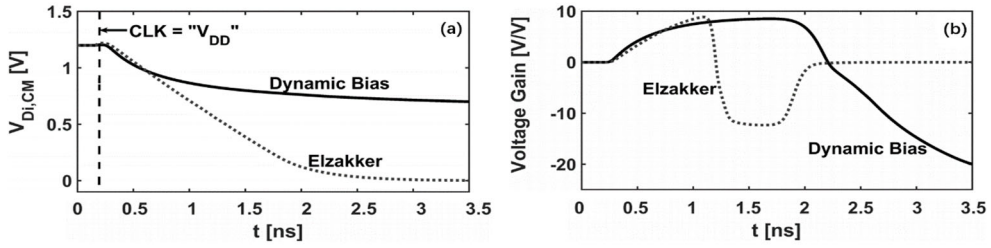


Fig.8: Simulation of: (a) output common-mode voltage (b) voltage gains for 6-mV input differential voltage at $V_{CM} = 0.6V$

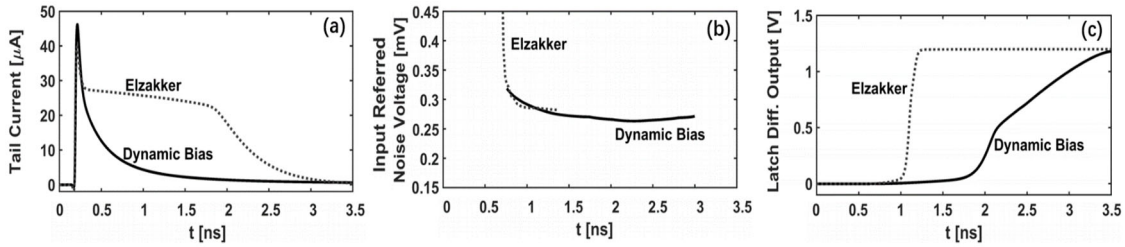


Fig.9: Simulated (a) tail current (b) input referred noise voltage (c) differential latch output for 6-mV input differential voltage at $V_{CM} = 0.6V$

$$E[v_{n,WI,in}^2(T_{INT})] = \frac{2nkT}{C_p \cdot \Delta V_{Di,CM}(T_{INT}) \cdot (\frac{gm}{I_{CM}})_{WI,T_{INT}}} \quad (2)$$

Where $\Delta V_{Di,CM}$ is the common-mode voltage drop of the integration nodes of the dynamic pre-amplifier from the pre-charged voltage V_{DD} and I_{CM} is the common-mode discharging current of the pre-amplifier's integration nodes. To achieve larger gain, C_{TAIL} and C_p can be modified according to (1). C_{TAIL} is the independent parameter of the gain that its value does not influence the noise performance. However, both the voltage gain and the noise are proportional to $1/C_p$, thus if change C_p to achieve larger gain or smaller noise, it sacrifices one another. In order to improve the noise performance, a large g_m/Id is desirable. The connection between $V_{GS} - V_T$ is presented in Fig.10. As the proposed pre-amplifier operates in weak inversion region, thus it has a smaller $V_{GS} - V_T$ and larger g_m/Id than the Elzakker's comparator therefore achieves smaller input referred noise.

Fig.11 is the measurement results of the energy per comparison consumes versus the input differential voltage, showing energy costs under different common-mode voltages for different comparators. It shows that the dynamic bias comparator only costs about 50% of energy that Elzakker's comparator consumes per comparison. The trends of the energy consumption changing with the input voltage, differential and common-mode, however, are very similar. It shows that when $V_{CM} = 0.6V$, the energy consumption per comparison reaches its minimum value for both comparators while the dynamic bias comparator only consumes approximately half the energy the Elzakker's comparator costs.

Fig.12 measures the CLK-Q delay for the two comparators versus ΔV_{IN} under various input common-mode voltages. It implies that for the same V_{CM}, the proposed comparator costs longer delay than the Elzakker's. The two comparator's CLK-Q delay, however, are almost the same when the differential input voltage goes near 100mV.

It also shows that the dynamic bias comparator's CLK-Q delay elongates more as the input common-mode voltage drops when the differential input signal is smaller. It becomes particularly conspicuous when changing $V_{CM} = 0.7$ to $0.6V$. Thus, while implementing the dynamic bias comparator, the common-mode voltage should be around 0.7 to 0.8V. Though higher input common-mode voltage will cause higher energy consumption approximately 15%, it can significantly reduce the CLK-Q delay of the proposed comparator. Also, if the proposed comparator has higher common-mode voltage, it still retains its energy advantage while reaching similar CLK-Q delay for small differential inputs.

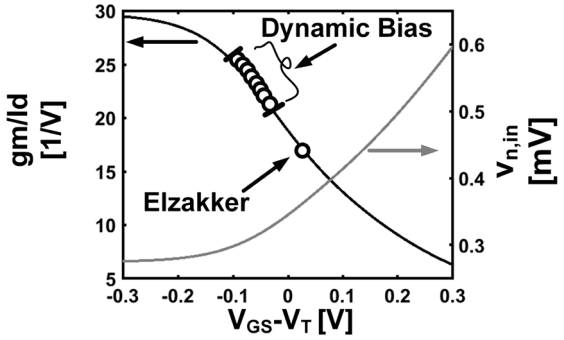


Fig.10: input referred noise and g_m/I_d versus $V_{GS} - V_T$

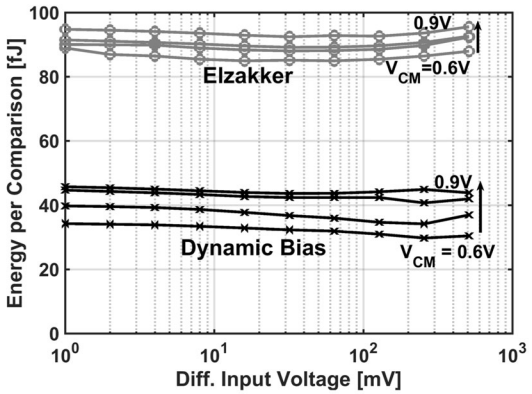


Fig.11: Simulated energy consumption plots versus input differential voltage

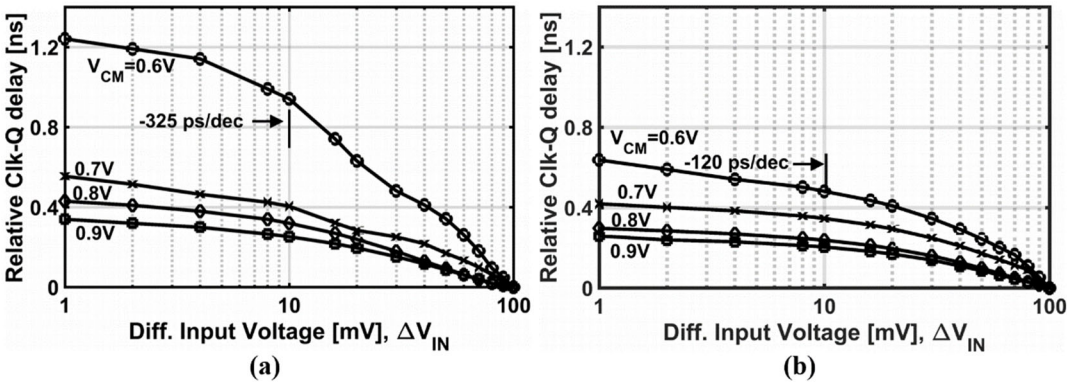


Fig.12: CLK-Q delay of (a) Elzakker's comparator (b) proposed comparator

4. Comparator with dynamic FIA

In this article published in 2020, the authors presented comparator design utilizing a reservoir capacitor which helps to abate the energy consumption and noise significantly. The proposed comparator's schematic is shown in Fig.13.

The C_{RES} shown in the schematic can provide an isolated power domain as well as leads to the comparator's insensitivity to the input common-mode voltage. It also increases g_m/I_D by providing dynamic source degeneration and keeps the internal nodes from fully discharging. Fig.14 shows that the output voltage (both differential and common-mode) of the floating inverter pre-amplifier (FIA) integration nodes are almost identical under both the variation of process corner and input common-mode voltage.

The integration gain of the FIA is:

$$A_V(T_{INT}) = \frac{2C_{RES} \cdot \Delta V_S(T_{INT})}{nC_x U_T} \tag{3}$$

The noise is:

$$\sigma^2_{in,FIA}(T_{INT}) = \frac{2nkT}{C_{RES} \cdot \Delta V_S(T_{INT})} \cdot \frac{I_D}{G_m} \tag{4}$$

Where $G_m = g_{m,n} + g_{m,p}$ represents the proposed FIA's total transconductance.

And the $FoM = Energy \cdot (NoisePower)$ is to represent the energy efficiency (the noise and energy consumption's balance):

$$FoM = 4nkT \cdot V_{DD} \cdot \frac{I_D}{G_m} \tag{5}$$

By the definition, the comparator achieves a higher efficiency when the FoM is smaller.

It can be seen that the voltage gain is inversely proportional to C_x. And C_x is the parameter only influence the voltage gain A_V. Thus, a larger gain can be achieved by reducing the value of C_x without degenerate the noise performance and the FoM-calculated energy efficiency. It also shows that C_{RES} can influence both the voltage gain and the input referred noise. The voltage gain is proportional to C_{RES} and the input referred noise is proportional to $1/C_{RES}$. So, both the voltage gain and the noise performance can be improved by achieving a larger C_{RES}. Plus, both the input referred noise and the FoM are inversely proportional to G_m/I_D. So, to achieve both smaller input referred noise and FoM, a larger G_m/I_D is desirable.

When considering the parasitic capacitance impact, the drop of the common-mode voltage of the internal nodes is estimated as:

$$\Delta V_{X,CM} \approx -2 \cdot \Delta V_{I,CM} \cdot \frac{C_P}{C_X} \tag{6}$$

Where $\Delta V_{I,CM}$ is the input common-mode voltage shift and C_P represents the C_{RES}'s parasitic capacitance as shown in Fig.15. This voltage change will impact the vintage gain slightly.

The measurement result is illustrated in Fig.16. The output common-mode voltage has a approximately 0.1V variation as $V_{I,CM}$ fluctuates from 0.4 to 0.8V. Meanwhile, the variation of the voltage gain is approximately 15%.

Fig.17 measures the CLK-Q delay and the FoM versus the value of C_{RES}. As shown, order to achieve lower CLK-Q delay, a larger C_{RES} should be implemented. In fact, the FoM and C_{RES} are correlated despite (5) showed no connection between them. If C_{RES} adopted in the design is 3pF, the pre-amplifier can achieve both a relatively low CLK-Q delay and FoM. It can be seen that with the value of C_{RES} varying from 2.5 to 3.5 pF, the variation of the FoM is within 0.3%. And the CLK-Q delay diminishes at a relatively low rate. This allows the pre-amplifier to operates steadily under small perturbation of the value of C_{RES}. On the other hand, in order to achieve larger g_m/I_D boost and smaller area, C_{RES} could be implemented as 2pF. Table I presents the devices's sizes implemented in the prototype design proposed in the original article.

Compared with the SA latch comparator, the FIA comparator has smaller input referred noise and diminishes the noise variation versus the comparator input common-mode voltage by nearly four times as shown in Fig.18 and Fig.19.

Fig.20 is the measurement results of the energy consumption versus input differential voltage under various input common-mode voltage.

It shows that there's an approximately 73% reduction in the energy consumption per comparison when $V_{I,CM} = 0.6V$. It also shows that there is little impact in the energy consumption when the $V_{I,CM}$ fluctuates in the proposed circuits.

Table 1 presents the devices's sizes implemented in the prototype design proposed in the original article.

Transistor	Width [μm]	Length [μm]
M_1	44	0.18
M_2	44	0.18
M_3	22	0.18
M_4	22	0.18
Capacitor	**Size [pF]**	
C_X*	0.25	
C_{RES}	2	

*C_X includes the integration node parasitics

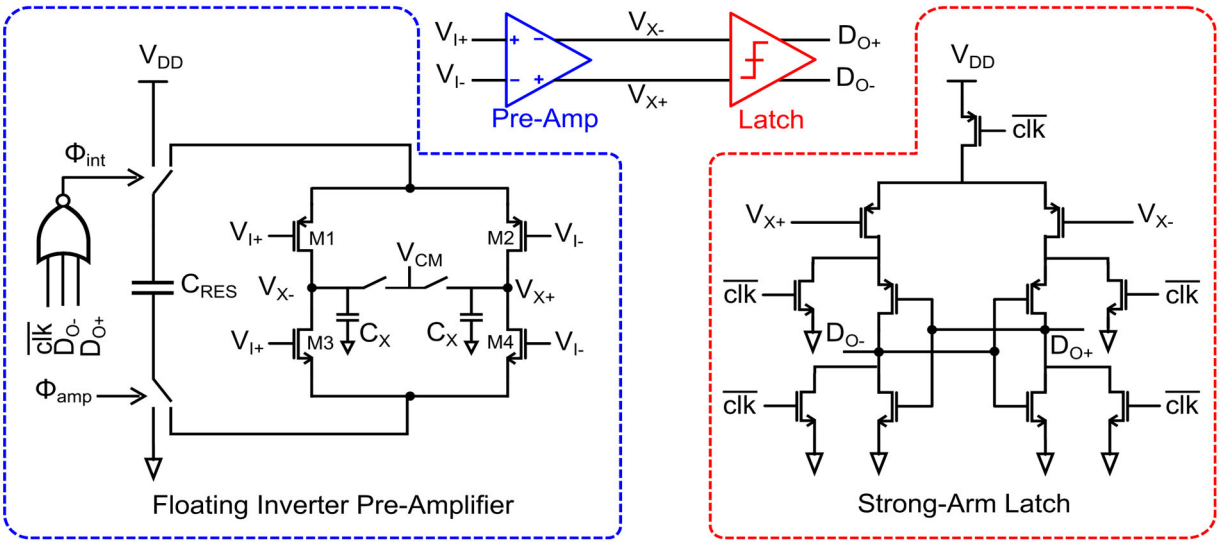


Fig.13: Topology of the FIA comparator

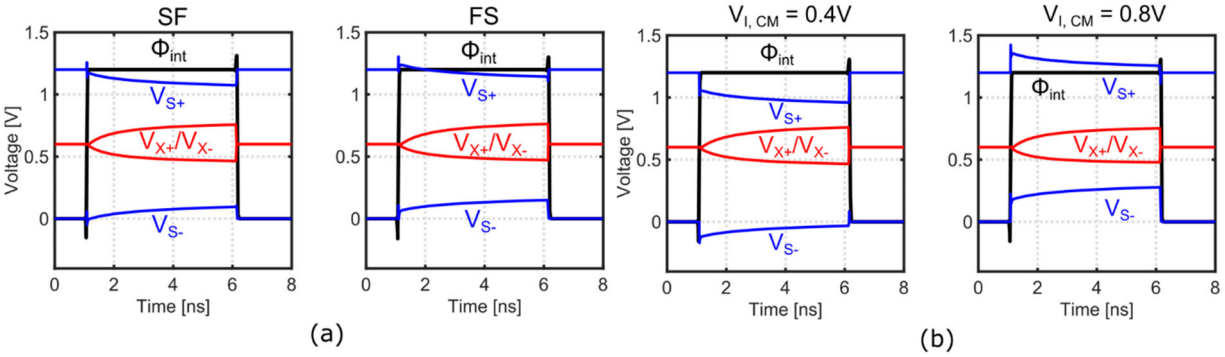


Fig.14: Simulation under (a) different process corner and (b)

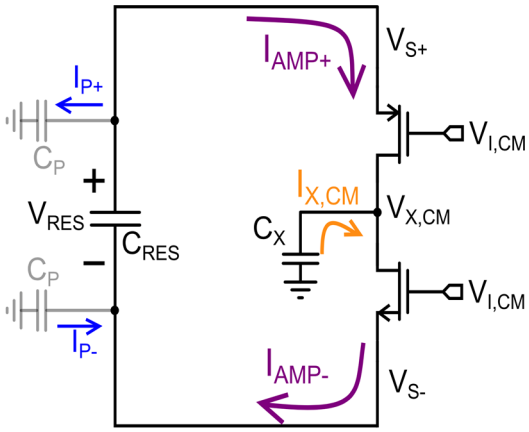


Fig.15: Equivalent circuit when considering parasitic capacitance

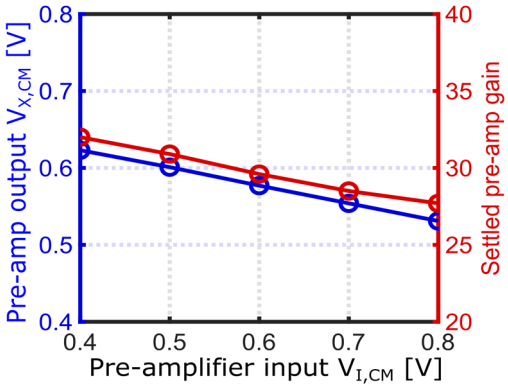


Fig.16: Simulated pre-amp output gain and common-mode voltage

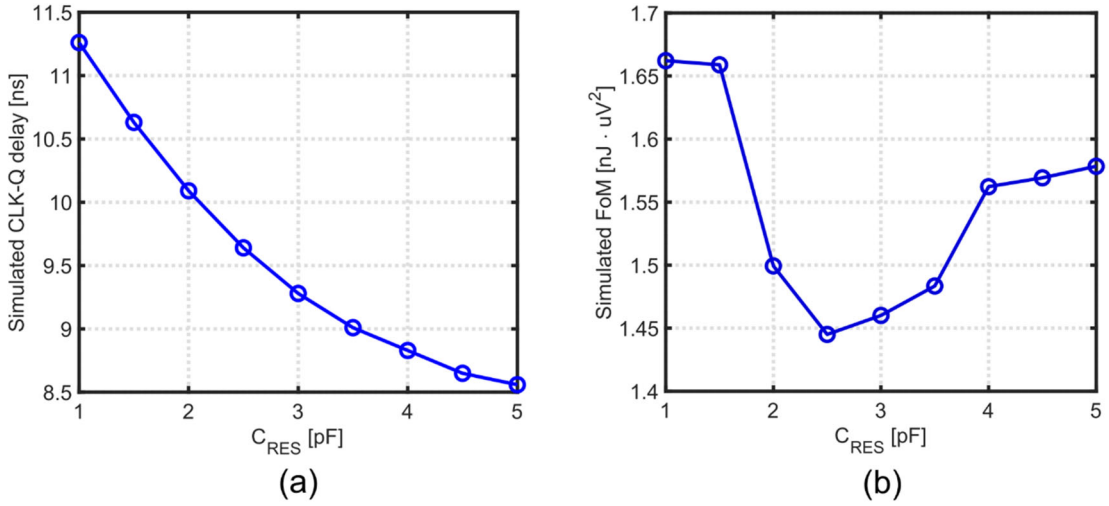


Fig.17: Simulated (a) CLK-Q delay and (b) FoM versus C_{RES} value

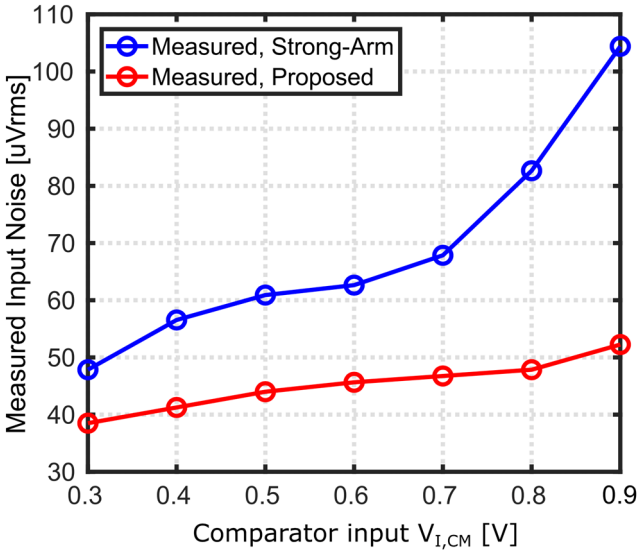


Fig.18: Measured input referred noise

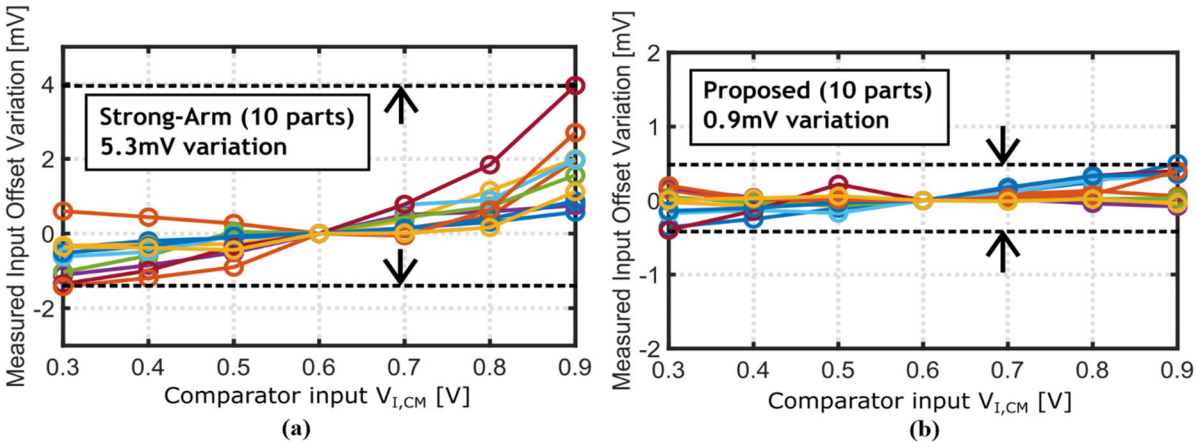


Fig.19: Input referred offer versus $V_{I,CM}$

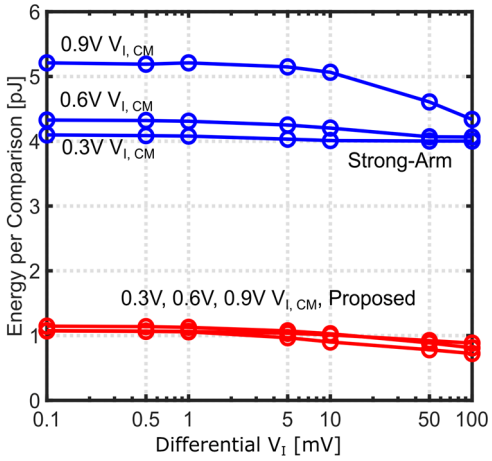


Fig.20: Measured energy consumption under the variation of input

5. Performance comparison

Table 2. Performance comparison

	[1]	[3]	[4]
Architecture	Proposed Circuit	Dynamic Bias	Proposed FIA+SA
Process [nm]	65	65	180
Supply [V]	1	1.2	1.2
Noise [μV]	220	400	46
Energy [pJ]	0.192	0.034	0.98
Area [μm^2]	1025	125	9800
FoM* [$nJ \cdot \mu V^2$]	9.29	5.44	2.07

*FoM = Energy × (Noise Power)

Table II summaries the measurement of the performances of the comparators studied in this paper. The dynamic bias comparator consumes the lowest energy per comparison and achieves the smallest area among these three comparators, making it an ideal block for implementations requires low power and area. Also, the comparator with the FIA has the highest energy efficiency (FoM), which indicates it nicely balanced the tradeoff between the energy and the noise.

6. Conclusion

This paper pays attention to the design and optimization methods of the comparator. All three comparators achieve better performance compared with the prior arts. The dynamic comparator reduced its energy consumption by adding cross-couple devices that does not encompass capacitors and complex logic. The comparator with the FIA added a reservoir to achieve lower energy and noise as well as the insensitivity to input common-mode voltage V_{CM} as well as process corners.

The dynamic bias comparator is an innovative design that added a tail capacitor to its pre-amplifier. Such capacitor could escalate the source voltage V_S and thus only partially discharge the pre-amplifier's integration nodes to improve the energy performance. The energy consumption it achieved reduced by about 2.5 times compared with the Elzakker's comparator for the nominal common-mode voltage. However, it turned out to obtain a higher CLK-Q delay and there's still room for improvement on the input referred noise performance. So, the next step to work on the CLK-Q delay and its input referred noise while maintaining its energy advantage.

References

[1] Chevella S., O'Hare D., O'Connell I. A Low-Power 1-V Supply Dynamic Comparator [J]. IEEE Solid-State Circuits, 2020, 3: 154-157.

[2] van Elzakker M., van Tuijl E., Geraedts P., et el. A 10-bit Charge-Redistribution ADC Consuming 1.9μW at 1MS/s [J], 2010, 45(5): 1007-1015.

[3] Bindra H. S., Lokin C. E., Schinkel D., et el. A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise [J]. IEEE Solid-State Circuits, 2018, 53(7): 1902-1912.

[4] Tang X., Shen L., Kasap B., et el. An Energy-Efficient Comparator with Dynamic Floating Inverter Amplifier [J]. IEEE Solid-State Circuits, 2020, 55(4): 1011-1022.

[5] Schinkel D., Mensink E., Klumperink E., et el. A Double-Tail Latch-Type Voltage Sence Amplifier With 18 ps Setup + Holdtime [J]. IEEE Int. Solid-State Circuits Conf. (ISSCC) Papers, 2007, 314-605.

[6] Bindra H. S., Lokin C. E., Annema A-J., and Nauta B. A 30fJ/comparison Dynamic Bias Comparator [J]. Proc. 43rd IEEE Eur. Solid-State Circuits Conf. (ESSCIRC), 2017, 270-271.

[7] Tang X., Kasap B., Shen L., et el. An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier [J]. Proc. IEEE Symp. VLSI Circuits (VLSI), 2019, C140-C141.

[8] Kobayashi T., Nogami K., Shirotori T., and Fujimoto Y. A Current-Mode Latch Sense Amplifier and a Static Power Saving Input Buffer for Low-Power Architecture [J]. Proc. VLSI Symp., 1992, 28-29.

[9] Liu M., Pelzers K., van Dommele R., van Roermund A., and Harpe P. A 106-nW 10b 80kS/s SAR ADC With Data-Driven Noise Reduction [J]. IEEE Solid-State Circuits, 2016, 51(10): 2435-2445.

[10] Nuzzo P., de Bernardinis F., Terreni P., and van der Plas G. Noise Analysis of Regenerative Comparators for Reconfigurable ADC architectures [J]. IEEE Trans. Circuits Syst. I, Reg. Papers, 2008, 55(6): 1441-1454.