# A Review of Innovative Comparator Designs

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**Abstract.** Three papers on the optimal design of comparator circuits are further analyzed in this work. Each paper presents a method to improve the performance of comparators. Floating inverter amplifier applied an independent capacitor as the source of the preamplifier, which improves the overall performance of the circuit. In another design, a special local clock generator is proposed to control the input of both of the latch stage and the preamplifier, which makes it possible to adjust the speed and improve the energy efficiency. In dynamic bias circuit design, stabilized common-mode voltage is realized by adding a capacitor to the tail of the pre-amplifier of a latch-type comparator, optimizing the power and noise performance successfully.

**Keywords:** Comparator, Floating Inverter Amplifier, Local Clock Generator, Dynamic bias.

## 1. Introduction

Comparators are an important part of many circuits, such as analog to digital converter. The performances of power consumption, delay and noise are important indexes to measure the quality of a comparator design. In recent years, many designs have made their own innovations on the basis of traditional circuits to improve the performance of circuits. The analysis of these fruitful and novel works has important guiding significance for our design work.

The FIA design was proposed by Xiyuan Tang [1]. An independent isolation capacitor is used to make the inverter-based input pair of the whole preamplifier floating, dealing with the failure of the integration in the process corner and with low or high input common-mode voltage. Current reuse is realized with the inverter-based input stage. And gm/Id increases because of dynamic source degeneration realized by the reservoir capacitor. So the improvement of energy efficiency and noise performance are achieved.

A circuit with local clock generator was presented in 2018 [2], in which a local clock generator of special design is used to generate control signals, thus the delay time can be adjusted to its optimum value, with the cross-coupled circuit reducing $V_{I,CM}$. Therefore, optimization of both delay and power consumption can be proved.

An innovative design of dynamic bias comparator was proposed [3]. A capacitor is added to realize it. Voltages of the source nodes are not discharged completely because of the existence of $C_{TAIL}$, so the pre-charge energy is lower than Elzakker's comparator. Due to lower overdrive voltage $V_{ov}$, input pair has higher gm/Id, which leads to lower input referred noise. When $V_{I,CM}$ is equal to half of the supply, the average energy consumption can be reduced by nearly 2.5 times for the same noise. However, at the same time, there is deterioration of delay performance of the proposed circuit. This is where the circuit needs to be further optimized.

The organization of the paper is provided as follows. Section 2 further discusses the comparator with FIA proposed in an article. Circuit with a special local clock generator proposed in another paper is reviewed in Section 3. In Section 4, innovation of the proposed dynamic bias circuit and its optimized performance are studied and further analyzed. The conclusion is presented in Section 5.

## 2. The comparator with FIA

Comparator based on CMOS DB integration realizes optimization on power consumption. Nevertheless, in the SF corner, FS corner, or with low or high $V_{I,CM}$, the outputs of CMOS DB

integration pre-amplifier are pulled to the supply or to the ground, which results in the failure of the integration. So the FIA architecture, which is shown in Figure 2, is proposed in order to deal with this problem.

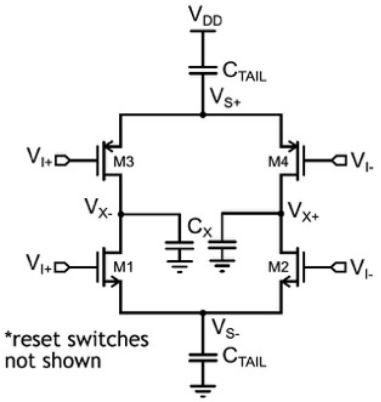



Figure 1. Proposed CMOS DB integration model

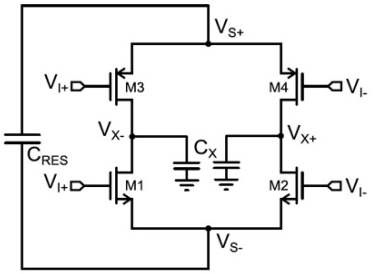



Figure 2. Proposed FIA model

Because of the structure of the circuit, output common mode voltage is a constant [4], [5]. As can be seen from the FIA behavioral simulation result in different process corners and different input common-mode voltage, the integration is correct. The proposed comparator with FIA is designed as Figure 3 shows.

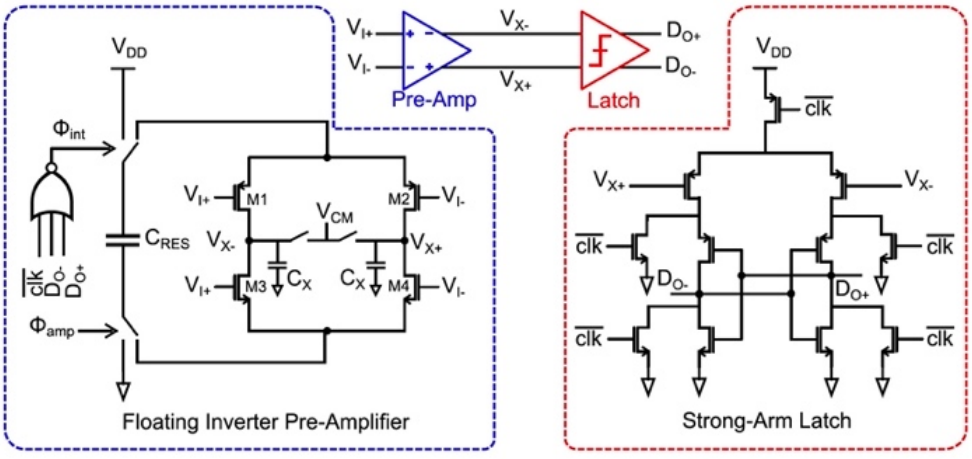



Figure 3. Proposed comparator with FIA

$$A_V(T_{INT}) = \frac{2 \cdot C_{RES} \cdot \Delta V_S(T_{INT})}{n \cdot C_X \cdot U_T}, \quad (1)$$

$$A_V(T_{INT}) = \frac{\Delta V_{X,CM}(T_{INT})}{n \cdot \frac{kT}{q}}, \quad (2)$$

In the part of Pre-Amplifier Gain Analysis, a formula of gain is deduced as (1). $A_V\left(T_{INT}\right)$ of FIA is influenced by $C_{RES}$ and some other parameters that are easy to adjust. However, in the formula

(2), $A_V\left(\mathrm{T_{INT}}\right)$ of DB comparator is not easy to adjust intuitively.

$$\sigma^2_{\mathrm{in,SA}}(\mathrm{T_{INT}}) = \frac{2\mathrm{nKT}}{\mathrm{V_{THN}}\cdot\mathrm{C_X}}\cdot\frac{\mathrm{I_D}}{\mathrm{g_m}}, \quad (3)$$

$$\mathrm{FoM_{SA}} = \frac{4\mathrm{nKT}\cdot\mathrm{V_{DD}^2}}{\mathrm{V_{THN}}}\cdot\frac{\mathrm{I_D}}{\mathrm{g_m}}, \quad (4)$$

Two formula in the analysis regarding noise index and energy efficiency index of SA latch, are taken as examples for further discussion, which are equation (3) and (4). When adjusting parameters to meet multiple design metrics simultaneously, the independent parameters should be adjusted first. The independent parameter of the noise related formula is the parasitic capacitance $\mathrm{C_X}$, and the independent parameter of the power consumption related formula is $\mathrm{V_{DD}}$.

Secondly, the parameters that have great influence on the design index should be adjusted first, and then the parameters that have little influence should be adjusted. The order of the parameter can reflect the magnitude of the influence to some extent, for example, the power is higher than the logarithm. In the formula (4), the square of $\mathrm{V_{DD}}$ should be adjusted preferentially. If the power consumption index $\mathrm{FoM_{SA}}$ cannot meet the requirement, then parameter $\mathrm{V_{DD}}$ can be slightly adjusted.

It is also necessary to clarify the direction of parameter optimization, that is, whether the larger the parameter is, the better it is for the design index or the smaller the better. Therefore, it is necessary to clarify whether the design index is positively or negatively correlated with the parameter. Each parameter is adjusted in a certain direction to obtain a more optimized design index. As far as noise is concerned, the smaller the design index $\sigma^2_{\mathrm{in,SA}}\left(\mathrm{T_{INT}}\right)$ is, the better, so the larger the parameters $\mathrm{V_{THN}}$ and $\mathrm{C_X}$ are, the better, while the smaller the $\frac{\mathrm{I_D}}{\mathrm{g_m}}$ is. The design index $\mathrm{FoM_{SA}}$ of power consumption can be analyzed similarly.

Other formulas can also be analyzed using the same method as above.

$$\sigma^2_{\mathrm{in,DB}}(\mathrm{T_{INT}}) = \frac{2\mathrm{nKT}}{\mathrm{C_P}\cdot\Delta\mathrm{V_{X,CM}}(\mathrm{T_{INT}})}\cdot\frac{\mathrm{I_D}}{\mathrm{g_m}}, \quad (5)$$

$$\sigma^2_{\mathrm{in,FIA}}(\mathrm{T_{INT}}) = \frac{2\mathrm{nKT}}{\mathrm{C_{RES}}\cdot\Delta\mathrm{V_S}(\mathrm{T_{INT}})}\cdot\frac{\mathrm{I_D}}{\mathrm{G_m}}, \quad (6)$$

The performance index formula of different circuits can also be compared. Take noise index as an example. The formulas of $\sigma^2_{\mathrm{in}}\left(\mathrm{T_{INT}}\right)$ of SA latch, DB comparator and proposed FIA are deduced in the article as equation (3) (5) and (6). Comparing these three formulas, $\sigma^2_{\mathrm{in,FIA}}\left(\mathrm{T_{INT}}\right)$ is only related to independent design parameters like $\mathrm{C_{RES}}$, but $\sigma^2_{\mathrm{in}}\left(\mathrm{T_{INT}}\right)$ of SA latch and DB comparator are related to parasitic parameters like $\mathrm{C_X}$ and $\mathrm{C_P}$. Independent design parameters are easier to adjust, while parasitic parameters depend on the size of the transistor and when adjusting the size, it will change the current or other parameters, which results in large changes the circuit to be required to maintain the same current. This is also an optimization.

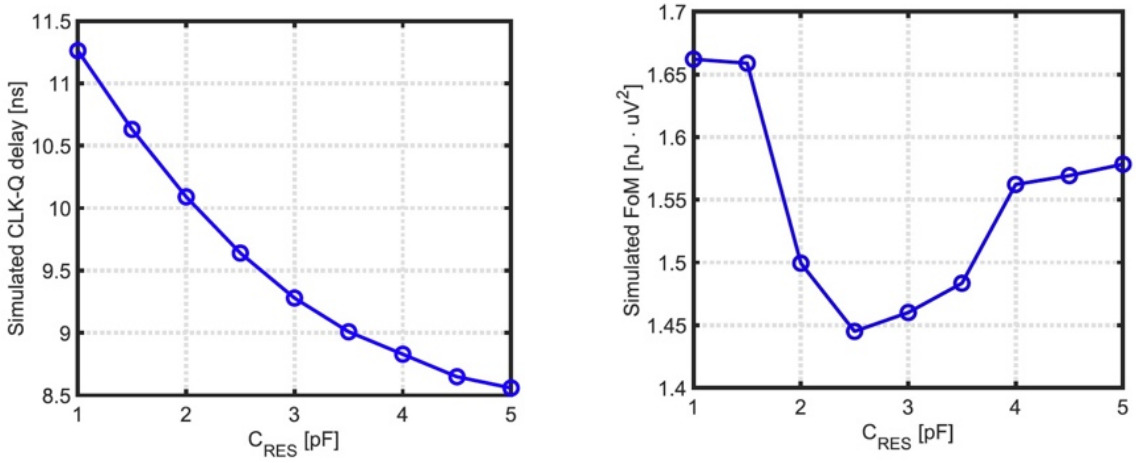
The parameter $\mathrm{G_m}$ is an equivalent transconductance of PMOS and NMOS, which is different from $\mathrm{g_m}$. The equivalent transconductance $\mathrm{G_m}$ is better for optimize the noise index than $\mathrm{g_m}$.

$$\frac{FoM_{SA}}{FoM_{FIA}} = \frac{\mathrm{V_{DD}}\cdot}{\mathrm{V_{THN}}}\cdot\frac{\left(\frac{\mathrm{G_m}}{\mathrm{I_D}}\right)_{FIA}}{\left(\frac{\mathrm{g_m}}{\mathrm{I_D}}\right)_{SA}}, \quad (7)$$

Energy Efficiency of different circuits is also compared in the original text. In the proposed FIA

operation, full discharge of $C_X$, which is unnecessary, is canceled, resulting in the ratio of $V_{DD}$ and $V_{THN}$ in the formula (7). The other advantage is that $G_m/I_D$ in the FIA is 2.5 times larger than $g_m/I_D$ in the SA latch. Energy-efficiency improvement is obvious.

Simulation with regard to delay is also completed.




(a) (b)

Figure 4. (a) CLK-Q delay versus $C_{RES}$ with 1-mV differential input (b) Energy efficiency versus $C_{RES}$

Figure 4(a) discusses the influence of $C_{RES}$ on delay, and according to the unit of FoM, Figure 4(b) discusses the influence of $C_{RES}$ on power consumption.

With the increase of $C_{RES}$, delay decreases continuously and reaches the minimum value when $C_{RES}$ equals 5pF. With the increase of $C_{RES}$, the power consumption exhibits an approximate square law function, and the minimum value is obtained when $C_{RES}$ equals 2.5pF.

When $C_{RES}$ is between 1 and 3, the rate of change of delay is large, while when $C_{RES}$ is between 3pF and 5pF, the rate of change of delay is small. When $C_{RES}$ is between 2pF and 3.5pF, the change rate of power consumption is relatively small. With the intention of improving the stability of the circuit in the actual state, it is necessary to keep the performance unchanged when the circuit parameters change, which means that the parameters should be selected in the interval with relatively gentle changes.

Considering the change trend and rate of delay with $C_{RES}$, $C_{RES}$ should be set between 3 pF to 5 pF. Considering the change trend and rate of power consumption with $C_{RES}$, $C_{RES}$ should be set between 2 pF to 3.5 pF. In order to optimize both delay and power consumption as much as possible, $C_{RES}$ should be set at the intersection of the two, namely the interval between 3 pF and 3.5 pF. However, in the original text, it is not in this interval, but equals 2 pF. There is only one sentence in the original text to mention why this is so, that is, when $C_{RES}$ is equal to 2 pF, the current efficiency is the highest, that is, $\frac{g_m}{I_D}$ is the largest. However, the simulation diagram of the influence of current efficiency on delay and power consumption is not given in the original paper. If the three-dimensional curve diagram of the influence of $C_{RES}$ and $\frac{g_m}{I_D}$ on delay and energy performance can be given in the paper, the reason for the final selection of $C_{RES}$ can be more supported. Therefore, the original text has its shortcomings in data analysis.

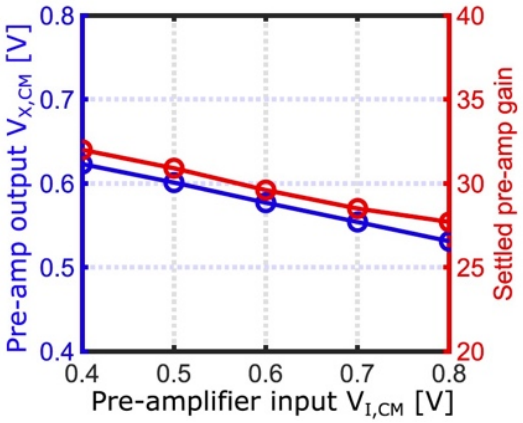



Figure 5. Pre-amplifier output common-mode voltage and settled pre-amp gain versus $V_{I,CM}$

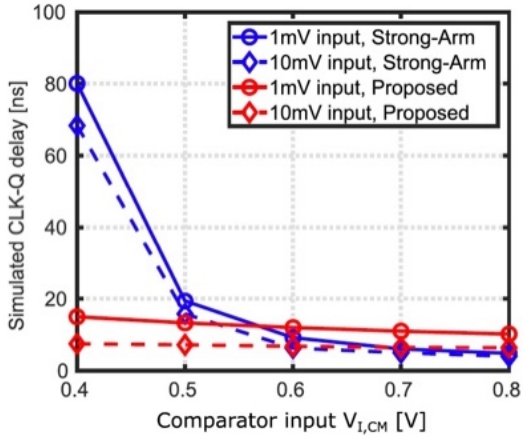



Figure 6. CLK-Q delay versus $V_{I,CM}$

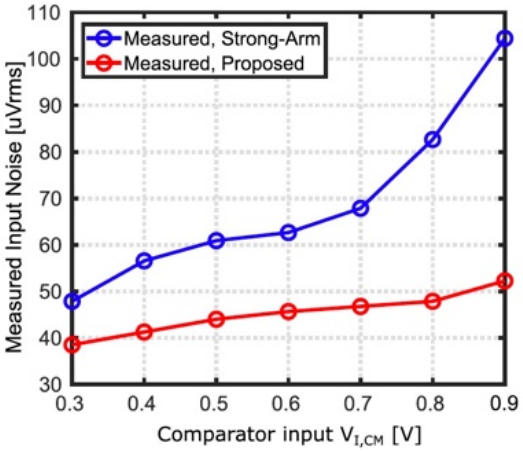



Figure 7. Measured input-referred noise versus $V_{I,CM}$

Figure 5 shows the influence of $V_{I,CM}$ on common-mode voltage and settled pre-amplifier gain. As can be seen from the diagram, as input of the common-mode voltage increases, the two dependent variables decrease at the same time, with a linear relationship. But $V_{X,CM}$ is the bigger the better, settled pre-amplifier gain is the smaller the better, which is a contradiction. Input common-mode voltage should be a compromise value.

Figure 6 and Figure 7 both discuss the influence of the change of $V_{I,CM}$ on the circuit, which are respectively delay and measured input noise, and also add a comparison with the traditional circuit SA latch. Figure 6 shows that the delay performance of proposed circuit is not superior to that of SA latch under all $V_{I,CM}$, but in the range of 0.6V to 0.8V. However, for the measured input noise in Figure 7, proposed circuit is superior to the traditional comparator under any input common-mode

voltage. Therefore, combining the two figures, it can be concluded that input common-mode voltage needs to be selected between 0.6V and 0.8V to realize the simultaneous optimization of delay and measured input noise.

If Figure 5, Figure 6 and Figure 7 are discussed simultaneously, the influence of $V_{I,CM}$ on various performance parameters can be comprehensively considered to obtain the optimum value of it.

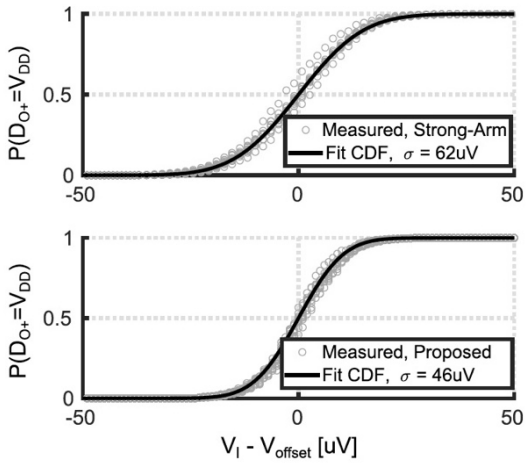



Figure 8. Measured cumulative probability versus $V_I$-$V_{offest}$ and fit to Gaussian distribution

Every point on this graph is measured, which is different from the traditional method, the Monte Carlo simulation. The fitting of the measured results in the experiment is more convincing than the traditional method, which is also the advisable point in data analysis of this paper.

## 3. Comparator with a special local clock generator

Traditional two-stage dynamic comparator is presented in Figure 9 [6], [7]. Using a local clock generator, the control circuit is designed as Figure 10, in which the black inverter is a component that specially designed to realize the adjustment of the delay. The delay time of the evaluation phase can be controlled simply, which means it can be adjusted to the optimum value. The cross-coupled circuit is used with the intention of realizing the optimum delay. It is quite different from the conventional comparator, whose delay is not controllable since charging the output parasitic capacitors to a specific value cost a fixed time.

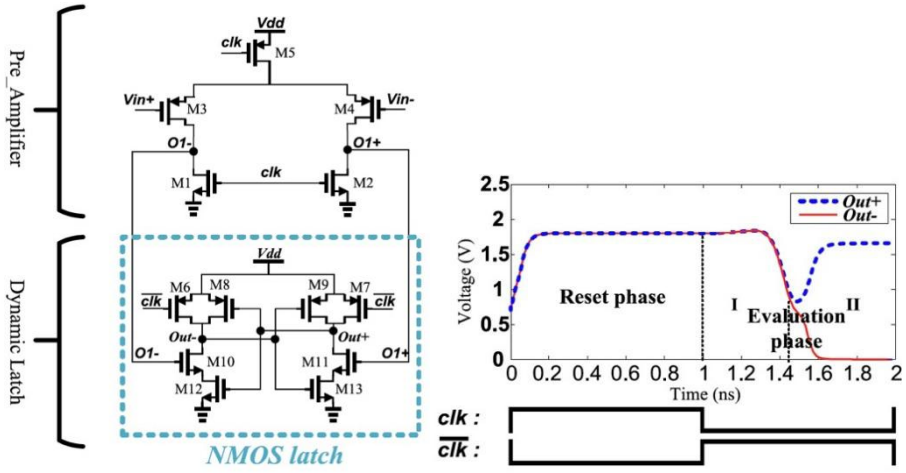



Figure 9. Traditional two-stage dynamic comparator

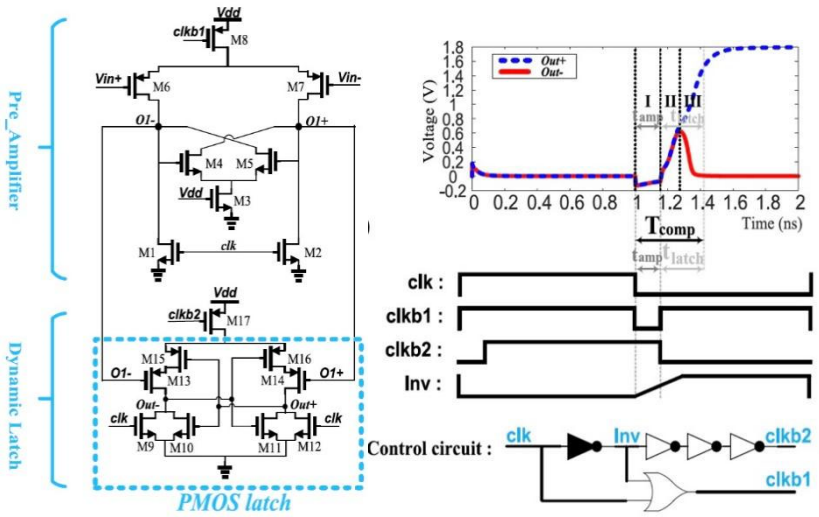



Figure 10. Proposed two-stage dynamic comparator

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{VDD-GND}{V_{idl}}\right) + \frac{K_{latch}}{\left(VDD-V_{cml}-V_{thp}\right)^2}, \quad (8)$$

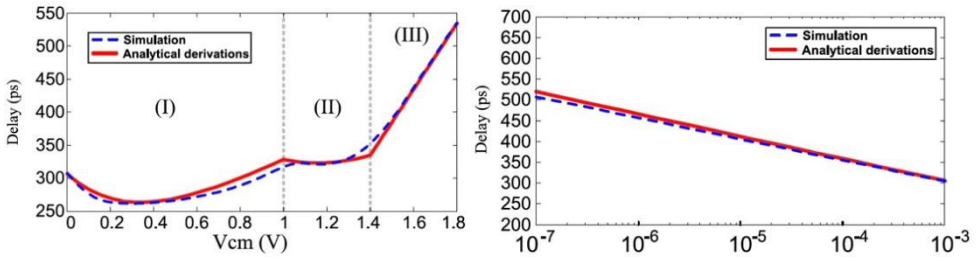
$$Power \cong \frac{t_{amp}}{T} VDD \times I_{M8}, \quad (9)$$

The latch delay, part of the comparison delay, is defined by equation (8) [8]. And the total power consumption can be calculated as (9).

These two equations can be taken as example for further discussion. When an index of the circuit need to be changed to satisfy the requirement, parameters that are independent of the formula should be adjusted preferentially for the sake of not influencing another indexes. For instance, in formula (9), $t_{amp}$ is one of the independent parameters. So parameters like $t_{amp}$ should be somehow changed first when there is a need to alter power.

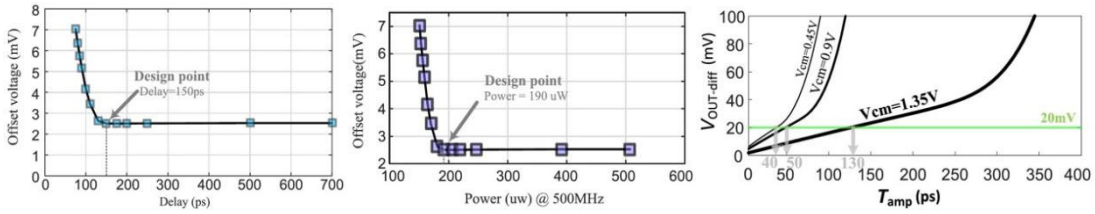
Then parameters that have great influence on the indexes, like some that have high order, should be adjusted earlier. For example, in equation (8), VDD-GND is in a logarithmic term, which means even if it changes a lot, the result of $t_{latch}$ will just have a little change. So adjusting VDD-GND has less meaning than other parameters. Square terms should be adjusted preferentially in most cases.

The direction of change of indexes and parameters should also be figured out. Whether it is the larger the better determines the direction of the adjustment. Take equation (8) as an example. As part of the comparison delay, the latch delay should be adjusted shorter, which means parameter $V_{cml}$ should be smaller, while parameter $V_{idl}$ should be adjusted larger. The simulation result shown in Figure 11 proves the analytical derivations can precisely predict the delay. As $V_{cm}$ decreases or as $V_{id}$ increases, delay gets shorter.




(a) (b)

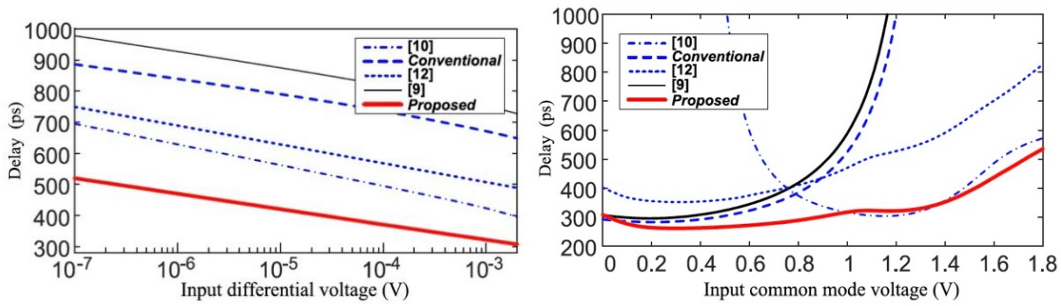
Figure 11. (a) Delay versus $V_{cm}$ (b) Delay versus $V_{id}$




(a) (b) (c)

Figure 12. (a) Offset voltage versus delay (b) Offset voltage versus power (c) Output differential voltage versus $T_{amp}$

And the optimum delay $t_{amp}$ can be determined using Figure 12. As Figure 12(a) and Figure 12(b) show, offset voltage first decreases and then remains stable as delay increases and as power increases, offset voltage has the same trend. Therefore, the offset voltage and delay, offset voltage and power need to make some trade-offs. Parameter $t_{amp}$ should be the minimum value that makes power consumption small enough. Obviously, offset voltage should be 2.5mV, since delay and power are both small at that point. The optimum delay to be chosen should be equal to 150ps. Considering Figure 12(c), preamplifier time need to be longer than 130ps, which is the point where $V_{cm}$ is 1.35V and differential voltage equals 20mV. $t_{amp}$ of 150ps meet that demand apparently.




(a) (b)

Figure 13. (a) Delay versus $V_{id}$ (b) Delay versus $V_{I,CM}$

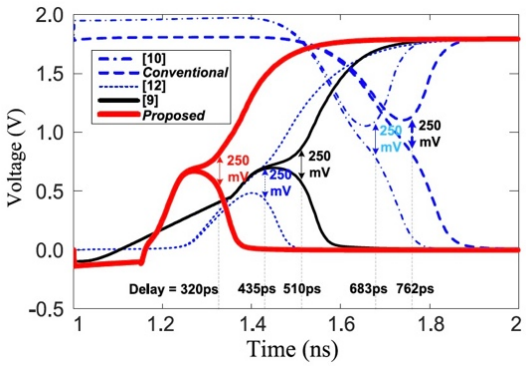
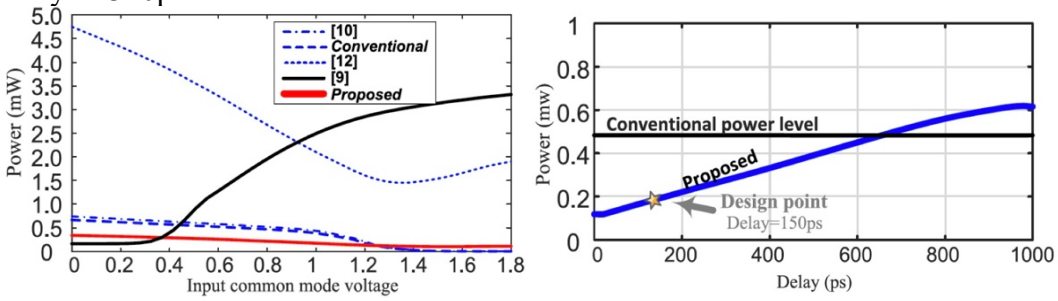



Figure 14. Output waveforms

Figure 13(a) and Figure 13(b) respectively present the trend of change as $V_{id}$ and $V_{I,CM}$ changes. More importantly, they exhibit the comparison with other comparators. As input differential voltage increases, delay of any comparators goes down with almost the same rate of change considering $V_{cm}$ = 0.7V and there is a big difference of the trend of change as input common mode voltage increases. It's worth mentioning that, Figure 13(a) shows delay versus $V_{id}$ when $V_{I,CM}$ is set where the delay of the proposed circuit is shortest. If $V_{I,CM}$ equals other values, the delay time may not be always better as $V_{id}$ changes.

Figure 13(b) reveals that under almost all given $V_{I,CM}$, the delay performance of proposed circuit is better than any other given circuit.

The output waveforms shown in Figure 14 also indicate that proposed circuit is fastest with the shortest delay of 320ps.




(a) (b)

Figure 15. (a) Power versus $V_{I,CM}$ (b) Power versus delay

Apparently, under all $V_{I,CM}$, the energy efficiency of proposed comparator is high, which is shown in Figure 15(a). It is worth noting that some other comparators have power that are quite larger than conventional comparator, whose power consumption performance are sacrificed to improve other aspects of performance. Power consumption versus delay is presented in Figure 15(b). The conventional circuit has a fixed power level because of the fixed $t_{amp}$. As is revealed in formula (9), as delay time increases, the power consumption increases with a linear relationship. When delay is shorter than about 650ps, the power consumption is lower than conventional circuit. A 150ps-delay obviously meet the requirement.

Considering Figure 13(b) and Figure 15(b) simultaneously, the appropriate range for $V_{I,CM}$ can be obtained. From the perspective of the changing trend, as $V_{I,CM}$ increases, the delay is prolonged, while the power consumed is decreased. Therefore, there is a contradictory relationship between the two, thus $V_{I,CM}$ needs to be set to a moderate value. From the perspective of the rate of change, the curve is relatively flat when $V_{I,CM}$ is between 0.2V and 0.8V and between 1V and 1.2V. Power consumption, however, varies at a relatively constant rate. Considering the performance comparison with other comparators, when $V_{I,CM}$ is between 0.6V and 0.8V, delay has a relatively high optimization degree. The proposed circuit has lower power consumption than any other comparator when $V_{I,CM}$ is between 0.4V and 1.2V. To sum up, $V_{I,CM}$ should be set between 0.6V and 0.8V, which is consistent with the 0.7V obtained in the original article. However, if the circuit has high power requirements and can accept a slightly higher delay, $V_{I,CM}$ can be set between 1V and 1.2V.

Table.1. Comparison between the indexes of comparators when $\sigma_{offset} = 2mV$

| | Conventional | [9] | [10] | [12] | Proposed |
|---|---|---|---|---|---|
| Average power at 500MHz | 0.48 mW | 0.44 mW | 2.3 mW | 2.75 mW | 0.20 mW |
| Estimated area ($\mu m^2$) | 440 | 370 | 580 | 1100 | 490 |
| Delay | 301 ps | 303 ps | 313 ps | 370 ps | 263 ps |
| $V_{cm}$ range at 500MHz | 64% VDD | 66% VDD | 71% VDD | 100% VDD | 100% VDD |
| $\sigma V_{noise\text{-}in}$ | 24.6uV | 28.4uV | 34.2uV | 65.5uV | 28.6uV |

In Table.1, different kinds of performance of these comparators are compared. As mentioned above, the power and delay performance of proposed comparator are optimized. At the same time, the size of the circuit and noise performance remain almost the same, while other comparators are unable to optimize some performance while keeping others constant.

## 4. Dynamic bias comparator

For the sake of reducing the amount of discharge on $D_i+$ and $D_i-$, a kind of technique named dynamic bias can be used, which is a simple method and the overhead is less. To control the discharge

from $D_i$+ and $D_i$-, it adds a capacitor in the tail of the pre-amplifier. For a given charge transfer, to achieve maximum voltage gain, it reduce the bias current with the intension of making the operation takes place in weak inversion region. It is an energy efficient mechanism for biasing. Based on dynamic biasing, the idea of a new comparator is put forward in order to reduce the energy.

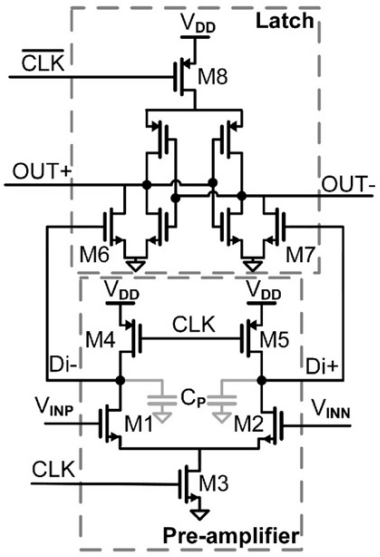



Figure 16. Double-tail latch-type comparator [9]

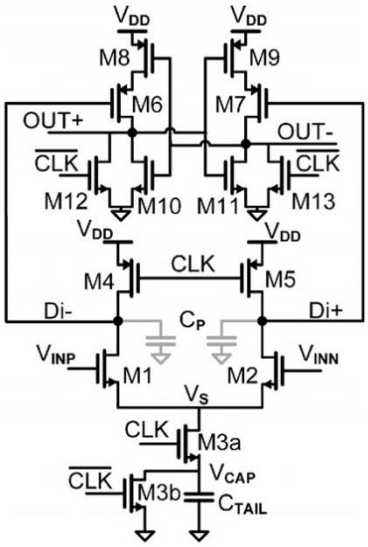



Figure 17. Proposed dynamic bias comparator

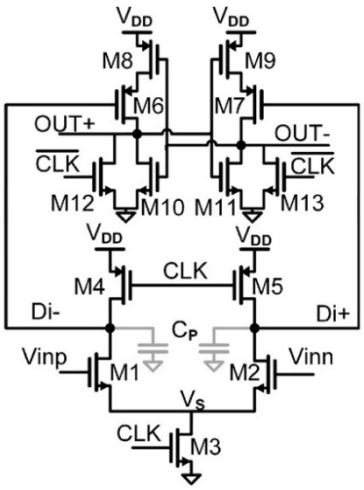



Figure 18. Elzakker's comparator [10]

The proposed circuit has a small propagation delay since for low input differential voltages, the operation mostly takes place in weak inversion region, which features high voltage gain and low noise and it operates with a large $V_{ov}$ for large $V_{id}$. Nevertheless, for small $V_{id}$, the CLK-Q delay is relatively higher compared to Elzakker's comparator because the gain-bandwidth is lower.

$$A_V(T_{INT}) = \frac{C_{TAIL}}{2n \cdot C_P} \cdot \frac{V_S(T_{INT})}{\frac{kT}{q}}, \tag{10}$$

$$E\left[v_{n,WI,in}^2(T_{INT})\right] = \frac{2nkT}{C_P \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{gm}{I_{CM}}\right)_{WI,T_{INT}}}, \tag{11}$$

The analysis of voltage gain and noise of proposed pre-amplifier are both completed. Equations (10) and (11) are deduced [11], [12]. We can make some further discussion on these two formulas.

If some performance indexes should be somehow changed to meet the requirement, parameters

that are independent should be adjusted first. For instance, $C_{TAIL}$ is an independent parameter, which is not related to $E\left[v_{n,WI,in}^2(T_{INT})\right]$, which means adjusting $C_{TAIL}$ will not influence the other index.

Parameters that have greater influence on the index should be noticed. But in these two formulas, each parameter has the same order, so to some extent, there is no big gap between the magnitude of influence of these parameters.

The direction of adjusting, which means whether the parameter should be adjusted larger or smaller, should also be attached great significance. In the equation (10), if $\mathrm{A_V\left(T_{INT}\right)}$ is the larger the better, then parameter $\mathrm{C_{TAIL}}$ should be adjusted larger and parameter $\mathrm{C_P}$ should be adjusted smaller. For noise, if design index $\mathrm{E\left[v_{n,WI,in}^2(T_{INT})\right]}$ is asked to be small, then parameter $\mathrm{C_P}$ should be large. Taking the two demands into consideration, parameter $\mathrm{C_P}$ is supposed to be a compromise value.

$$A_V(T_{INT}) = \frac{g_m \cdot \Delta V_{Di,CM}(T_{INT})}{I_{CM}}, \tag{12}$$

By analyzing constant tail current pre-amplifier, a formula of voltage gain is deduced as (12). In (10), some parameters that are easy to adjust, such as $\mathrm{C_{TAIL}}$, can influence voltage gain of proposed pre-amplifier. However, for constant tail current pre-amplifier, voltage gain cannot be adjusted intuitively. The convenience of changing the value of voltage gain $\mathrm{A_V\left(T_{INT}\right)}$ is an advantage of dynamic bias pre-amplifier compared to constant tail current pre-amplifier.

$$\mathrm{E\left[v_{n,SI,in}^2(T_{INT})\right]} = \frac{4kT\gamma}{\mathrm{C_P \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{gm}{I_{CM}}\right)_{SI,T_{INT}}}}, \tag{13}$$

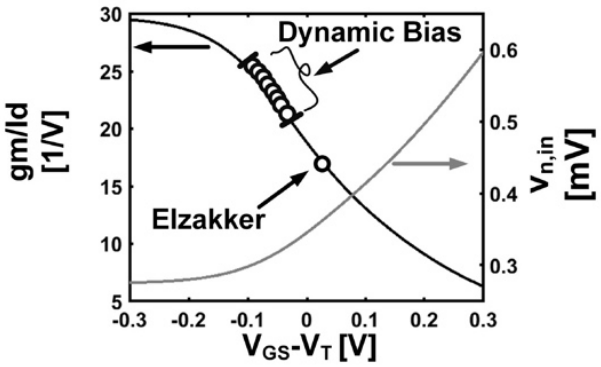



Figure 19. gm/Id and $\mathrm{V_{n,in}}$ versus $\mathrm{V_{GS} - V_T}$

The noise index of two comparators, which is respectively in strong inversion and weak inversion, shown in the form of the following two formulas, are analyzed as (11) and (13). The value of numerator of these two mathematical expressions are almost same. Figure 19 indicates that, with the increase of the overdrive voltage, gm/Id decreases, and input referred noise also decreases. For the differential pair biased near weak inversion region when t is equal to 0+, dynamic bias comparator has a continuously increasing $\mathrm{V_s}$, which makes that throughout the whole integration time, the gm/Id is higher. So proposed dynamic bias comparator successfully improve the noise performance.

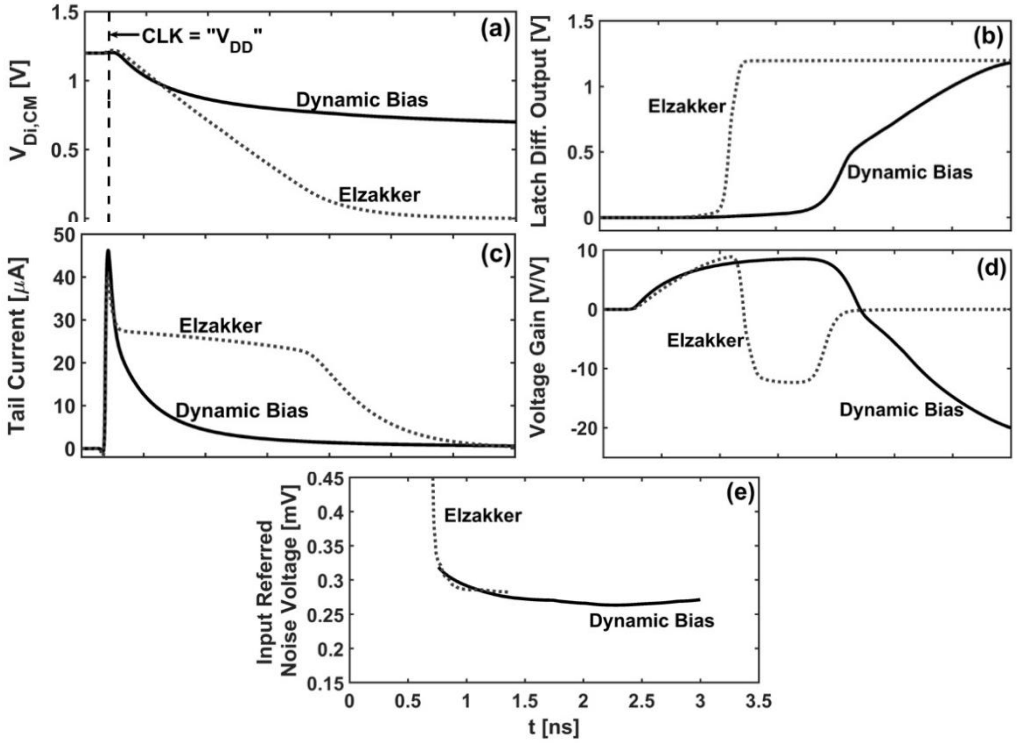



Figure 20. (a) $V_{Di,CM}$ versus time (b) differential latch output versus time (c) tail current versus time (d) voltage gain versus time (e) input referred noise voltage versus time

Five pictures in Figure 20 with regard to simulated indexes of proposed comparator and Elzakker's comparator, can be divided into three categories, which are power consumption, noise and delay performance. Figure 20(a)(c)(d) three pictures show the improvement of the energy efficiency of proposed comparator compared to Elzakker's comparator. Figure 20(e) reflects that noise performance of the proposed circuit is also optimized. Figure 20(b) reveals the disadvantage of proposed circuit, which is delay performance.

In Figure 20(a), $V_{Di,CM}$ of the proposed comparator changed steadily. On the other hand, $V_{Di,CM}$ of Elzakker's comparator dropped rapidly to 0, indicating that the working state of dynamic bias comparator was relatively stable. It does not need to carry out frequent charging and discharging, which also reduces the power consumption.

Figure 20(c) indicates that both of the two comparators had an impact current when the switch was on. The proposed dynamic bias comparator rapidly dropped to 0, while Elzakker's comparator kept producing current and only dropped to 0 after a relatively long time. The two have the same $V_{DD}$, but the average current of the former is smaller, indicating the power consumption of the former is lower.

As is shown in Figure 20(d), the proposed circuit has a relatively stable pre-amplifier voltage gain, while the gain of Elzakker's comparator had a large variation. It also indicates that the working state of the proposed circuit is relatively stable and therefore the consumed power is low.

Obviously, it can be seen from Figure 20(e) that the proposed circuits has relatively smaller input referred noise than Elzakker's comparator, indicating that its noise performance was relatively better.

However, as mentioned above, not every aspect of the proposed dynamic bias comparator's performance has been optimized.

As can be seen from Figure 20(b), Elzakker's comparator can output logic 1 quickly, whereas the proposed dynamic bias comparator takes a long time. Therefore, compared with Elzakker's comparator, the delay of dynamic bias circuit is longer and the performance of delay is relatively deteriorated.

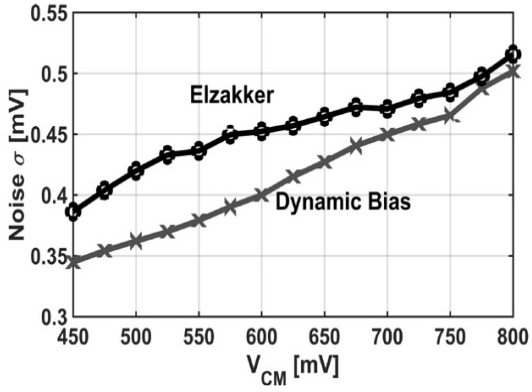



Figure 21. Input referred noise versus $V_{CM}$

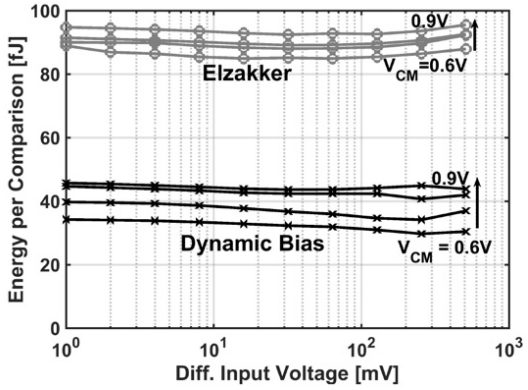
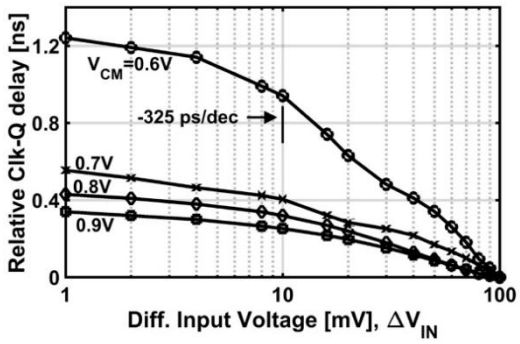
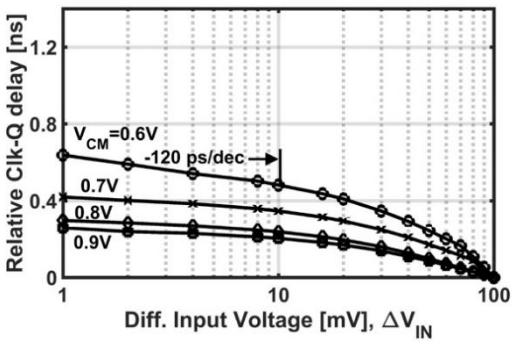



Figure 22. Energy consumption versus differential input voltage




(a)




(b)

Figure 23. (a) Relative CLK-Q delay of dynamic bias comparator versus differential input voltage (b) Relative CLK-Q delay of Elzakker's comparator versus differential input voltage

From Figure 21 and Figure 22, it is easy to find that under all given $V_{CM}$, the noise performance of proposed circuit is better than Elzakker's comparator and under all given differential input voltage, the power performance of the former is also better than the latter. As $V_{CM}$ increases, the noise index $\sigma$ increases, but the gap between the two comparators is getting smaller. The difference between the noise performance of them tends to be small as $V_{CM}$ increases.

Figure 23 shows that under almost all given differential input voltage, relative Clk-Q delay of proposed circuit is larger, meaning the delay performance is poorer than Elzakker's comparator. Obviously, the difference of them is also getting smaller as differential input voltage increases. Relative Clk-Q delay of proposed circuits is quite large, close to 1.2ns, when differential input voltage is small and $V_{CM}$ is also small, which is what should be avoided.

As can be seen from Figure 19, $V_{ov}$ is a negative number, meaning the transistors are working at sub-threshold region. Considering what is revealed in Figure 23, it is not hard to notice that low $V_{ov}$ is the cause of the deteriorative delay performance.

## 5. Conclusions

Some improvement schemes of comparators are discussed in this work. For instance, the FIA architecture is proposed to solve the problem of the failure of the integration of CMOS DB integration pre-amplifier and improve the power consumption and noise performance. In addition, the input of both preamplifier and latch are controlled by a specially designed local clock generator with cross-coupled transistors of another proposed circuit in order to realize a comparator that has low power

consumption and high speed.

With a dynamic bias pre-amplifier, a proposed circuit is implemented to optimize both the performance of energy efficiency and noise. The energy consumed is more than 2.5 times less than the Elzakker's comparator. Nevertheless, there is a disadvantage that the delay performance is deteriorated. Improving the delay performance while maintaining the optimization of energy efficiency and noise performance is the research direction and focus of researchers in the future.

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