Comparative Study of High Speed ADCs

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Abstract. With the development of information technology, analog-to-digital converter (ADC) is widely used. In products such as radar, ultra wideband communication system, high-performance digital oscilloscope and so on, the speed performance of analog-to-digital converter is usually the bottleneck of the whole system performance, so the research of high-speed ADC has attracted much attention. ADC is an interface circuit that converts analog signals into digital signals that can be processed by DSP. This paper will start with the basic knowledge of ADC, explain the general working process of ADC, introduce several architectures and working principles suitable for high-speed ADC, and compare and analyze their advantages and disadvantages.

Keywords: analog-to-digital converter (ADC), ultra wideband communication system

1. Introduction

Since the development of analog-to-digital converter technology, there have been a variety of ADCs suitable for different scenarios. Some of them can not be used to design GSPS level ADCs due to the limitation of working principle, such as successive approximation ADCs, that is, SAR ADCs. Dichotomy is the basic working idea of SAR ADC. An n-bit saradc needs n time periods to quantize a digital output code, which is suitable for low-power design but not suitable for high-speed ADC [1]. At present, the commonly used high-speed ADC architectures generally include full parallel, two-step, folding interpolation, pipeline, and time interleaving technology, which will be described in detail below. In addition, in addition to the above architectures, there are also hybrid ADCs suitable for High-Speed ADCs, such as pipeline successive approximation ADCs [2,3].

2. Types of high-speed ADC

2.1 Flash adc

Flash ADC can complete quantization and output at the same time in one clock cycle, without the complicated signal amplification and signal conversion process. Therefore, it has been considered as an analog-to-digital converter with the simplest structure and the highest conversion rate of single channel [4]. An n-bit full parallel ADC is shown in Figure 1. Its main body only includes a resistor string, a comparator and a digital coding circuit.

The basic working process is that the input signal is connected to one input terminal of all comparators, and the other input terminal of the comparator is connected to different reference voltages, wherein the reference voltages are generated by the resistor string. At this time, the comparator obtains the digital output under the control of the clock, which is in the form of thermometer code, and needs to be converted into the commonly used binary code by the digital circuit to complete the signal conversion.

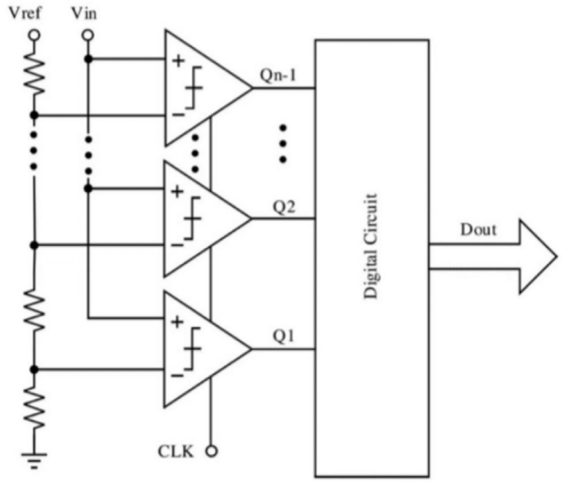


Figure 1. Structure diagram of flash ADC.

It can be seen from the working process that the full parallel ADC can complete quantization and output at the same time in one clock cycle, and can realize extremely fast data conversion. Since only the comparator in the ADC is an analog circuit, theoretically speaking, the sampling rate of the ADC is only determined by the working speed of the comparator, and the improvement of ADC accuracy only needs to increase the number of resistors and the number of comparators. However, in practical application, its accuracy is generally below 8 bits, and the factors of low accuracy include area and power consumption; Influence of parasitic capacitance; Non linearity of reference voltage; The misalignment between multiple comparators leads to nonlinearity; In addition, clock jitter will also have a great impact on ADC. Due to the influence of the above factors, the accuracy of full parallel ADC is low in practical application, which limits its application range.

2.2 Two step adc

In order to alleviate the problem that the power consumption, area and parasitic capacitance of the comparator input end of the full parallel ADC increase exponentially with the increase of the resolution, a two-step structure can be considered [5]. Its basic structure is shown in Figure 2. An n-bit two-step ADC includes a sample and hold circuit, two sub ADCs (coarse quantization m bits, fine quantization L bits), a DAC circuit, a subtraction circuit and a logic circuit, where N = M + L. The two sub ADCs are fully parallel.

The working principle of the two-step ADC is that the input signal is sampled first and then quantized by the coarse quantization sub ADC to obtain m-bit coarse quantization codewords. On the one hand, the quantized code is stored in the latch and represents the high m-bit quantized codeword of the ADC. On the other hand, it is restored to the analog voltage via the DAC circuit. At this time, the same input signal and the output value of the DAC are processed by a subtraction circuit to obtain a difference signal, which is quantized by another sub ADC to obtain the remaining codeword. Finally, the two groups of digital codewords are combined with the complete digital output code of ADC through the logic circuit to complete the data conversion.

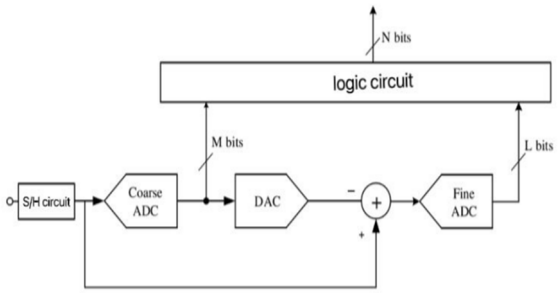


Figure 2. Structure diagram of two-step ADC.

Compared with the full parallel structure, the number of comparators required by the two-step structure is only 2M + 2L-2, and the number of comparators is greatly reduced. The two-step ADC contains some other circuit modules, which makes the circuit design more complicated. Moreover, when the resolution is further increased, the number of comparators will also increase rapidly, and there will also be similar problems such as the nonlinearity of the reference voltage and the nonlinearity introduced by the offset between multiple comparators.

2.3 Pipeline adc

Pipeline ADC is evolved from two-step ADC, which develops two-step ADC into multi-step ADC. The pipeline ADC [6,7] is obtained by expanding the stages of the two-step ADC and connecting it to the inter stage margin amplifier, and the sub ADCs of each stage are usually designed as the same modules to simplify the design, as shown in Figure 3. Among them, the sub ADC is generally composed of Sha, sub ADC, subtractor, sub DAC and margin amplifier, and the latter three circuits are often combined to form a module, i.e. margin gain unit (MDAC). MDAC can realize the function of sample and hold, so the sample and hold circuit is sometimes omitted.

The working process of the circuit is as follows: after the input signal is sampled, it first reaches the sub ADC of the first stage, and after being quantized by it, several digital codes will be obtained. Similar to the processing of the two-step structure, this part of digital codes will enter the digital circuit for processing, and will be restored to the corresponding analog voltage signal by the sub DAC of the stage, and then the input value will be subtracted to obtain a new signal, which will be amplified by the amplifier, And then sent to the next stage circuit as its input. The next stage circuit performs the same processing as the previous stage, and then sends the signal to the next stage circuit until the quantization is completed. Since each stage circuit will output several digital codes, these digital codes will be processed and synthesized into complete digital output codes by logic circuits to realize data conversion.

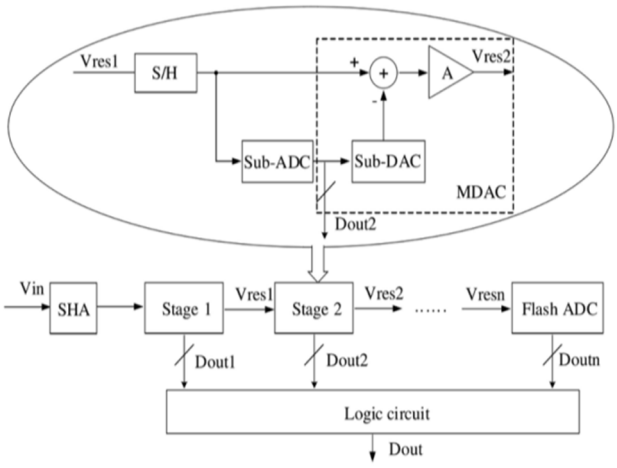


Figure 3. Structure diagram of pipeline ADC.

This ADC adopts the serial design of splitting the design of high-speed and high-precision ADC into many sub ADCs with low accuracy but high speed, which is easier than the design of realizing high-precision and high-speed at the same time through direct quantization. Compared with the two-step ADC, the introduction of pipeline work idea is helpful to improve the accuracy of ADC, but it reduces the conversion rate of ADC. In general, the pipeline ADC is suitable for occasions with high requirements for speed and accuracy. However, when the conversion rate exceeds 4GSps, it is difficult to realize a single-channel pipeline ADC due to the requirements of inter stage operational amplifier performance and process factors.

2.4 Time interleaving adc

Strictly speaking, the time interleaved ADC [8,9] is not an ADC with an independent architecture and cannot be paralleled with the previous ones. Time interleaving is a technology that can be applied

to different types of ADCs. It is an important method to improve the conversion rate by using chip area and power consumption in exchange for the improvement of ADC sampling rate. ADCs using time interleaving technology can be called time interleaved ADCs.

The emergence of time interleaving technology is due to the fact that the comprehensive performance of ADC is fast reaching the limit that can be reached by the process. It is impossible to significantly improve the performance of ADC by adopting any existing architecture at that time. Therefore, it is proposed to use multiple ADCs for alternating sampling to break through the process limit, which is the time interleaved ADC. Its working principle block diagram and the timing diagram are shown in Figure 4 and 5 respectively.

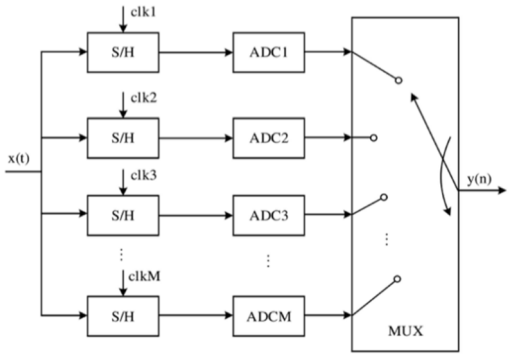


Figure 4. Working principle block diagram of time interleaving ADC.

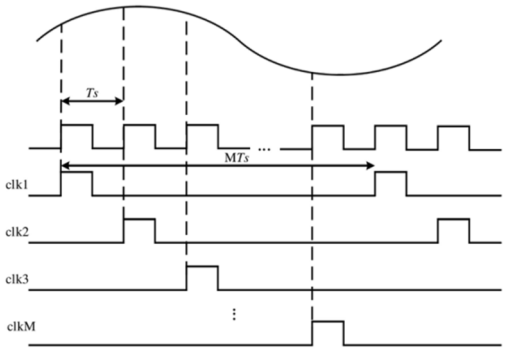


Figure 5. Timing diagram of time interleaved ADC.

The working principle of time interleaving ADC is that M sub ADCs work in parallel at the same time without mutual interference. They sample and quantize the input signal x (t) in order under the control of the clock. The digital code quantized by each sub ADC will be synthesized into a complete digital output by the subsequent circuit, i.e. signal Y (n). clk1, clk2, clk3... clkM are the clock signals of the sub ADCs, which are used to control the orderly sampling of each sub circuit.

The timing chart shows that the time interval of the sampling points of the sub ADCs sampled in order is 1Ts, where Ts is the system clock cycle. Since M channels are sampled alternately, the sampling period of the sub ADC is M times of the system clock period. In an ideal case, the time interleaving technique can increase the conversion rate of the ADC to M times that of the sub ADC, and the resolution can be kept consistent with that of the sub ADC.

Theoretically, the ADCs of each sub channel should be completely consistent, but the actual situation is that the process factors will bring many non ideal factors, which have little impact on the sub ADCs, but will cause mismatch between channels, thus reducing the performance of the ADC. In general, sampling time mismatch, gain mismatch and offset mismatch are the three main error sources [10]. Therefore, excellent calibration technology is required when using time interleaving technology, otherwise, the speed of the entire ADC may not be improved, but the accuracy may be decreased.

2.5 Folding interpolation adc

Similar to the two-step ADC, the folded interpolation ADC [11,12] is also proposed to solve the problem that the number of comparators in the full parallel ADC increases exponentially with the increase of resolution. Its structural block diagram is shown in Figure 6. It can be seen from the figure that an N-bit folding interpolation ADC includes a sample and hold circuit (S/H), a folding interpolation circuit, an M-bit coarse quantization sub ADC and an L-bit fine quantization sub ADC, where N = L + M. In terms of structure, folded interpolation ADC is very similar to two-step ADC. Both of them generate high-order digital quantization code and low-order digital quantization code through two sub ADCs. The difference is that the fine quantization module in the folding interpolation ADC first performs folding preprocessing on the analog input signal, and then sends the folded signal to the fine quantization sub ADC. The schematic diagram of the folded signal is shown in Figure 6. The advantage of this is that the equivalent full swing range of the input signal of the fine quantized sub ADC is greatly reduced, and the number of comparators in the ADC can be effectively saved.

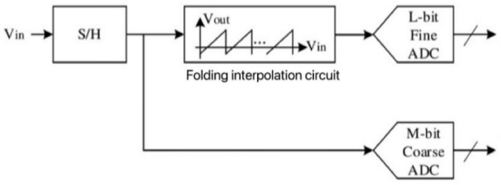


Figure 6. Structure block diagram of folded interpolation ADC.

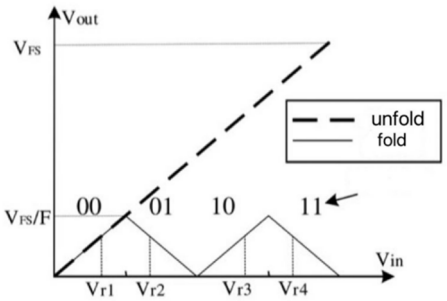


Figure 7. Schematic diagram of folding signal.

The working principle of folding interpolation ADC is as follows: the analog input signal first passes through the sample and hold circuit, and then the signal is divided into two parallel paths, one of which is to send the sampled signal to the folding amplifier for folding preprocessing, and obtain the low L-bit quantized code word through the fine quantizer ADC. Figure7 shows that the slope signal is folded. The folding coefficient F means that the entire input signal range is divided into F segments, and the amplitude of the folded signal will be reduced to 1 / F of the original; The other signal passes through the coarse quantization module, and the coarse quantization sub ADC quantizes the high m-bit digital code. After the coarse quantization, it is equivalent to dividing the signal full swing interval into 2M intervals. The high-order output digital code represents the coarse quantization circuit to determine which interval the current input signal falls in

From the mapping relationship, the folding amplifier maps all the input signals before folding to the same section, and then quantizes them into digital output codes by the fine quantization sub ADC, that is, a digital output code with low L bits is obtained. The high m-bit digital code output by the coarse quantization module and the low L-bit digital code output by the fine quantization module together constitute the N-bit digital output code of the folded interpolation ADC, that is, the analog-to-digital conversion process is completed. From the number of comparators, for an n-bit ADC, if the folded interpolation structure is adopted, the number of comparators is (2N/F-1+2M-1), and if the full

parallel structure is adopted, the number needs to be 2n. Assuming N = 8 and M = 3, the number of comparators required by the two structures is 38 and 256 respectively. Thus, the folded interpolation structure can effectively reduce the number of comparators.

The output end of the folding amplifier uses the interpolation technology. The initial purpose of the interpolation technology is to reduce the number of comparators in the full parallel ADC and reduce the total parasitic capacitance. Since the folded amplifier multiplies the input signal, it is easy to cause distortion and introduce nonlinearity. The introduction of interpolation technology can improve the nonlinear distortion of the folded signal and reduce the number of folded amplifiers.

From the perspective of ADC speed, the folded interpolation ADC quantizes the signal through two sub ADCs synchronously, and only needs one clock cycle to obtain the quantized digital code. Therefore, it can also achieve the same sampling rate as the flash ADC.

3. Performance comparision of various adc

Different systems have different requirements for ADC performance, so there are many kinds of ADCs to meet different systems. In the development process of high-speed ADC, several classical structures have appeared. The above describes several common architectures currently applicable to high-speed ADC design, expounds their working mechanism in detail, and objectively introduces their advantages and disadvantages. Namely, two-step ADC, flash ADC, folding & interpolating ADC, pipelined ADC and time interleaving ADC. These types of ADCs have their own advantages and disadvantages, which can meet different specific application requirements. The performance comparison of these five ADC structures is shown in Table 1.

Table 1. Performance comparison.

	Accuracy	Speed	Power Dissipation	Area
Two step	high	medium	low	small
Flash	low	fast	high	largest
Folding&Interpolation	medium	fast	medium	medium
Pipelined	medium	fast	medium	large
Time interleaving	high	slow	high	large

It can be seen that flash ADC is a good structural choice in low resolution and ultra-high speed applications. Compared with flash ADC, the two-step ADC contains some other circuit modules, which makes the circuit design more complex. Therefore, the two-step ADC is only suitable for the application scenarios with low requirements for ADC accuracy. The characteristics of the folding mode are that the two quantizations of the data are carried out at the same time, with the characteristics of full parallel transformation and fast speed; The circuit scale and power consumption are not large. Pipelined ADC has the following characteristics: it simplifies the circuit design and combines the advantages of serial parallel converter and algorithm correction converter; The number of devices used is proportional to the number of conversion bits, and the hardware consumption and power consumption are limited; High accuracy is achieved by digital correction circuit, and the performance of the functional circuit used is not high; Although the analog signal needs to undergo multi-stage conversion, because each stage has its own independent sample and hold amplifier, the sample / hold of the previous stage circuit can be released for processing the next sample, so it is allowed that each stage of the pipeline can process multiple samples at the same time, so analog signals are processed in parallel, so high conversion speed can be achieved; Multilevel conversion improves the resolution of A / D converter; The input signal must pass through several stages of circuits, causing pipeline delay; Complex reference circuit and bias structure; Strict latch timing is required to synchronize all outputs.

Time interleaving technology has three advantages. First, the technology has high flexibility and can be applied to ADCs of various architectures. For ADCs with excellent performance, time

interleaving technology can be considered to further improve ADC performance; Secondly, the processing of digital codes is relatively free. The digital output codes of sub ADCs can be combined first and then processed, or processed first and then combined; Finally, the time interleaving technology improves the conversion rate of the ADC, but the clock frequency of the sub ADCs in each channel does not change, which makes it possible to reduce the requirements for the sampling rate when designing the sub ADCs and pay more attention to the improvement of the ADC accuracy. This practice is more conducive to achieving the ultimate goal of high-speed and high-precision analog-to-digital conversion.

4. Conclusion

With the rapid development of computer technology, communication technology and microelectronics technology, the development of ADC technology has been greatly promoted. As a key component of analog and data interface, ADC is widely used in various fields and plays an important role in information technology. Like computers, ADC has experienced the development from low speed to high speed. This paper first introduces the basic concept of ADC and the basic working process in signal processing. Then, several common architectures suitable for high-speed ADC design are described. Their working mechanism is described in detail, and their advantages and disadvantages are objectively introduced and compared.

References

[1] C. Liu, S. Chang, G. Huang, et al. A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure. IEEE Journal of Solid-State Circuits, 2010, 45(4):731-740

[2] J. Kuppambatti, P. R. Kinget. Current Reference Pre-Charging Techniques for Low-Power Zero-Crossing Pipeline-SAR ADCs. IEEE Journal of Solid-State Circuits, 2014, 49(3): 683-694

[3] J. Gao, G. Li, L. Huang, et al. An Amplifier-Free Pipeline-SAR ADC Architecture With Enhanced Speed and Energy Efficiency. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 63(4): 341-345

[4] Y. Akazawa, A. Iwata. A 400-MSPS 8b Flash AD Conversion LSI. IEEE InternationalSolid-State Circuits Conference, San Francisco, 1987, 98-100

[5] K. Yoshioka, R. Saito, T. Danjo, et al. Dynamic Architecture and Frequency Scaling in 0.8-1.2GS/s 7 b Subranging ADC. IEEE Journal of Solid-State Circuits, 2015, 50(4): 932-945

[6] S. H. Lewis, P. R. Gray. A pipelined 5-Msample/s 9-bit analog-to-digital converter. IEEE Journal of Solid-State Circuits, 1987, 22(6): 954-961

[7] K. K. Rim, B. Murmann. A 12-b 30-MS/s 2.95-mW Pipelined ADC Using Single-Stage Class- AB Amplifiers and Deterministic Background Calibration. IEEE Journal of Solid-State Circuits, 2012, 47(9): 2141-2151

[8] S. K. Gupta, M. Choi, M. Inerfield, et al. A 1GS/s 11b Time-Interleaved ADC in 0. l3um CMOS. IEEE International Solid-State Circuits Conference, San Francisco, 2006, 2360-2369

[9] C. C. Hsu, F. C. Huang, C. Y. Shih. An 11b 800MS-s Time-Interleaved ADC with Digital Background Calibration. IEEE International Solid-State Circuits Conference, San Francisco, 2007, 464-615

[10] Guanglin Wu. Research and implementation of multi-channel time cross ADC calibration technology. Nanjing: Southeast University, 2006,14-17

[11] Wenwei He. Research and design of key technologies of ultra high speed folding interpolation ADC. Nanjing: Southeast University, 2017, 110-113

[12] Jincan Zhang Research on design method of GaAs HBT ultra high speed folding interpolation ADC chip Xi'an: Xi'an University of Electronic Science and technology, 2014,88-93