# Design analyst of low energy, high gm/Id, and high sensitivity comparator

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**Abstract.** This paper analyses three innovative designs of comparators and those structures have better performance than the traditional comparator. The dynamic floating inverter amplifier improves energy efficiency by preventing full discharging and charging. The Dynamic Bias Latch-Type Comparator used a double-tails latch to decrease energy consumption. The charge-injection compensations comparator has better sensitivity and less noise by utilizing the feedback loop. Those methods have greatly increased voltage gain, energy efficiency, and gm/Id

**Keywords:** Dynamic floating inverter amplifier, Dynamic Bias Latch-Type Comparator, Charge-injection compensations comparator.

## 1. Introduction

Comparator is the fundamental part of IC design and it changes the current or voltage input into digital output. Comparators can be treated as analog-to-digital (ADCs). The novel IC design required a comparator that has a faster switch time, low energy consumption, and greater sensitivity. There is no certain way to optimize and innovate. The novel design can try different circuit structures or utilize common circuit features.

Those three comparators utilized differential circuits, double-tail comparators, and latch structures to improve the features they wanted. [1] added a capacitor to the tail to make Vs change slightly and to prevent the capacitor from discharging and charging fully. By using this method, the energy consumption decreases but the delay time increases compared to Elzakker's design used the trade-off strategy.

For the dynamic floating inverter amplifier (FIA) [2], the authors were inspired by [1], and they found the reason why the delay time increased. Because only holds Vs, the voltage on the pmos is affected by $V_{dd}$ [3], added a capacitor Cres which made a closed loop so that the voltage between pmos and nmos can change dynamically [4]. They made an innovative structure to achieve a balance of energy consumption and delay.

The charge-injection compensation comparator improves another aspect of the comparator. The compensation circuit eliminates the charge-injection error and shortens the time response [5]. Moreover, the offset compensation increases the accuracy.

Those simulation results show that the noise, energy consumption, and gain increase. There are still lots of possibilities to optimize the property of comparators.

This paper also demonstrates the design consideration of the choice of the capacitor and how it affects the expected performance. The order of the paper is shown as follows. Section 2 Introduced the structures of three comparators and their simulation results. Section3 concludes the paper and mentions further improvement direction.

## 2. Architecture Of The Comparators

### 2.1 V Dynamic Bias Latch-Type Comparator

Dynamic means the circuit's parameters will change themselves. The dynamic bias latch-type comparator [6] uses the structure of a double-tail and reduces energy consumption 2.5 times by adding a capacitor in the tail. The authors improved van Elzakker et al to get this structure because they

found out that the discharge and charge of the comparator consume large parts of energy. $C_{Tail}$ can hold Vs so the capacitor did partial discharge and charge. figure 1 showed the proposed schematic

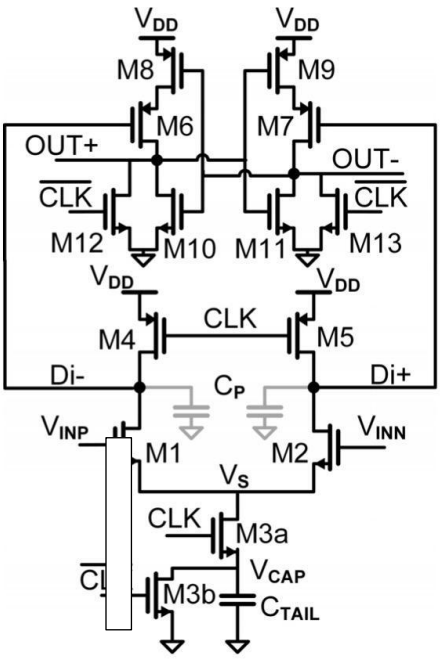



**Figure 1.** Schematic of Dynamic Bias Latch-Type

The voltage gain (1) of Elzakker is proportional to gm/Id but the voltage gain of the dynamic bias comparator (2) is decided by the $C_{Tail}$ /$C_p$.

$$A_V(T_{INT}) = \frac{\Delta V_{Di}(T_{INT})}{\Delta V_{IN}(T_{INT})} = \frac{g_{m*\Delta V_{Di,CM}(T_{INT})}}{I_{CM}} \tag{1}$$

$$A_V(T_{INT}) = \frac{C_{TAIL}}{2n*C_P} \frac{V_S(T_{INT})}{\frac{kT}{q}} \tag{2}$$

The Elzakker and dynamic bias preamplifier's noise current in strong inversion is negatively proportional to Cp and gm/Id.

$$E[v^2_{n,WI,in}(T_{INT}) = \frac{2nkT}{C_P*\Delta V_{Di,CM}(T_{INT})*(\frac{g_m}{I_{CM}})_{Wi,T_{INT}}}] \tag{3}$$

$$E[v^2_{n,SI,in}(T_{INT}) = \frac{4kT\gamma}{C_P*\Delta V_{Di,CM}(T_{INT})*(\frac{g_m}{I_{CM}})_{Si,T_{INT}}}] \tag{4}$$

The pre-amplifier energy $[2 * c_p * V_{DD}^2 - c_p * V_{DD} * (V_{D1} + V_{D2})]$ required is less than the regular energy $2 * C_P * V_{DD}^2$. From the equations, low noise and high gain is achieved by adjusting $C_{Tail}$ /$C_P$ and increasing gm/Id.

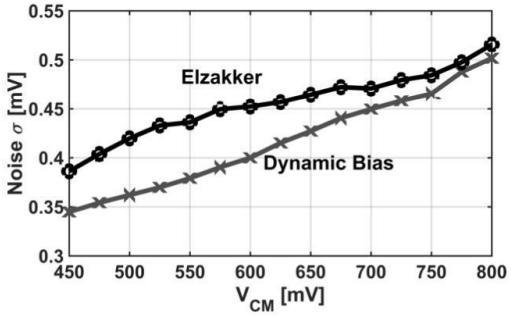



**Figure 2.** The relationship between $V_{cm}$ and Noise.

Figure 2 shows the relationship between $V_{cm}$ and Noise. The dynamic bias comparator has less noise than ELakker under common mode. When the $V_{cm}$ increases, the difference between the two designs becomes small.

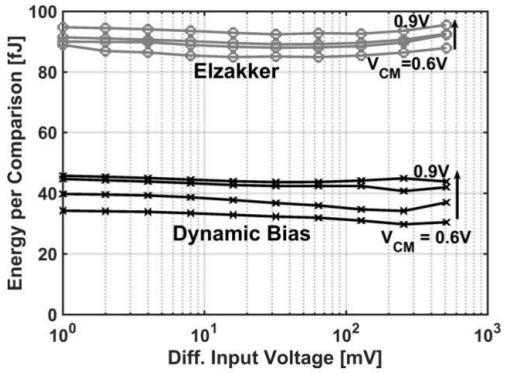



**Figure 3.** The $V_{cm}$ is simulated at values 0.6V, 0.7V, 0.8V, and 0.9V. The relationship between the differential input voltage and energy consumption

Figure 3 and figure 4 are simulation results that can guide researchers on how to set the value of $V_{cm}$. The author of this DB preamplifier mainly focused on energy consumption. $V_{cm}$ =0.8 or 0.7 is the best choice. Although $V_{cm}$ =0.6 can obtain the least energy consumption, the CLK-Q delay is obviously larger than the other three values.

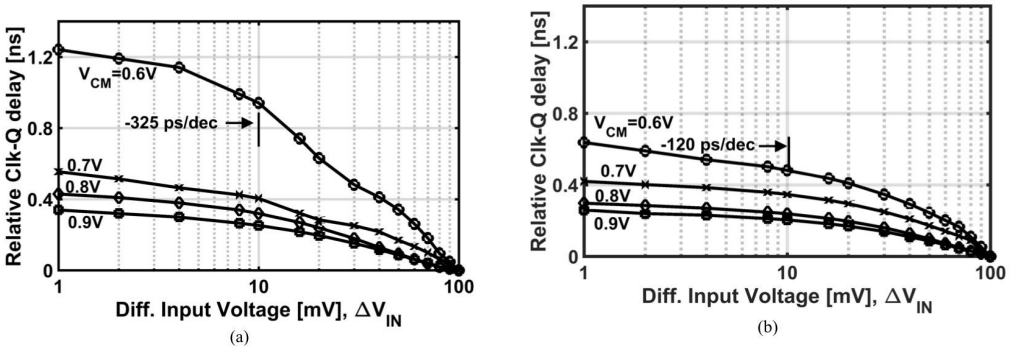



**Figure 4.** The $V_{cm}$ varies from 0.6V to 0.9V and the relative CLK-Q delay is measured.

They did a simulation comparison based on the 65nm CMOS process between the previous design and the current [7]. Figure 5 (a)(c) shows that dynamic dies preamplifiers have more stable $V_{di,cm}$, and higher gain during the amplifier operation time and indicate that this improvement can decrease energy consumption. Figure 5 (b) shows that this method has a larger delay time. (c) means the $C_{TAIL}$ did decrease the tail current. For the consideration of energy consumption, the DB structure is a nice choice.

## 2.2 Dynamic floating inverter amplifier

The FIA comparator contains two parts: A floating inverter pre-amplifier [8] and a strong-arm latch. By using a capacitor to prevent the load from fully charged or discharged and, in the integration phase, improve the gm/Id. Besides those features, this proposed design also can counteract the impact of the process corner and improve the performance of the comparator.

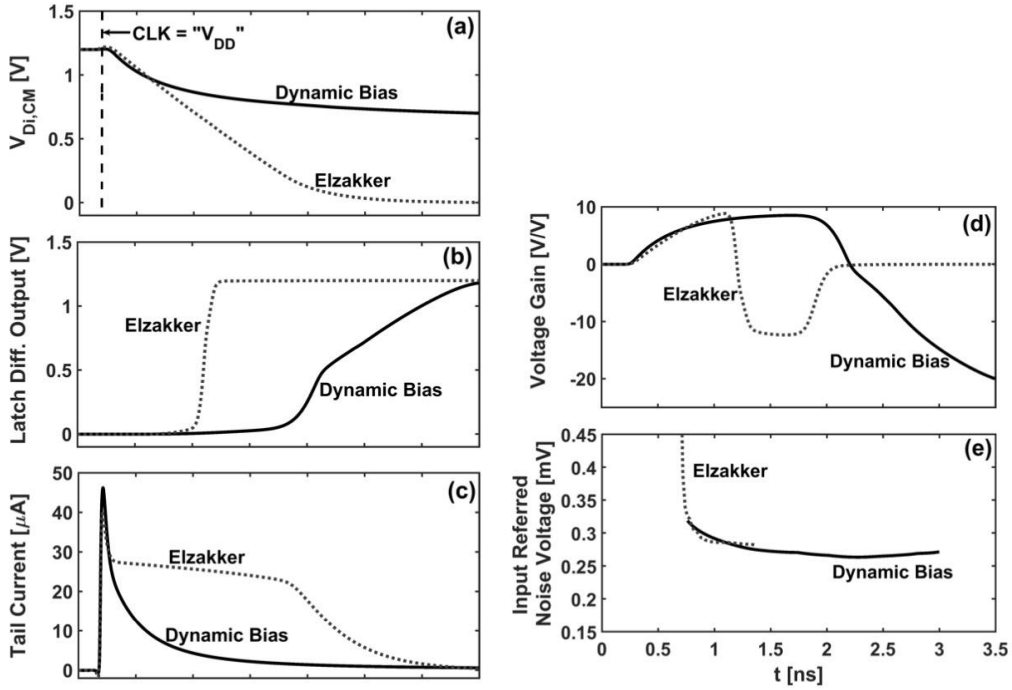



**Figure 5.** Simulation results for the DB preamplifier when the time changes.

Figure 6 shows the pre-amplifier design, they added the capacitor $C_X$ which can prevent the discharge. For the simulation result, the time for dynamically-based NMOS integration is longer than conventional NMOS integration. Moreover, VS and gm/Id are higher than the traditional Nmos integration so this circuit can be noiseless and energy-less. The Vgs-Vth slightly changes and $V_{X,cm}$ has a higher value so comparator performance is improved. In this method, the Vs+ decrease and Vs- increase so that the Gm/Id is double the one in the SA latch. After the simulation result satisfied the expected value, they tested the process corner. The result from the corner test and input common-mode voltage variation shows that this result shows that the voltage between pmos and nmos is not balanced. This means that this circuit cannot be used in the manufactory.

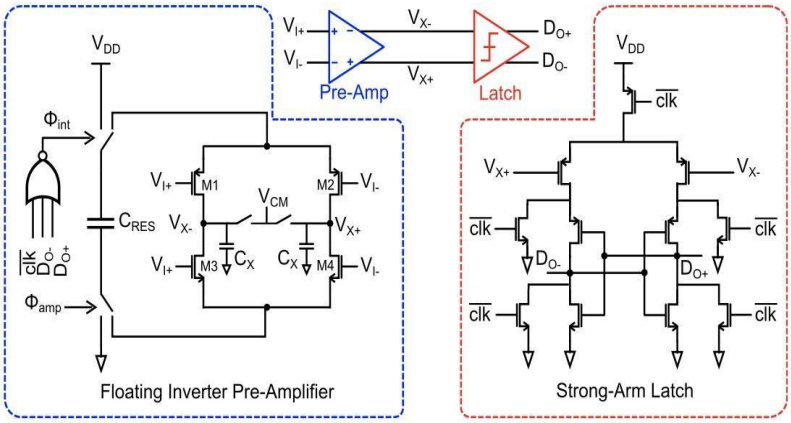



**Figure 6. The Schematic of the proposed Dynamic floating inverter amplifier**

Floating inverter pre-amplifier with reservoir capacitor is a more appropriate solution to let the process corner and input common-mode variation stable. In the previous part, the failure reason is that the voltage of pmos and nmos is not balanced so they tried to combine two tails capacitors into one. As a result, the value of the capacitor becomes 1/2 $C_{TAIL}$ and this is an isolated voltage domain. Therefore, the current flow in the $C_X$ is 0. This design forces the current to be the same so the Vs+ and Vs- will decrease first, and then the Vpgs decrease and Vngs increase. This indicated that this circuit can dynamically adjust the voltage and it can fulfill the condition of its design.

The integration gain is mainly affected by the value of Cres and $C_X$. But basically, $C_X$ can be treated as constant. $C_{RES}$ proportional to pre-amplifier gain. This is not related to gm/Id

$$A_V(T_{INT}) = \frac{\Delta V_{X,DM}(TNT)}{\Delta V_{I,DM}} = \frac{2\Delta C_{RES} * V_S(T_{INT})}{n * C_X * U_T} \quad (5)$$

Those noise voltage equations show the difference among three structures: noise voltage is affected by $C_{RES}$, $C_X$, and Gm/Id. In FIA, $C_X$ affects this value more but is inversely proportional to noise voltage. For DB, the $C_P$ negatively affects the value. For SA, the $C_X$ affects the final value. In conclusion, the capacitor will affect noise voltage. Although the gm/Id also determines the noise voltage, it also depends on the value of the capacitor.

For energy consumption, $G_m/I_d$ affects the cost. ($G_m = g_{m,n} + g_{m,p}$). For SA, VDD affects the energy efficiency more and Vth is constant. The equations indicated that the FIA has a better energy efficiency

$$\sigma^2_{in,SA}(T_{INT}) = \frac{2nkT}{V_{THN} * C_X} * \frac{I_D}{g_m} \quad (6)$$

$$\sigma^2_{in,DB}(T_{INT}) = \frac{2nkT}{C_P * \Delta V_{X,CM}(TNT)} * \frac{I_D}{g_m} \quad (7)$$

$$\sigma^2_{in,FIA}(T_{INT}) = \frac{2nkT}{C_{RES} * \Delta V_S(TNT)} * \frac{I_D}{G_m} \quad (8)$$

For energy consumption, Gm/Id affects efficiency ($G_m = g_{m,n} + g_{m,p}$). For SA, VDD which is the constant affects the energy efficiency more and Vth is constant. The equations indicated that the FIA has a better energy efficiency.

$$FoM_{SA} = \frac{4nkT * V_{DD}^2}{V_{THN}} * \frac{I_D}{g_m} \quad (9)$$

$$FoM_{DB} = 4nkT * V_{DD} * \frac{I_D}{g_m} \quad (10)$$

$$FoM_{FIA} = 4nkT * V_{DD} * \frac{I_D}{G_m} \quad (11)$$

By analysing the equations above, Cres is the most important factor in this design and everything related to capacitors. Although there are several equations that have gm/Id, gm is the interior value and Id depends on the current flow which is affected by the value of Cres. The difficult point is how to decide the value of Cres from the simulation result. The range for the delay is from 8.5 to 11.3 ns and the FoM range from 1.45 to 1.66. As fig FoM vs. Cres shows that when Cres = 2.5, energy efficiency reached the highest value. They chose Cre =2 but I think it is better to choose 3 or four. The author wants to build an energy-efficient comparator and $C_{RES}$=3 is the best option and it also has less delay time. They also can choose $C_{RES}$ = 4, it also has a small FoM and shorter delay time. After all, the range of FoM is small, therefore, Cres doesn't affect it a lot. But large Cres can get the larger amplifier gain value. In reality, parasitic capacitance impact matters, and it will slightly affect the output common-mode voltage. When they decide the value of Cres, they need to consider the percent of post-layout-extracted parasites.

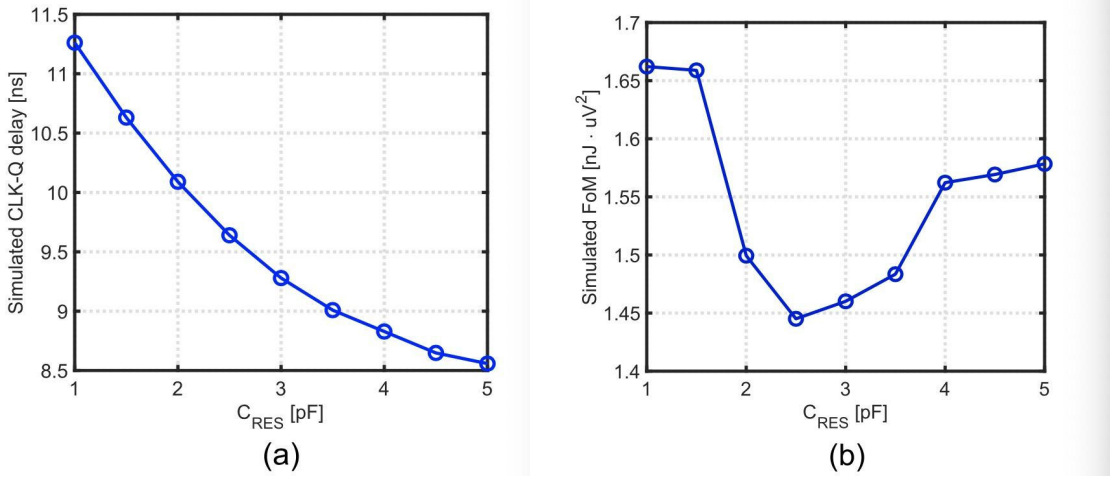



**Figure7.** Simulation result: a) the relationship between Cres and CLK-Q delay. b) the FoM vs $C_{RES}$

## 2.3 Charge-Injection Compensation Comparator

The paper [3] is based on the current mirror structure and it also shows that offset and chancre-injection compensations can improve the property of the CMOS current comparator.

In order to have the expected offset, the control of common-mode voltage, and charge-injection compensation [6], this design contained two parts: a double folded-cascade structure uncompensated comparator and a compensation circuit. In this paper, there are two types of compensation circuits: series-connect and parallel-connect (figure 8). The authors used the AB source-coupled stage and transconductance stage which are the main factor. There will be two operation types [9]. Differential signal for uncompensated comparator and common-mode signal for compensation circuit.

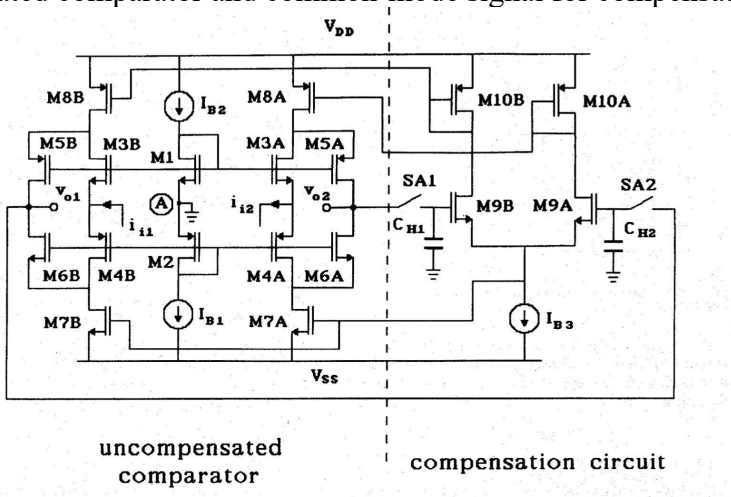



**Figure 8.** Schematic for a proposed fully differential current comparator with charge-injection compensation

There are two connected ways to get the offset: series or parallel. This is the offset current with the charge-injection compensation and this equation is negatively proportional to $g_m/I_d$. By using a larger capacitor Ch, the error is eliminated [10].

$$I_{osc} \cong \frac{I_{os}}{g_m r_o} + g_m \Delta V_{ck} \tag{12}$$

Figure 9 shows that this design achieves the expected goal. Line1 is the voltage without compensation and line 2 is the voltage with compensation. Figure 9 shows the charge-injection error is reduced by using a compensation circuit. The difference between the two methods is around 0.4V [11].

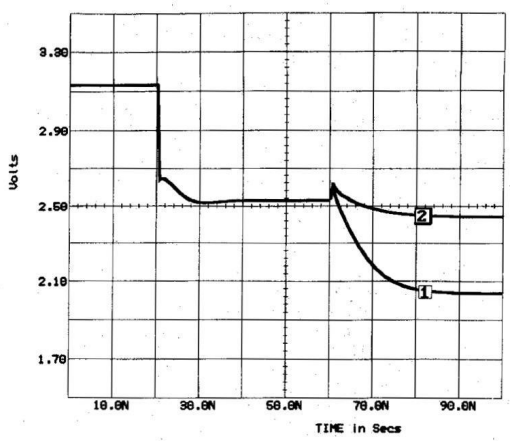



**Figure 9.** simulation result for 1) without charge-injection compensation 2) with charge-injection compensation

Sensitivity is an important parameter in comparators and strong sensitivity detects the input current easier. Figure 10 showed sensitivity related to the time response. The simulation result showed the relationship between input set current and $v_{i1}$-$v_{o2}$. The offset compensation time response is less than 8 ns.

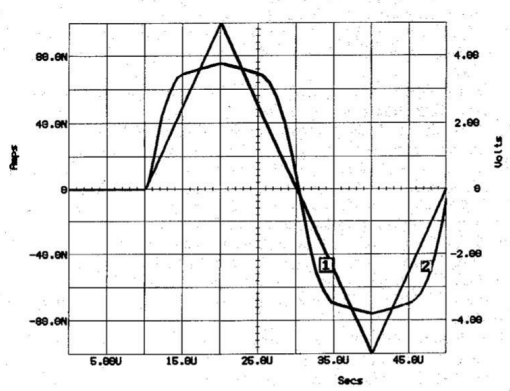



**Figure 10.** simulation result for the sensitivity. 1)input current 2) output voltage

## 3. Conclusion

In this paper, innovative design and optimized methods are introduced. Those three designs focused on how to decrease energy consumption and improve sensitivity. Moreover, the goal of low noise voltage is also achieved. Two of the comparator's designs focused on improving energy efficiency by preventing the process of discharging and charging fully. The DB preamplifier optimized the previous design but the FIA is a novel design by using the capacitor feature. The DB preamplifier comparator demonstrated the dynamic bias methods can reduce around 2.5times of energy consumption under the same conditions as the conventional comparator. The FIA studies the DB preamplifier and creates an innovative design that greatly boosts gm/Id to gain higher energy efficiency and around 30% lower noise than the DB amplifier design. The charge-injection fully differential compensation comparator, which is another optimized method, can reach low to 20nA and it can detect small input signals. Those three comparators need to trade off parts of the performance. The value of capacitors can change the gain, noise, and gm/Id.

In the next step, there are still a couple of values of capacitors to operate and the delay time is not the best option. In those three papers, all discussed how the gm/Id is important to the comparator design. In the future, gm/Id can lead to more innovation and high-performance comparators.

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